SANYO Preliminary	8 BIT SINGLE CHIP MICROCONTROLLER LC87F5664A

LC87F5664A

8-Bit Single Chip Usb(Full-speed) Microcontroller with on-chip 64KB FLASH-ROM and 3072 byte RAM.

Overview

The LC87F5664A microcomputer is 8-bit single chip Usb microcomputer with the following on-chip functional blocks:

- CPU: Operable at a minimum bus cycle time of 83ns
- 64K bytes flash ROM (re-writeable on board)
- 3072 byte RAM
- two high performance 16 bit timer/counters (can be divided into 8 bit units)
- four 8 bit timers with prescalers
- timer for use as date/time clock
- one synchronous serial I/O ports (with automatic block transmit/receive function)
- one asynchronous/synchronous serial I/O port
- PWM × 2
- 8-channel × 8-bit AD converter
- usb serial bus interface engine (conforms to USB Specification, Version 1.1)
- 29-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (Flash ROM)
- single 3.3V power supply, writeable on-board.
- block erase in 128 byte units
- 65535 × 8 bits (LC87F5664A)

(2) Bus Cycle Time
- 83ns (if CF=12MHz)

Note: The bus cycle time indicates ROM read time.

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(3) Minimum Instruction Cycle Time : 250ns (if CF=12MHz)

(4) Ports

- Input/output ports

Each bit data direction programmable	40	(P1n, P2n, P70 to P73, P8n, SI3P0 to SI3P3, PBn)
Nibble data direction programmable	8	(P0n)
- Input ports	2	(XT1,XT2)
- PWM Output ports	2	(PWM0,PWM1)
- Oscillator pins	2	(CF1,CF2)
- Reset pin	1	($\overline{\mathrm{RES}}$)
- Power supply	6	(VSS1 to 3,VDD1 to 3)
- USB ports	2	(D+, D-)
- FILTER port	1	(FILT)

(5) Timers

- Timer0: 16 bit timer/counter with capture register
  - Mode 0: 2 channel 8 bit timer with programmable 8 bit prescaler and 8 bit capture register
  - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register + 8 bit counter with 8 bit capture register
  - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
  - Mode 3: 16 bit counter with 16 bit capture register
- Timer1: PWM/16 bit timer/counter (with toggle output)
  - Mode 0: 8 bit timer (with toggle output) + 8 bit timer counter (with toggle output)
  - Mode 1: 2 channel 8 bit PWM
  - Mode 2: 16 bit timer/counter (with toggle output)
  - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM output.
- Base timer
  1. The clock signal can be selected from any of the following: sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output for timer 0.
  2. Interrupts can be selected to occur at one of five different times.
- Timer4: 8-bit timer with 6-bit prescaler
- Timer5: 8-bit timer with 6-bit prescaler
- Timer6: 8-bit timer with 6-bit prescaler
- Timer7: 8-bit timer with 6-bit prescaler

(6) SIO

- SIO0: 8 bit synchronous serial interface
  1. LSB first/MSB first function available
  2. Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 T_{CYC})
  3. Continuous automatic data communications (1 - 256 bits)
- SIO1: 8 bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8 bit serial IO (2-wire or 3-wire, transmit clock 2 - 512 T_{CYC})
  - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8 - 2048 T_{CYC})
  - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 - 512 T_{CYC})
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

(7) AD converter

- 8-bits × 8-channels

(8) PWM

- 2 channel synchronous variable 12 bit PWM

(9) USB Controller

- conforms to USB Specification, Version 1.1
- supports up to 5 user-configured endpoionts
  - USB Control endpoint 0
  - USB Interrupt & Bulk endpoint 1
  - USB Interrupt & Bulk endpoint 2
  - USB Isochronous & Interrupt & Bulk endpoint 3
  - USB Isochronous & Interrupt & Bulk endpoint 4

(10) Remote control receiver circuit (connected to P73/INT3/T0IN terminal)

- Noise rejection function (noise rejection filter time constant can selected from 1/32/128 T_{CYC})

(11) Watchdog timer

- The watchdog timer period set by external RC.
- Watchdog timer can be set to produce interrupt, system reset

(12) Interrupts

- 29-source, 10-vectored interrupts:
    1. Three level (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower level interrupt request is refused.
    2. If interrupt requests to two or more vector addresses occur at once, the higher level interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt signal
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/USB Bus active
4	0001BH	H or L	INT3/INT5/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/USB Bus reset
8	0003BH	H or L	SIO1/USB ERR/USB POV/USB SOF/USB ENP/USB NAK/USB STL
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/PWM0, 1/T4/T5

• Priority Level: X>H>L

• For equal priority levels, vector with lowest address takes precedence.

(13) Subroutine stack levels

- 1536 levels max. Stack is located in RAM

(14) Multiplication and division

- 16 bit × 8 bit (executed in 5 cycles)
- 24 bit × 16 bit (12 cycles)
- 16 bit ÷ 8 bit (8 cycles)
- 24 bit ÷ 16 bit (12 cycles)

(15) Oscillation circuits

- On-chip RC oscillation circuit used for system clock
- On-chip CF oscillation circuit used for system clock
- On-chip Crystal oscillation circuit used for system clock and time-base clock

(16) Standby function

- HALT mode

  HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate.

  1. Oscillation circuits are not stopped automatically
  2. Release on system reset

- HOLD mode

  HOLD mode is used to reduce the power dissipation. Both program execution and peripheral circuits are stopped.

  1. CF, RC and crystal oscillation circuits stop automatically
  2. Release occurs on any of the following conditions
     •input to the reset pin goes low
     •a specified level is input to at least one of INT0, INT1, INT2, INT4, INT5
     •an interrupt condition arises at port 0
     •USB BUS Active interrupt condition arises

- X'tal HOLD mode

  X'tal HOLD mode is used to reduce power consumption. Program execution is stopped. All peripheral circuits except the base timer are stopped.

  1. CF and RC oscillation circuits stop automatically
  2. Crystal oscillator is maintained in its state at HOLD mode inception.
  3. Release occurs on any of the following conditions
     - •input to the reset pin goes low
     - •a specified level is input to at least one of INT0, INT1, INT2, INT4, INT5
     - •an interrupt condition arises at port 0
     - •an interrupt condition arises at the base-timer
     - •USB BUS Active interrupt condition arises

(17) Factory shipment

- delivery form SQFP64, QIP64E

(18) Development Tools

- Evaluation chip : LC876095
- Emulator : EVA62S + ECB875664A (Evaluation chip board) + POD875664A (POD)
- Attachment board of EPROM programmer : W87F56256Q (For QIP64E package)
  W87F56256SQ (For SQFP64 package)

(19) How to Use of Attachment Board of EPROM Programmer

① Data

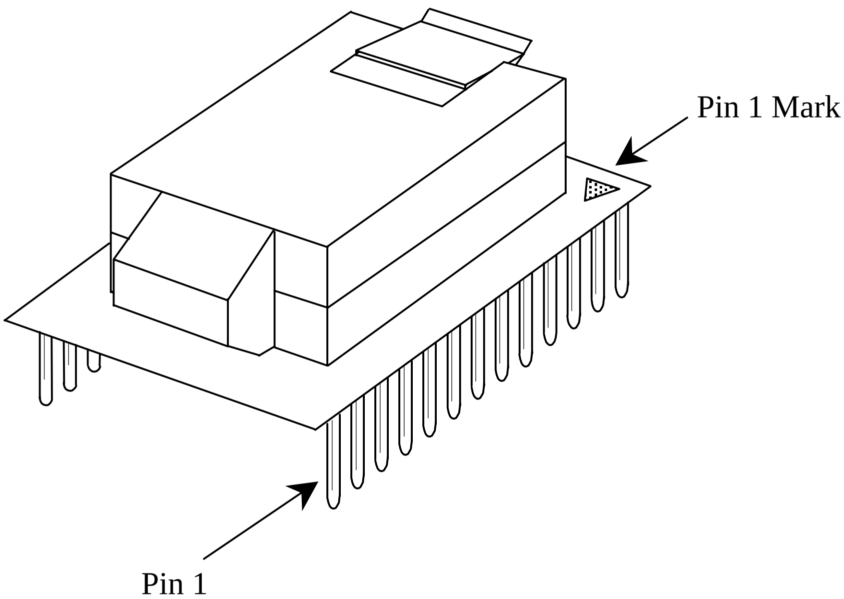
Programming data for the LC87F5664A's FLASH ROM is required.
The HEX file is used as the programming data for the LC87F5664A.

② How to program the FLASH ROM

The LC87F5664A can be programmed by an EPROM programmer with attachments W87F56256Q and W87F56256SQ.

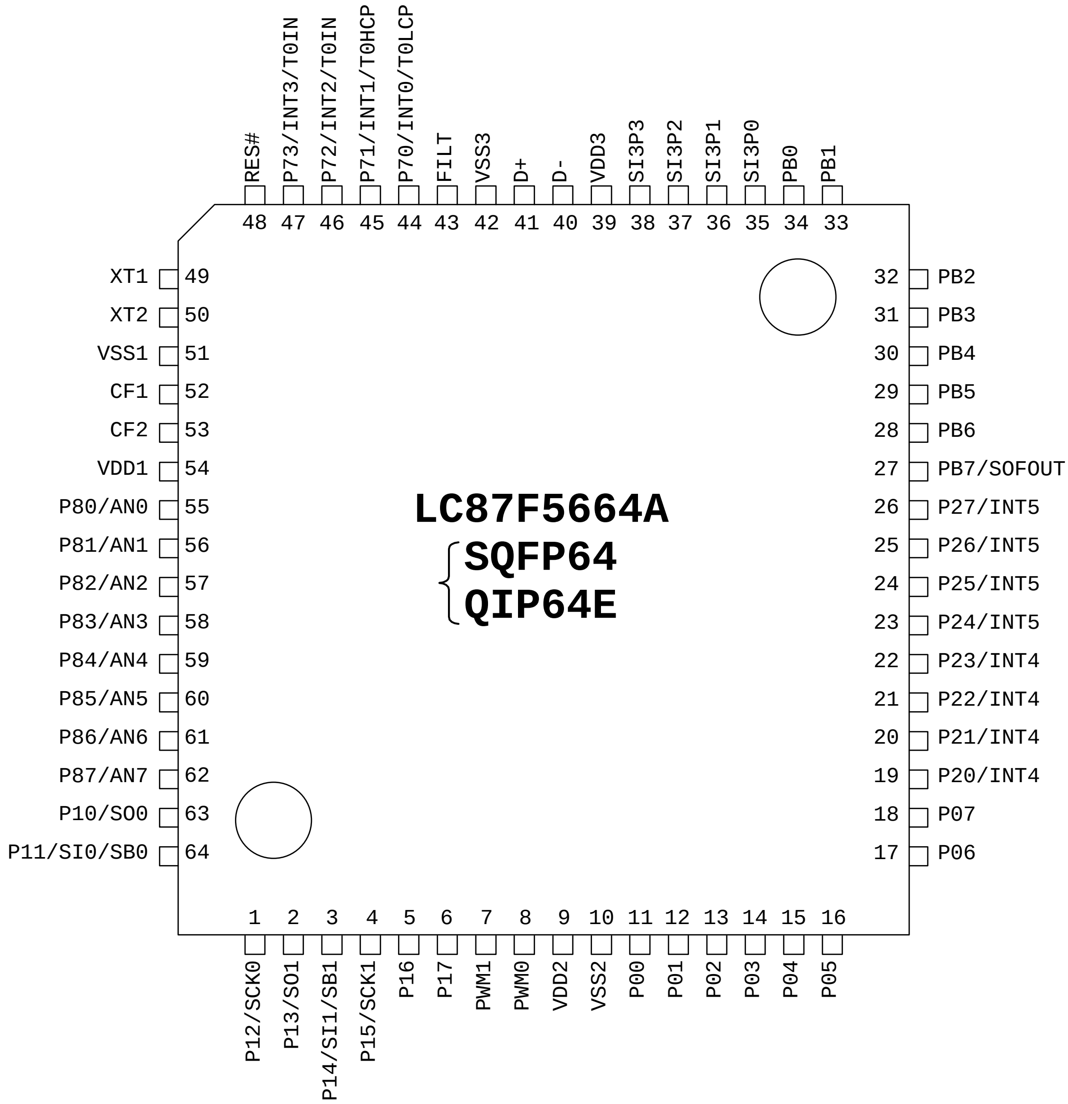
- Recommended EPROM programmer

Supplier	EPROM programmer	
Andou	AF-9706	Code "47100" (for SST 29EE512 mode)
Minato Electronics	MODEL 1890A	Code "D617" (for SST 29EE512 mode)



W87F56256Q

Pin Assignment

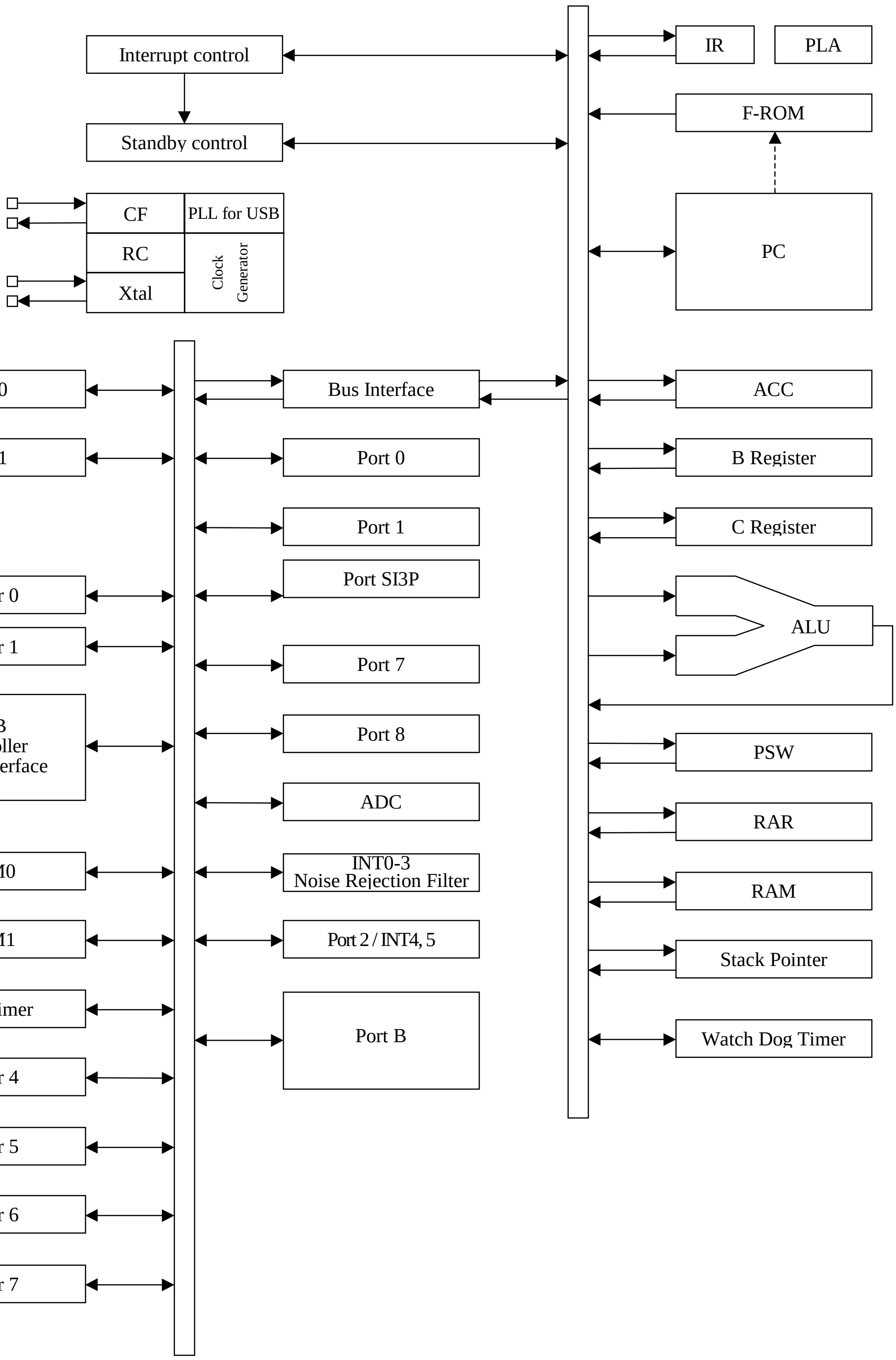


PIN assign table

QIP	NAME	SQFP
1	P12/SCK0	1
2	P13/SO1	2
3	P14/SI1/SB1	3
4	P15/SCK1	4
5	P16	5
6	P17	6
7	PWM1	7
8	PWM0	8
9	VDD2	9
10	VSS2	10
11	P00	11
12	P01	12
13	P02	13
14	P03	14
15	P04	15
16	P05	16
17	P06	17
18	P07	18
19	P20/INT4	19
20	P21/INT4	20
21	P22/INT4	21
22	P23/INT4	22
23	P24/INT5	23
24	P25/INT5	24
25	P26/INT5	25
26	P27/INT5	26
27	PB7/SOFOUT	27
28	PB6	28
29	PB5	29
30	PB4	30
31	PB3	31
32	PB2	32
33	PB1	33
34	PB0	34
35	SI3P0	35
36	SI3P1	36
37	SI3P2	37
38	SI3P3	38
39	VDD3	39
40	D-	40

QIP	NAME	SQFP
41	D+	41
42	VSS3	42
43	FILT	43
44	P70/INT0/T0LCP	44
45	P71/INT1/T0HCP	45
46	P72/INT2/T0IN	46
47	P73/INT3/T0IN	47
48	RES#	48
49	XT1	49
50	XT2	50
51	VSS1	51
52	CF1	52
53	CF2	53
54	VDD1	54
55	P80/AN0	55
56	P81/AN1	56
57	P82/AN2	57
58	P83/AN3	58
59	P84/AN4	59
60	P85/AN5	60
61	P86/AN6	61
62	P87/AN7	62
63	P10/SO0	63
64	P11/SI0/SB0	64

System Block Diagram



Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1, VSS2
VSS3</td><td>-</td><td>Power terminal (-)</td><td>No</td></tr>
<tr><td>VDD1, VDD2
VDD3</td><td>-</td><td>Power terminal (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 - P07</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable in nibble units
• Pull-up resistor provided/not provided (specified in nibble units)
• HOLD release input
• Port 0 interrupt input</td><td>Yes</td></tr>
<tr><td>Port 1
P10 - P17</td><td>I/O</td><td>•8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P10: SIO0 data output
P11: SIO0 data input, bus input/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input, bus input/output
P15: SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 - P27</td><td>I/O</td><td>• 8-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P20-P23: INT4 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input
P24-P27: NT5 input/HOLD release input/Timer 1 event input/Timer 0L capture input/Timer 0H capture input

• Interrupt detection style
<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
falling</th><th>H level</th><th>L level</th></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table></td><td>Yes</td></tr>
<tr><td>Port 7
P70 - P73</td><td>I/O</td><td>• 4-bit input/output port
• Data direction programmable for each bit individually
• Pull-up resistor provided/not provided (specified by bit)
• Other functions
P70: INT0 input/HOLD release input/Timer 0L capture input/Output for watchdog timer
P71: INT1 input/HOLD release input/Timer 0H capture input
P72: INT2 input/HOLD release input/Timer 0 event input/Timer0L capture input
P73: INT3 input with noise filter/Timer 0 event input/Timer 0H capture input

• Interrupt detection style
<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
falling</th><th>H level</th><th>L level</th></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table></td><td>No</td></tr>
</table>

(Continued)

Name	I/O	Function description	Option
Port 8 P80 - P87	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Other functions P80-P87 : AD converter input port	No
Port B PB0 - PB7	I/O	• 8-bit input/output port • Data direction programmable for each bit individually • Pull-up resistor provided/not provided (specified by bit) • Other functions PB7 : SOFOUT (START OF FRAME of USB) output	Yes
SI3 Port SI3P0 – SI3P3	I/O	• 4-bit input/output port • Data direction programmable for each bit individually	No
PWM0	O	PWM0 output port	No
PWM1	O	PWM1 output port	No
D -	I/O	USB data input/output D -	×
D +	I/O	USB data input/output D +	×
$\overline{\mathrm{RES}}$	I	Reset terminal	No
XT1	I	• Input terminal for 32.768kHz X'tal oscillation • Other function General input port When not in use, connect terminal to VDD1.	No
XT2	I/O	• Output terminal for 32.768kHz X'tal oscillation • Other function General input port When not in use, set as oscillation and leave terminal open	No
CF1	I	Input terminal for ceramic resonator	No
CF2	O	Output terminal for ceramic resonator	No

Port Output Configuration

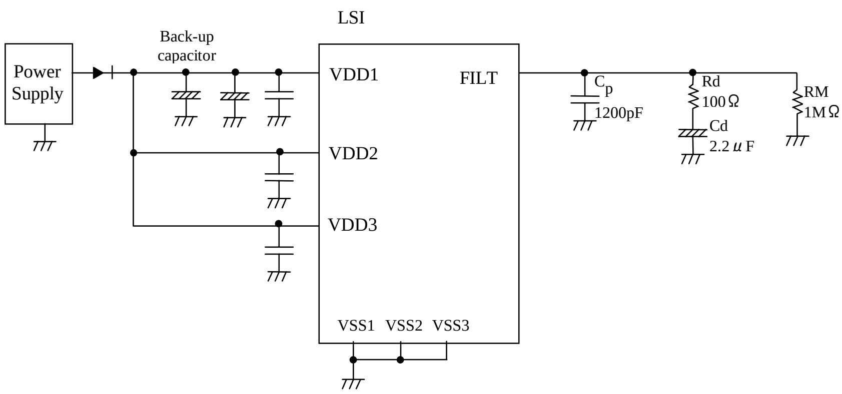
Output configuration and pull-up resistor options are shown in the following table.
Input is possible even when a port is in output mode.

Terminal	Option applies to:	Option	Output Format	Pull-up resistor
P00 - P07	each bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	None
P10 - P17 P20 - P27	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PB0 - PB7	each bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	None	Nch-open drain	Programmable
P71 - P73	-	None	CMOS	Programmable
P80 - P87	-	None	Nch-open drain	None
SI3P0, SI3P1 SI3P2, SI3P3	-	None	CMOS	None
			Nch-open drain	
PWM0, PWM1		None	CMOS	None
XT1	-	None	Input only	None
XT2	-	None	Output for 32.768kHz crystal oscillation	None

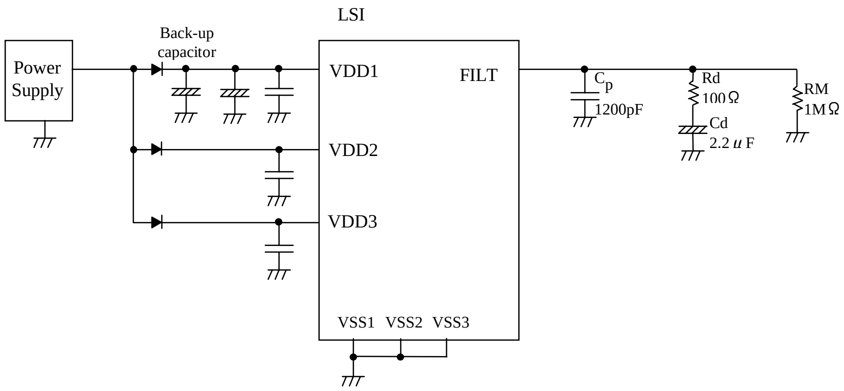
Note 1 Programmable pull-up resistor of Port 0 is specified in nibble units (P00 - P03, P04 - P07).

Note: To reduce VDD signal noise and to increase the duration of the backup battery supply, VSS1, VSS2, and VSS3 should connect to each other and they should also be grounded.

Example 1 : During backup in hold mode, port output 'H' level is supplied from the back-up capacitor.



Example 2 : During backup in hold mode, output is not held high and its value in unsettled.



1. Absolute maximum ratings / Ta=25°C, VSS1=VSS2=VSS3=0V

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[V]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD1, VDD2, VDD3	VDD1=VDD2 =VDD3		-0.3		+6.0	V
Input voltage		VI(1)	XT1, XT2, CF1			-0.3		VDD+0.3	
Output voltage		VO(1)	PWM0, PWM1			-0.3		VDD+0.3	
Input/Output voltage		VIO(1)	• Ports 0, 1, 2 • Ports 7, 8 • Port B • SI3P0-SI3P3 • PWM0, PWM1			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	• Ports 0, 1, 2 • Port B • SI3P0-SI3P3 • PWM0, PWM1	• CMOS output • For each pin.		-10			mA
		IOPH(2)	P71-P73	For each pin.		-5			
	Total output current	ΣIOAH(1)	P71-P73	Total of all pins		-5			
		ΣIOAH(2)	• Port 1 • PWM0, PWM1 • Port 3 • SI3P0-SI3P3	Total of all pins		-30			
		ΣIOAH(3)	Ports 0, 2	Total of all pins		-20			
		ΣIOAH(4)	Port B	Total of all pins		-20			
Low level output current	Peak output current	IOPL(1)	• P02-P07 • Ports 1, 2 • Port B • SI3P0-SI3P3 • PWM0, PWM1	For each pin.				20	
		IOPL(2)	P00, P01	For each pin.				30	
		IOPL(3)	Ports 7, 8	For each pin.				5	
	Total output current	ΣIOAL(1)	Port 7	Total of all pins				15	
		ΣIOAL(2)	Port 8	Total of all pins				15	
		ΣIOAL(3)	• Port 1 • PWM0, PWM1	Total of all pins				80	
		ΣIOAL(4)	Ports 0, 2 Port B • SI3P0-SI3P3	Total of all pins				80	
Maximum power consumption		Pdmax	QIP64E SQFP64	Ta= -20 to +70°C					mW
Operating temperature range		Topg				-20		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended operating range / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2 =VDD3	0.242μs ≤ tCYC ≤ 200μs		4.5		5.5	V
			0.242μs ≤ tCYC ≤ 200μs Except for on-board rewriting		3.0		5.5	
			0.365μs ≤ tCYC ≤ 200μs Except for on-board rewriting		2.7		5.5	
HOLD voltage	VHD	VDD1=VDD2 =VDD3	RAM and register data are kept in HOLD mode.		2.0		5.5	
Input high voltage	VIH(1)	• Ports 1, 2 • SI3P0 - 3 • P71-P73 • P70 port input /interrupt		2.7 - 5.5	0.3VDD +0.7		VDD	
	VIH(2)	• Ports 0, 8 • Port B		2.7 - 5.5	0.3VDD +0.7		VDD	
	VIH(3)	Port 70 Watchdog timer		2.7 - 5.5	0.9VDD		VDD	
	VIH(4)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.7 - 5.5	0.75VDD		VDD	
Input low voltage	VIL(1)	• Ports 1, 2 • SI3P0 - 3 • P71-P73 • P70 port input /interrupt		2.7 - 5.5	VSS		0.1VDD +0.4	
	VIL(2)	• Ports 0, 8 • Port B		2.7 - 5.5	VSS		0.15VDD +0.4	
	VIL(5)	Port 70 Watchdog timer		2.7 - 5.5	VSS		0.8VDD -1.0	
	VIL(6)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.7 - 5.5	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 - 5.5	0.242		200	μs
			Except for on-board rewriting	3.0 - 5.5	0.242		200	
			Except for on-board rewriting	2.7 - 5.5	0.365		200	
External system clock frequency	FEXCF(1)	CF1	• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	2.7 - 5.5	0.1		12	MHz
			• Leave CF2 pin open • System clock divider set to 1/1 • External clock DUTY=50±5%	2.7 - 5.5	0.1		6	

(Note 1) The oscillation parameters are shown on Tables 1 and 2.
(Note 2) VDD∞4.5V is required for on-board flash ROM rewriting.

3. Electrical characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Input high current	IIH(1)	• Ports 0, 1, 2 • Ports 7, 8 • Port B • SI3P0-SI3P3 • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • VIN=VDD (including the off-leak current of the output Tr.)	2.7 - 5.5			1	μA
	IIH(2)	XT1, XT2	• Using as an input port • VIN=VDD	2.7 - 5.5			1	
	IIH(3)	CF1	VIN=VDD	2.7 - 5.5			15	
Input low current	IIL(1)	• Ports 0, 1, 2 • Ports 7, 8 • Port B • SI3P0-SI3P3 • $\overline{\text{RES}}$ • PWM0, PWM1	• Output disable • Pull-up resistor OFF • VIN=VSS (including the off-leak current of the output Tr.)	2.7 - 5.5	-1			
	IIL(2)	XT1, XT2	• Using as an input port • VIN=VSS	2.7 - 5.5	-1			
	IIL(3)	CF1	VIN=VSS	2.7 - 5.5	-15			
Output high voltage	VOH(1)	• Ports 0, 1, 2 • Port B • SI3P0-SI3P3 • PWM0, PWM1	IOH=-1.0mA	4.5 - 5.5	VDD-1			V
	VOH(2)		IOH=-0.1mA	2.7 - 5.5	VDD-0.5			
	VOH(3)	Port 71, 72, 73	IOH=-0.4mA	4.5 - 5.5	VDD-1			
Output low voltage	VOL(1)	• Ports 0, 1, 2 • Port B • SI3P0-SI3P3 • PWM0, PWM1	IOL=10mA	4.5 - 5.5			1.5	V
	VOL(2)		IOL=1.6mA	4.5 - 5.5			0.4	
	VOL(3)		IOL=1mA	2.7 - 5.5			0.4	
	VOL(4)	P00, P01	IOL=30mA	4.5 - 5.5			1.5	
	VOL(5)	Ports 7, 8	IOL=1mA	2.7 - 5.5			0.4	
Pull-up resistor	Rpu	• Ports 0, 1, 2 • Port 7 • Port B	VOH=0.9VDD	2.7 - 5.5	15	40	70	kΩ
Hysteresis voltage	VHIS	• $\overline{\text{RES}}$ • Port 1 • Port 2 • Port 7 • SI3P0-SI3P3		2.7 - 5.5		0.1VDD		V
Pin capacitance	CP	All pins	• All pins except the measured terminal : VIN=VSS • f=1MHz • Ta=25°C	2.7 - 5.5		10		pF

4. Serial input/output characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tSCK(1)	SCK0(P12)	Refer to figure 6	2.7 - 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
			tSCKLA(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)				3(SIO0) 5(SIO2)			
		Cycle	tSCK(2)	SCK1(P15)	Refer to figure 6	2.7 - 5.5	2			
		Low level pulse width	tSCKL(2)				1			
		High level pulse width	tSCKH(2)				1			
	Output clock	Cycle	tSCK(3)	SCK0(P12)	• CMOS output • Refer to figure 6	2.7 - 5.5	4/3			
		Low level pulse width	tSCKL(3)					1/2		tSCK
			tSCKLA(2)		SCK0(P12) SIO0			3/4		
		High level pulse width	tSCKH(3)					1/2		
			tSCKHA(2)		SCK0(P12) SIO0			2		
		Cycle	tSCK(4)	SCK1(P15)	• CMOS output • Refer to figure 6	2.7 - 5.5	2			tCYC
		Low level pulse width	tSCKL(4)					1/2		tSCK
		High level pulse width	tSCKH(4)					1/2		
Serial input		Data set-up time	tsDI	SB0(P11), SB1(P14), SI0, SI1	• Data set-up to SI0CLK • Data hold from SI0CLK • Refer to figure 6	2.7 - 5.5	0.03			µs
		Data hold time	thDI				0.03			
Serial output		Output delay time	tdD0	SO0(P10), SO1(P13), SB0(O11), SB1(P14)	• Data hold from SI0CLK • Time delay from SI0CLK trailing edge to the SO data change in the open drain • Refer to figure 6	2.7 - 5.5			1/3tCYC +0.05	

5. Pulse input conditions / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72) INT4(P20-P23) INT5(P24-P27)	• Interrupt acceptable • Timer 0 and 1 event input acceptable	2.7 - 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (The noise rejection clock is selected to 1/1.)	• Interrupt acceptable • Timer 0 event input acceptable	2.7 - 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) (The noise rejection clock is selected to 1/32.)	• Interrupt acceptable • Timer 0 event input acceptable	2.7 - 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) (The noise rejection clock is selected to 1/128.)	• Interrupt acceptable • Timer 0 event input acceptable	2.7 - 5.5	256			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.7 - 5.5	200			µs

6. AD converter characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[V]	min.	typ.	max.	unit
Resolution	N	AN0(P80) - AN7(P87) AN9(P71)		3.0 - 5.5		8		bit
Absolute precision	ET		(Note 2)	3.0 - 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time=32 × tCYC (ADCR2=0) (Note 3)	3.0 - 5.5	15.10 (tCYC= 0.588μs)		97.92 (tCYC= 3.06μs)	μs
			AD conversion time=64 × tCYC (ADCR2=1) (Note 3)	3.0 - 5.5	15.10 (tCYC= 0.294μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 - 5.5	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	3.0 - 5.5			1	μA
	IAINL		VAIN=VSS	3.0 - 5.5	-1			

(Note 2) Absolute precision excludes the quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from executing the AD conversion instruction to setting the complete digital conversion value in the register.

7. Current dissipation characteristics / Ta=-20°C to +70°C, VSS1=VSS2=VSS3=0V

<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2">Pins</th><th rowspan="2">Conditions</th><th rowspan="2">VDD[V]</th><th colspan="4">Limits</th></tr>
<tr><th>min.</th><th>typ.</th><th>max.</th><th>unit</th></tr>
<tr><td rowspan="8">Current drain during basic operation
(Note 4)</td><td>IDDOP(1)</td><td rowspan="8">VDD1
=VDD2
=VDD3</td><td>• FmCF=12MHz by ceramic resonator
• FmX’tal=32.768kHz by crystal oscillation
• System clock : CF oscillation (10MHz)
• Internal RC oscillation stops
• 1/1 divided</td><td>3.0 - 5.5</td><td></td><td>23</td><td>39</td><td rowspan="6">mA</td></tr>
<tr><td>IDDOP(2)</td><td>• CF1=8MHz by external clock
• FmX’tal=32.768kHz by crystal oscillation
• System clock : CF1 oscillation (20MHz)
• Internal RC oscillation stops
• 1/2 divided</td><td>2.7 - 5.5</td><td></td><td>21</td><td>37</td></tr>
<tr><td>IDDOP(3)</td><td rowspan="2">• FmCF=6MHz by ceramic resonator
• FmX'tal=32.768kHz by crystal oscillation
• System clock : CF oscillation (5MHz)
• Internal RC oscillation stops</td><td>2.7 - 5.5</td><td></td><td>9</td><td>15</td></tr>
<tr><td>IDDOP(4)</td><td>2.7 - 4.5</td><td></td><td>6</td><td>11</td></tr>
<tr><td>IDDOP(5)</td><td rowspan="2">• FmCF=0Hz (when oscillation stops)
• FmX'tal=32.768kHz by crystal oscillation
• System clock : RC oscillation</td><td>4.5 - 5.5</td><td></td><td>3</td><td>6</td></tr>
<tr><td>IDDOP(6)</td><td>2.7 - 4.5</td><td></td><td>1.8</td><td>4</td></tr>
<tr><td>IDDOP(7)</td><td rowspan="2">• FmCF=0Hz (when oscillation stops)
• FmX'al=32.768kHz by crystal oscillation
• System clock : X'tal oscillation (32.768kHz)
• Internal RC oscillation stops</td><td>4.5 - 6.0</td><td></td><td>150</td><td>200</td><td>µA</td></tr>
<tr><td>IDDOP(8)</td><td>2.7 - 4.5</td><td></td><td>90</td><td>130</td><td>µA</td></tr>
<tr><td rowspan="2">Current drain in HALT mode
(Note 4)</td><td>IDDHALT(1)</td><td rowspan="2">VDD1
=VDD2
=VDD3</td><td>• HALT mode
• FmCF=12MHz by ceramic resonator
• FmX’tal=32.768kHz by crystal oscillation
• System clock : CF oscillation (10MHz)
• Internal RC oscillation stops
• 1/1 divided</td><td>3.0 - 5.5</td><td></td><td>13</td><td>19</td><td rowspan="2">mA</td></tr>
<tr><td>IDDHALT(2)</td><td>• HALT mode
• CF1=8MHz by external clock
• FmX’tal=32.768kHz by crystal oscillation
• System clock : CF1 oscillation (20MHz)
• Internal RC oscillation stops
• 1/2 divided</td><td>2.7 - 5.5</td><td></td><td>11</td><td>18</td></tr>
</table>

(Continued)

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Current drain in HALT mode (Note 4)	IDDHALT(3)	VDD1 =VDD2 =VDD3	• HALT mode • FmCF=6MHz by ceramic resonator • FmX'tal=32.768kHz by crystal oscillation • System clock : CF oscillation (5MHz) • Internal RC oscillation stops	4.5 - 5.5		5	10	mA
	IDDHALT(4)			2.7 - 4.5		1.2	3.2	
	IDDHALT(5)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : RC oscillation	4.5 - 5.5		1	1.5	
	IDDHALT(6)			2.7 - 4.5		0.4	1	
	IDDHALT(7)		• HALT mode • FmCF=0Hz (when oscillation stops) • FmX'tal=32.768kHz by crystal oscillation • System clock : X'tal oscillation (32.768kHz) • Internal RC oscillation stops	4.5 - 5.5		80	150	µA
	IDDHALT(8)			2.7 - 4.5		16	72	µA
Current drain during HOLD mode	IDDHOLD(1)	VDD1	• HOLD mode • CF1=VDD or leave it open (when using external clock)	2.7 - 5.5		0.01	25	µA
Current drain during time-base clock HOLD mode	IDDHOLD(2)	VDD1	• Time-base clock HOLD mode • CF1=VDD or leave it open (when using external clock) • FmX'tal=32.768kHz by crystal oscillation	2.7 - 5.5		35	100	µA

(Note 4) The current of the output transistors and pull-up MOS transistors are excluded.

8. USB characteristics, timing/ Ta=-20 to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Limits min.	typ.	max.	unit
Output High Level	$V_{OH(USB)}$		• With 15kΩ±5% to Gnd		2.8		3.6	V
Output Low Level	V_{OL}		• With 1.5kΩ±5% to 3.6V				0.3	V
Output Signal Crossover Voltage	V_{CRS}				1.3		2.0	V
Differential Input Sensitivity	V_{DI}		• |(D+)-(D-)|		0.2			V
Differential Input Common Mode Range	V_{CM}				0.8		2.5	V
Input High Level	$V_{IH(USB)}$				2.0			V
Input Low Level	$V_{IL(USB)}$						0.8	V
Input Capacitance	C_{IN}		• OV<(D+, D-)<3.3V, Hi-Z State				20	pF
Input Leakage	I_{LO}		• 15kΩ±5%		-10		10	µA
External Bus Pull-down Resistance	R_{PD}				14.25		15.75	kΩ
USB Data Transition Rise Time	t_R				4		20	ns
USB Data Transition Fall Time	t_F				4		20	ns
Rise/ Fall Time Matching	t_{RFM}		• t_R / t_F		90		110	%

(Continued)

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
Full Speed Data Rate	t_{DRATE}		• Ave. Bit		11.97	12	12.03	Mb/s
Receiver Data Jitter Tolerance	t_{DJR1}		• To Next Transition		-3.5		3.5	ns
Receiver Data Jitter Tolerance	t_{DJR2}		• For Paired Transition		-4		4	ns
Differential to EOP Transition Skew	t_{DEOP}				-2		5	ns
EOP Width at Receiver	t_{EOPR1}		• Rejects as EOP					ns
EOP Width at Receiver	t_{EOPR2}		• Accepts as EOP					ns
Source EOP Width	t_{EOPT}				160	167	175	ns
Differential Driver Jitter	t_{UDJ1}		• To Next Transition		-2		2	ns
Differential Driver Jitter	t_{UDJ2}		• To Paired Transition		-130		130	ns

9. Power On Reset/ Ta=-20 to +70°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
V_{DD} Slew	t_{VDD}		Linear Ramp on V_{DD} Pin to V_{DD}		0.010		1000	ms

10. F-ROM Write Characteristics / Ta=+10°C to +55°C, VSS1=VSS2=VSS3=0V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[V]	min.	typ.	max.	unit
On-board writing current	IDDFW(1)	VDD1	• 128-byte writing • including erase time current	4.5 - 5.5		30	65	mA
Writing time	tFW(1)		• 128-byte writing • including data erase time • Excluding time to fetch 128 byte data	4.5 - 5.5		4.2	7.0	mS

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions:
1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 1. Recommended circuit parameters for the main system clock using the ceramic resonator

Frequency	Manufacturer	Oscillator	Recommended circuit parameters			Operating supply voltage range	Oscillation stabilizing time		Note
			C1	C2	Rd1		typ	max	
12MHz	MURATA	~~CSA12.0MTZ~~	33pF	33pF	0Ω	3.0 – 5.5V	0.05ms	0.50ms	
		~~CST12.0MTW~~	(30pF)	(30pF)	0Ω	3.0 – 5.5V	0.05ms	0.50ms	Internal C1,C2
	KYOCERA	~~KBR-12.0M~~	33pF	33pF	0Ω	3.0 – 5.5V	0.05ms	0.50ms	
5MHz	MURATA	~~CSA6.00MG~~	33pF	33pF	0Ω	2.7 – 5.5V	0.05ms	0.50ms	
		~~CST6.00MGW~~	(30pF)	(30pF)	0Ω	2.7 – 5.5V	0.05ms	0.50ms	Internal C1,C2
	KYOCERA	~~KBR-6.0MSA~~	33pF	33pF	0Ω	2.7 – 5.5V	0.05ms	0.50ms	

*The oscillation stabilizing time is a period until the oscillation becomes stable after VDD becomes higher than minimum operating voltage. (Refer to Figure4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table bellow is based on the following conditions:
1. Using the standard oscillation evaluation board SANYO has provided.
2. Using the external peripheral parts with the indicated value.
3. The recommended circuit parameters for the peripheral parts are verified by the oscillator manufacturer.

Table 2. Recommended circuit parameters for the subsystem clock using the crystal oscillation

Frequency	Manufacturer	Oscillator	Recommended circuit Parameters				Operating supply voltage range	Oscillation stabilizing time		Note
			C3	C4	Rf	Rd2		typ	max	
32.768kHz	SEIKO EPSON	~~C-002Rx~~	12pF	15pF	OPEN	300kΩ	2.7 - 6.0V			

*The oscillation stabilizing time is the period until the oscillation becomes stable, after executing the instruction which starts the sub-clock oscillator or after releasing a HOLD mode. (Refer to Figure4)

(Notes) Since the oscillation frequency precision is affected by the circuit pattern, place the oscillation related parts as close to the oscillation pins as possible, using the shortest possible pattern length.

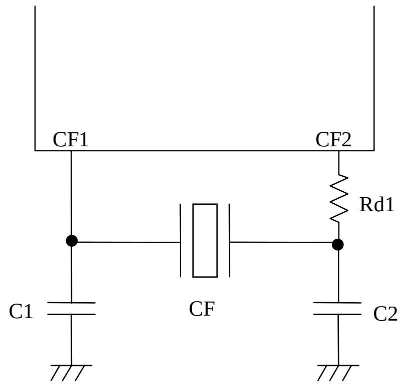


Figure 1 Ceramic oscillation circuit

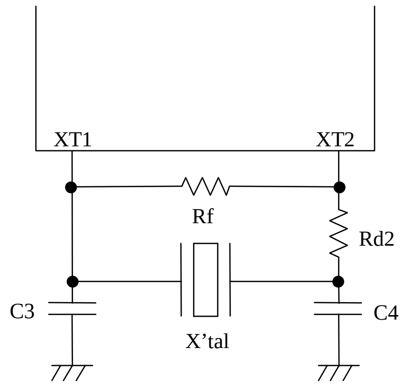


Figure 2 Crystal oscillation circuit

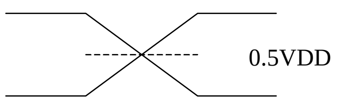
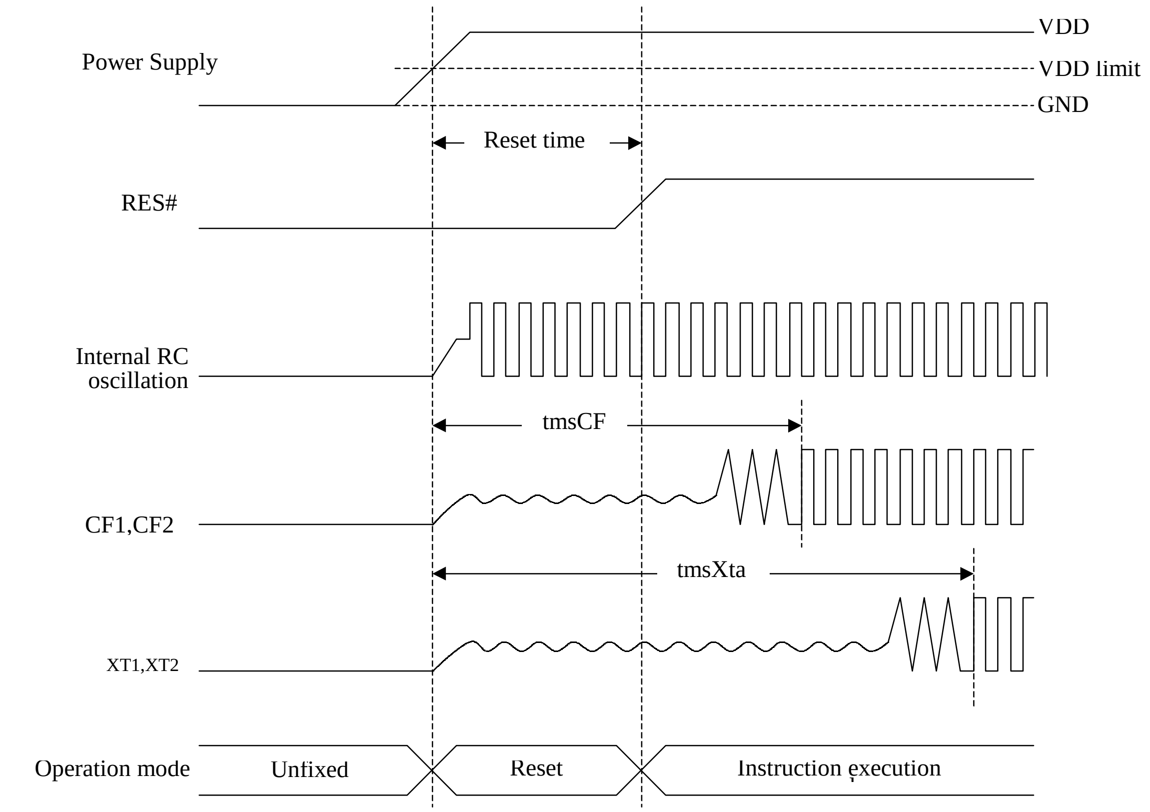
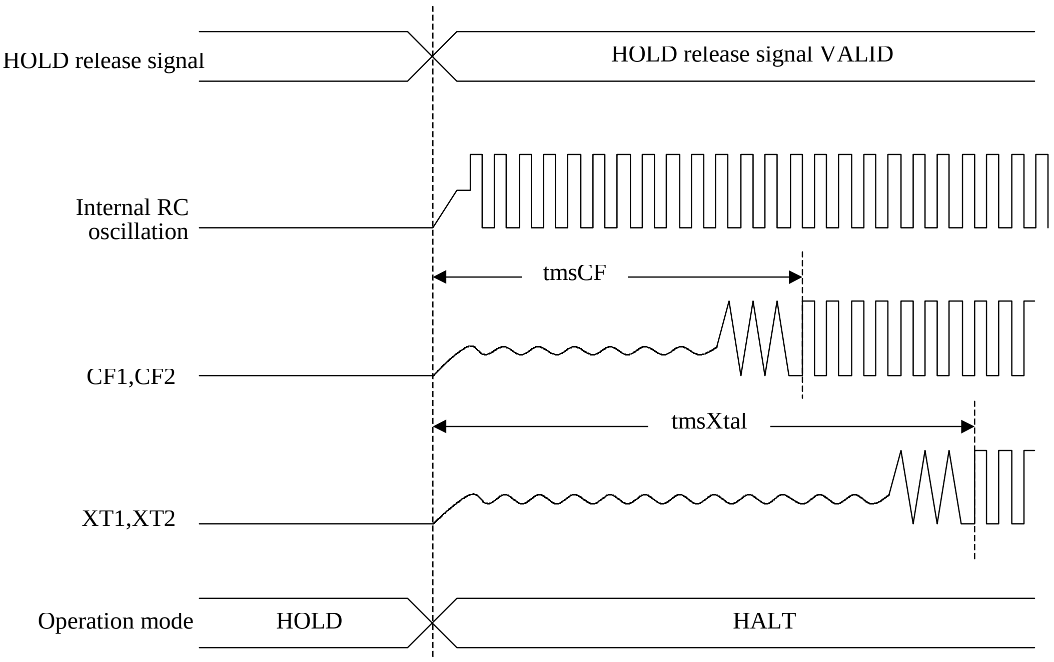


Figure 3 AC timing point

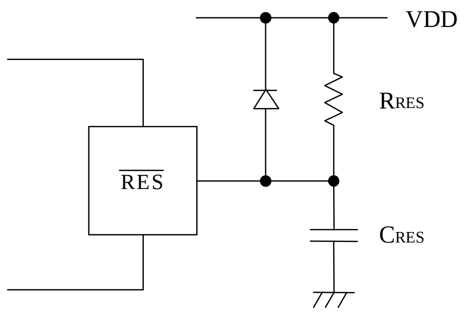


Reset time and oscillation stabilizing time



HOLD release signal and oscillation stabilizing time

Figure 4 Oscillation stabilizing time



(Note) Select CRES and RRES value to assure that at least 200µs reset time is generated after the VDD becomes higher than the minimum operating voltage.

Figure 5 Reset circuit

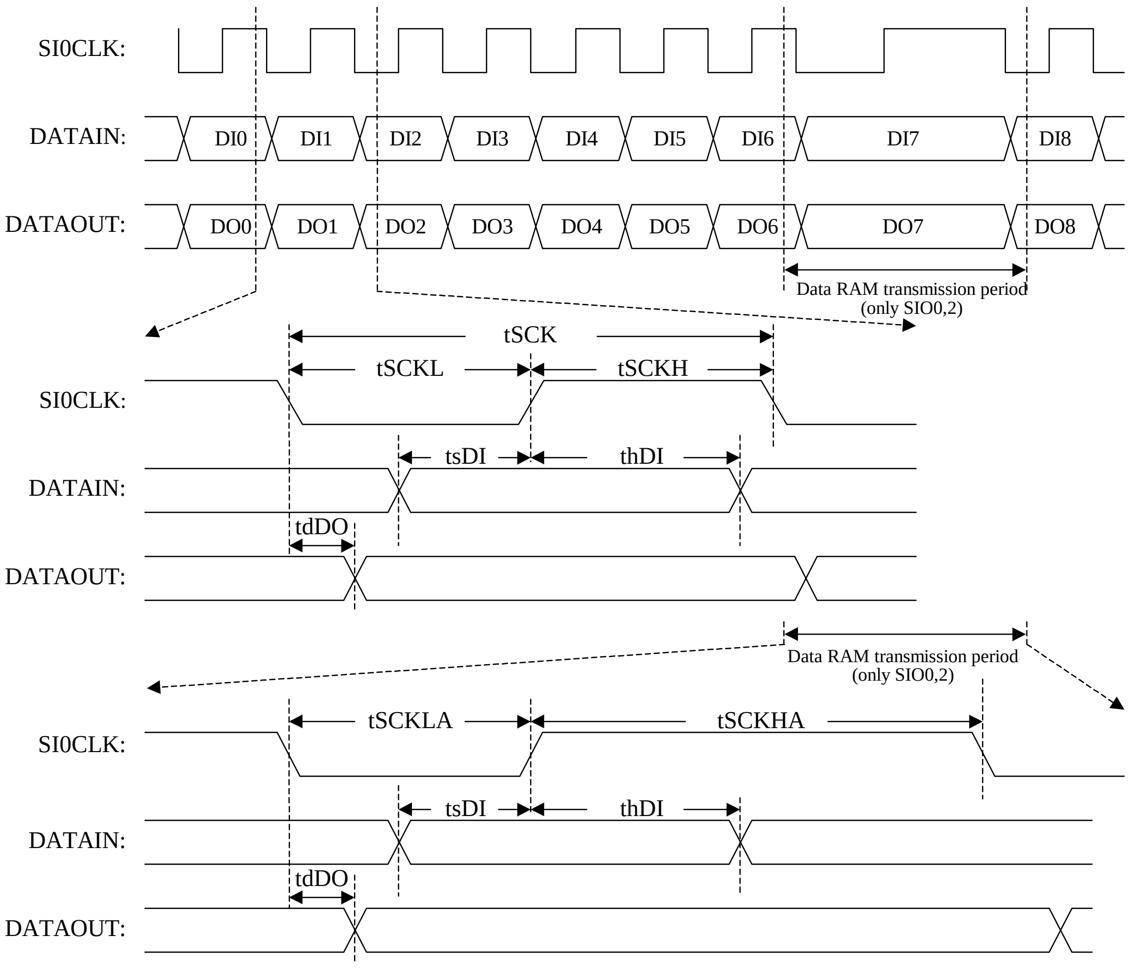


Figure 6 Serial input/output test condition

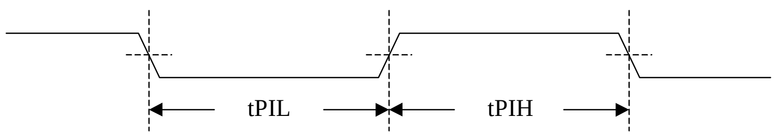


Figure 7 Pulse input timing condition

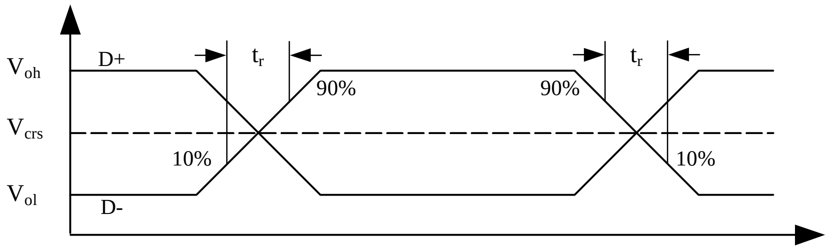


Figure 8 USB Data Signal Timing and Voltage Levels

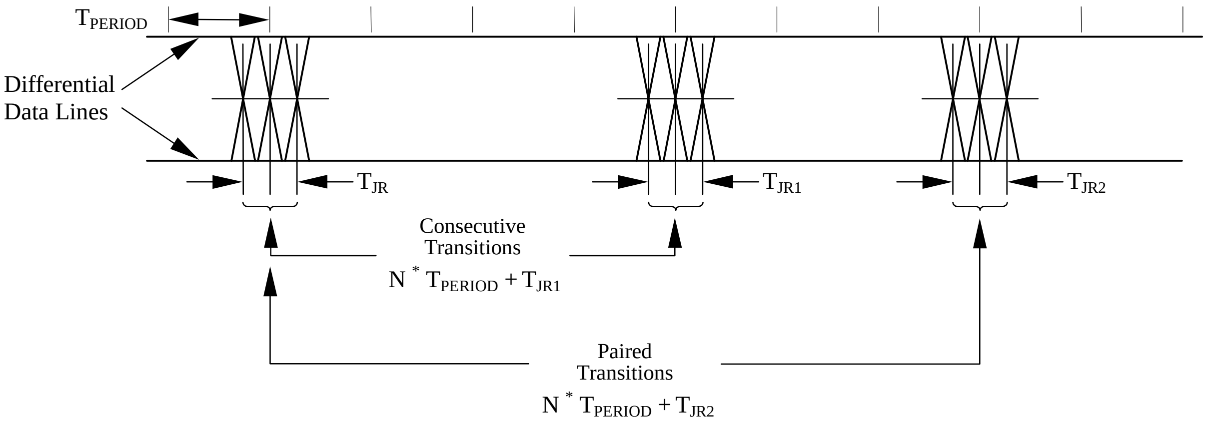


Figure 9 Receiver Jitter Tolerance

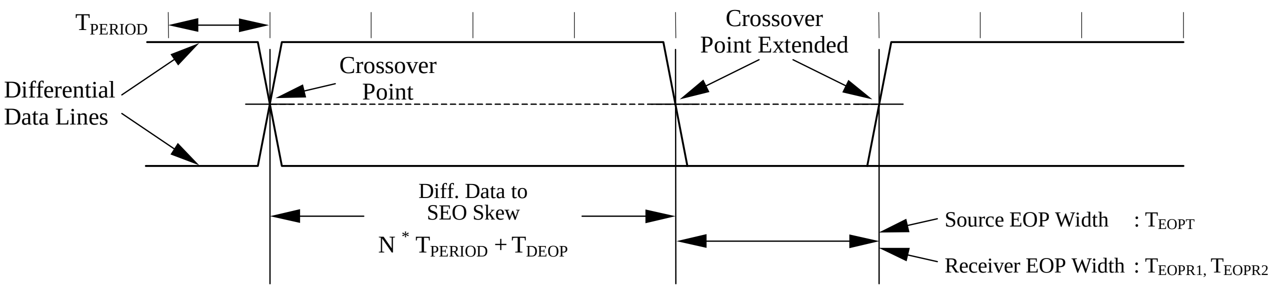


Figure 10 Differential to EOP Transition Skew and EOP Width

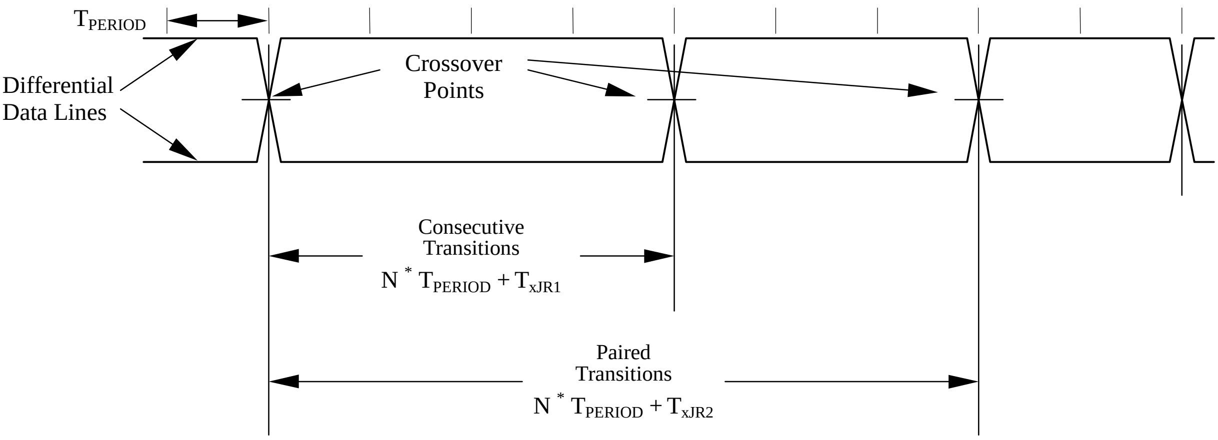


Figure 11   Differential Data Jitter

memo: