High Frequency Step Down Regulator

PRELIMINARY DATA SHEET

DESCRIPTION

The LX1910 is a voltage mode PWM buck regulator operating at high frequencies capable of achieving high efficiency over a broad range of operating load conditions.

The LX1910 implements a load-detection architecture and enters a power-saving PFM mode when driving small load currents ensuring optimal regulator efficiency over the entire output current range thus maximizing battery life.

The PWM operating mode implements typical fixed frequency operation of 1MHz in order to minimize the size of external components.

The transconductance error amplifier has 15uA of drive with an output voltage swing rail-to-rail, and compensation is external in order to maximize user flexibility in the selection of output inductance and capacitance.

With a minimum duty cycle of 0%, the LX1910 does not require a minimum load current for stable operation.

The input voltage range includes 2.7V to 6V and the regulator will provide up to 700mA of output current to the load.

Asserting the $\overline{SHDN}$ pin places the device in a sleep-mode drawing less than 1µA of quiescent current.

The LX1910 comes in the MSOP package allowing a complete application circuit to occupy a very small PCB area.

These features make the LX1910 ideal for use in SmartPhones, PDAs, or other battery-operated devices

KEY FEATURES

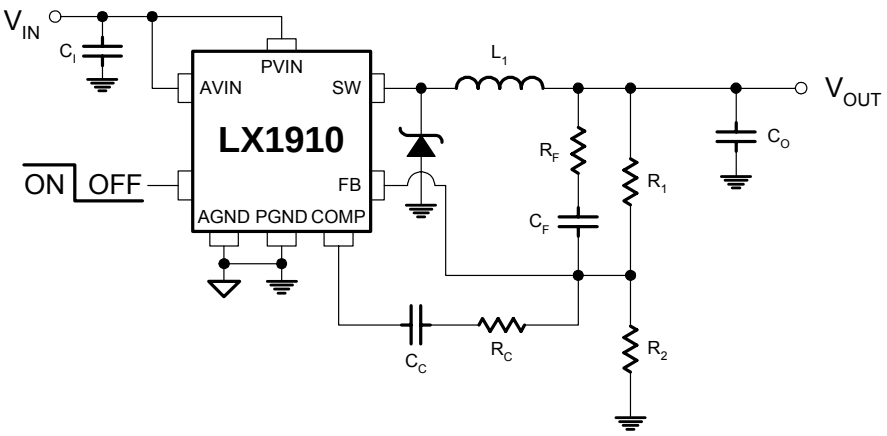
- 2.7V to 6.0V Input Range
- PWM/PFM Operation For Light Load Efficiency
- Adj. Output From 1.17V to V_{IN}
- Capable Of Supplying More Than 700mA
- Quiescent Current of 250µA
- 1MHz Operation Frequency
- 8-Pin MSOP

APPLICATIONS

- Portable Microprocessor Core Voltage Supplies
- LiIon Battery Voltage Conversion
- 5V to 3.3V
- 3.3V to 1.8V

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)	DU Plastic MSOP 8-Pin
-40 to 85	LX1910-CDU

Note: Available in Tape & Reel.
Append the letter "T" to the part number.
(i.e. LX1910-CDUT)

Rev. 0.9, 2003-09-12

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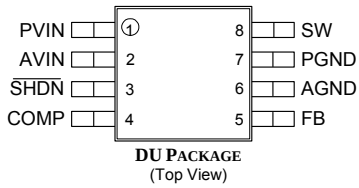
LX1910

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage (IN) ..... -0.3V to 7V
FB Input Voltage ..... -0.3V to 2V
SW Voltage ..... -0.3V to (V_{IN} + 0.3V)
SW Peak Current (Internally Limited) 1A
$\overline{SHDN}$ Input Voltage ..... -0.3V to 7V
Operating Temperature Range ..... -40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 40 seconds) ..... 250°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.
x denotes respective pin designator 1, 2, or 3

PACKAGE PIN OUT



DU PACKAGE
(Top View)

THERMAL DATA

DU Plastic MSOP 8-Pin

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	206°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

Name	Description
SW	Switch Node Connection – Connects to the internal P-Channel MOSFET drain.
AGND	Analog Circuit Ground – Common ground reference for IC operation.
PGND	Power Ground Return – Return for the internal P-Channel MOSFET gate driver.
FB	Feedback Error Amplifier Input – Connect to the output voltage through a resistor divider.
PVIN	MOSFET Source Supply – Connected to the internal P-Channel MOSFET Source. Connect to an unregulated supply voltage.
AVIN	IC Input Voltage Supply – Supplies power to the regulator circuitry. Connect to an unregulated supply voltage with adequate decoupling.
COMP	Error Amplifier Output – Loop compensation is effected by placing a series resistor/capacitor combination between the COMP pin and AGND.
$\overline{SHDN}$	Enable Signal Input – Active low signal which places the IC in a shutdown mode, reducing quiescent current to less than 1μA. In shutdown mode, pin 8 (SW) becomes high impedance.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $0°C \leq T_A \leq 70°C$ except where otherwise noted and the following test conditions: $V_{IN} = 3.6V$. Typical values are at $T_A = 25°C$

Parameter	Symbol	Test Conditions	LX1910			Units
			Min	Typ	Max	
ENTIRE REGULATOR						
Input Voltage	V_{IN}		2.7		6.0	V
Output Voltage Range	V_{OUT}	V_{IN} = 5V	V_{FBT}		4	V
Feedback Threshold	V_{FBT}		1.146	1.170	1.193	V
Quiescent Current	I_Q	$V_{FB} = V_{FBT}$ + 125mV (Pin 2 Supply Current)		250	400	µA
		$V_{\overline{SHDN}}$ = GND			1	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$		-100		100	nA
$\overline{SHDN}$ Voltage Threshold	$V_{\overline{SHDN}}$	(Device Off)			$0.2 \cdot V_{IN}$	V
		(Device On)	$0.8 \cdot V_{IN}$			
Oscillator Frequency	f_{OSC}		0.6	1.07	1.325	MHz
		V_{IN} = 5V	0.8	1.07	1.325	
Oscillator Ramp Voltage	V_{OSC}			3.3		V
Load Regulation	$\Delta V_{OUT}(I_{OUT})$			0.5		%
Line Regulation	$\Delta V_{FBT}(V_{IN})$			0.04	0.4	%
Thermal Shutdown	$T_{\overline{SHDN}}$		125	150		°C
ERROR AMPLIFIER						
Error Amplifier Gain	g_m			300		µA/V
FB Input Bias Current	I_{FB}	V_{FB} = 1.2V		300	550	nA
Error Amplifier Output Drive Current	I_{COMP}	$V_{FB} = V_{FBT}$ + 125mV	10	13		µA
		$V_{FB} = V_{FBT}$ - 125mV	-8.75	-13		
Error Amplifier Output Voltage	V_{COMP}	I_{COMP} = -10µA		95		mV
		I_{COMP} = 10µA, V_{IN} = 5V		4.86		V
POWER P-CHANNEL MOSFET						
On Resistance	$R_{DS(ON)}$	I_{SW} = 0.5A, T_A = 25°C, V_{IN} = 5V		0.4	0.5	Ω
SW Pin Leakage Current	$I_{SW(LEAK)}$	T_A = 25°C		0.01	1	µA
Maximum Duty Cycle	DC	I_{SW} = 0.5A			80	%
Current Limit	$I_{SW(MAX)}$		800	925		mA

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SIMPLIFIED BLOCK DIAGRAM

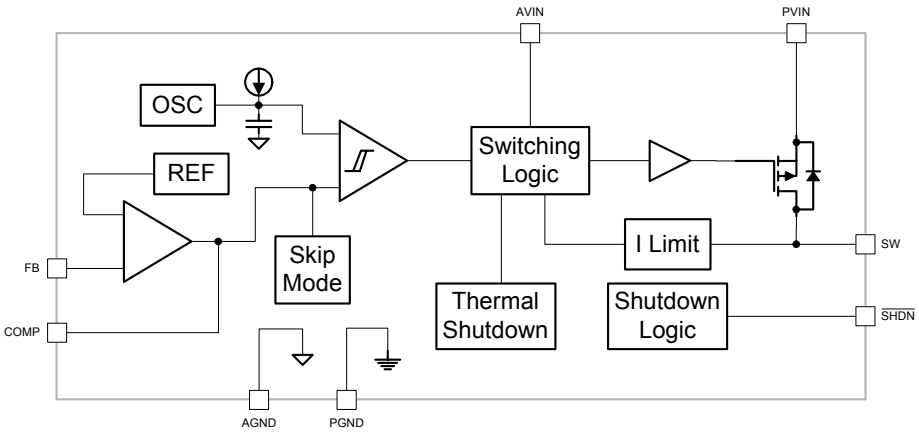

Figure 1– Simplified Block Diagram

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APPLICATION CIRCUITS

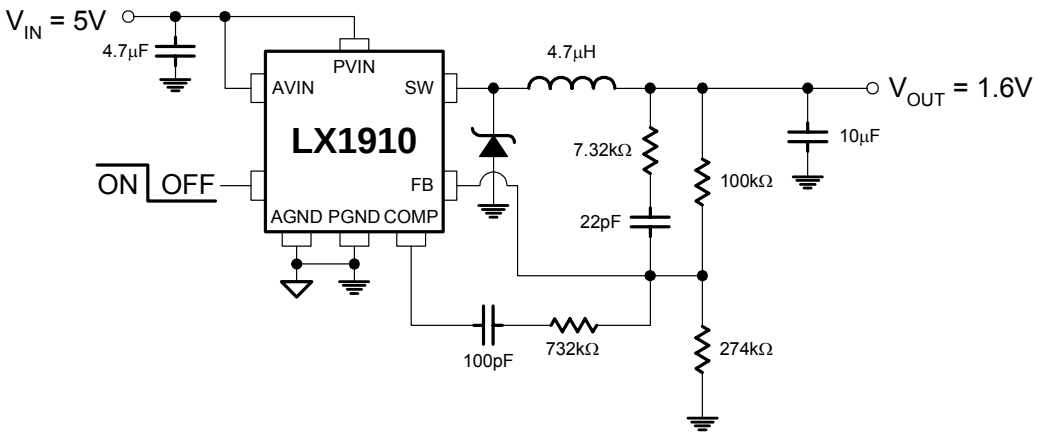

Figure 2 – Typical Application For A 1.6V Output Voltage

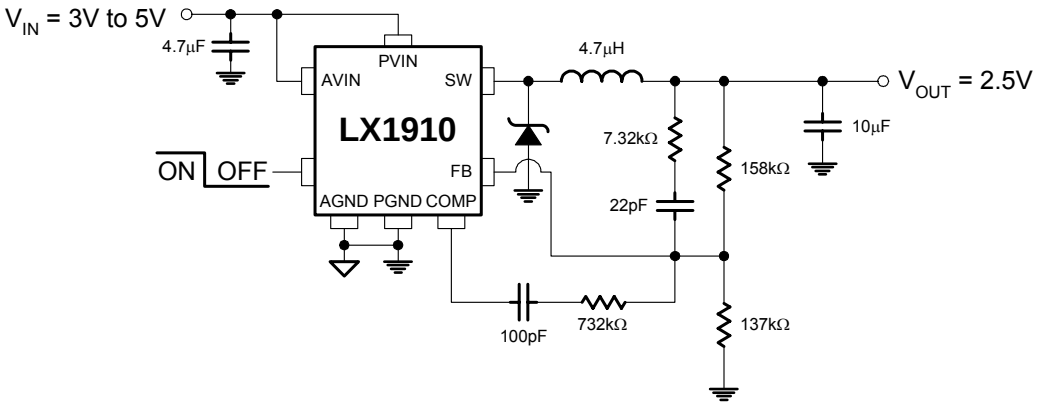

Figure 3 – Typical Application For A 2.5V Output Voltage

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THEORY OF OPERATION

The LX1910 is step-down, pulse-width modulated (PWM), DC-DC converter with an adjustable output voltage range of 1.2V to 80% of the input voltage.

An internal 1MHz reference oscillator determines the switching frequency when in the PWM mode of operation. During a light load condition the PWM mode will switch into a PFM mode of operation. In this PFM mode the switched output has a fixed ON time and the frequency is reduced to provide the lower output current demand. At a complete NO load condition the output switching becomes intermittent (Skip Mode) in order to maintain the output voltage level. The device switches modes when the error amplifier output goes below a voltage level that is set at the minimum voltage of the saw-tooth reference signal at the PWM comparator.

The LX1910 uses a low power, high gain bandwidth, transconductance amplifier for its error amplifier. The bandgap voltage reference goes to the positive input of the error amplifier. An external resistor divider feeds back the output voltage to the negative input of the error amplifier. The output of the transconductance error amplifier is a current proportional to gm gain of the amplifier. This output current is converted back to a voltage by the impedance connected to the output of this amplifier.

The output of the error amplifier is connected to the COMP pin. The impedance connected to this pin will change the open loop response of this error amplifier. A capacitor to ground on the COMP pin will establish a gain setting for the error amplifier at a given frequency on the Bode plot of the system response. The capacitor sets a pole in the Bode plot response which establishes a -1 slope in the response for a given range of frequency. The output LC filter also establishes another double pole (-2 slope) at the LC frequency. To produce a stable system the slope of the Bode plot has to be back to a -1 slope when the gain goes through unity or 0db. For systems utilizing output capacitors with appreciable ESR, a resistor added in series with the capacitor on the COMP pin can create a -1 slope shelved at a lower frequency than the system cross over frequency ensuring stability. The ESR of the output filter capacitor will shelve the -2 slope of the LC filter back to a -1 slope at the break frequency established by the RC values. This break frequency needs to be at a lower frequency that the cross over frequency, usually a 5 to 1 ratio. For additional stability a capacitor can be connected across the top resistor of the feedback divider network. This will produce a zero, +1 slope, in the Bode plot response at a frequency determined by the RC values. To be effective this lead should start at a lower frequency than the cross over frequency, again at a ratio of 5 to 1.

For low ESR output capacitors a more complex compensation scheme is layed out in the applications section.

The LX1910 has an internal current limit established by a comparator with a fixed voltage reference. The PMOS transistor switch has a current mirror brought off the drain to give a current reduction for sensing the output current. The current from the current mirror is passed through a resistor to ground that also is connected to the other input of the current limit comparator. The current limit is processed on a cycle by cycle basis and when the current limit comparator changes state it turns off the output switch thereby reducing the PWM duty cycle. The output pulse width can be reduced to less than 100ns when confronted with a short circuit.

The LX1910 also has a thermal shutdown detector that senses the chip temperature and shuts down operation when the temperature hits 150 deg C. This gives added protection when there is a continuous short circuit on the output.

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APPLICATION NOTE

The typical LX1910 application circuit is depicted in Fig. 2. Component selection is dependant on the required load, and begins with the selection of an output inductor.

INDUCTOR SELECTION

Generally the output inductance value will be from 1µH to 4.7µH. The inductor value is sized to meet the desired inductor ripple current. While smaller values of inductance will increase the transient response capability of the regulator, they will also raise the inductor ripple current causing an increase in output ripple voltage. This relationship is given by the following equation:

$$I_{RIPPLE} = \frac{1}{f_{OSC} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{eq. 1}$$

where V_{IN} is the maximum input voltage for the application, f_{OSC} is the minimum oscillator frequency, and V_{OUT} is the output voltage. Choosing these conditions will ensure that the calculated inductance value will correspond to the worst case inductor ripple current.

Generally, it is accepted practice to begin by selecting an inductor based on an inductor ripple current which is 20% to 40% of the maximum DC load current (I_{DC}). Substituting this value and solving eq. 1 for the inductor value yields:

$$L = \frac{1}{f_{OSC} \cdot I_{DC}(20\%)} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \qquad \text{eq. 2}$$

The DC rating of the inductor needs to be equivalent to the maximum DC current of the application plus half of the inductor ripple current.

Generally, better efficiency is obtained when the inductor ripple current is minimized. In addition, the inductor DC resistance (DCR) also plays a significant role.

OUTPUT CAPACITOR SELECTION

The selection of output capacitor is generally driven by the required output ripple voltage which is largely controlled by the capacitive effective series resistance (ESR). The output ripple voltage is given by:

$$V_{RIPPLE} = I_{RIPPLE} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_{OUT}}\right) \qquad \text{eq. 3}$$

where C_{OUT} is the total output capacitance. Low ESR values not only yield lower output ripple voltages, but also improve the transient response of the circuit.

Knowing the desired output ripple voltage, a capacitor type can then be selected. Using eq. 3 it can then be determined how many of the chosen capacitor type will need to be used in the application circuit.

Once the desired ripple voltage is met, the RMS current rating of the capacitors can be assessed from capacitor's manufacturer datasheet to ensure it is not exceeded. Generally, once the ESR requirement has been met the RMS current rating requirement has been more than satisfied.

INPUT CAPACITOR SELECTION

In PWM operation the source current of the internal MOSFET, at the SW pin, is a square wave at a duty cycle of V_{OUT}/V_{IN}. Localized low ESR decoupling must be placed at the pin in order to prevent large voltage transients. The input capacitors are selected according to their maximum RMS current rating which is given by:

$$I_{SW(RMS)} = I_{OUT(MAX)} \cdot \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \qquad \text{eq. 4}$$

where $I_{OUT(MAX)}$ is the maximum application DC output current and V_{IN} is the maximum input voltage. Once a capacitor is selected, the number of capacitors needed can be determined using the capacitor manufacturer's RMS current rating ensuring that it exceeds the calculated RMS switch current.

OUTPUT VOLTAGE PROGRAMMING

The output voltage, for the LX1910, is adjustable and set using a resistor divider to sense the output voltage as shown in Figure 4.

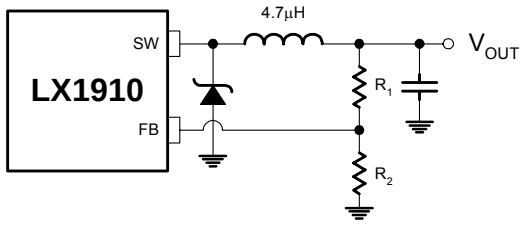

Figure 4 – Output Voltage Programming

The output voltage is determined using the following relationship:

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$$V_{OUT} = V_{FBT} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad \text{eq. 5}$$

where V_{FBT} is the Feedback Threshold Voltage.

A good starting value for R_2 is anywhere from 50kΩ to 100kΩ. Selecting R_2 yields an R_1 value for any given output voltage of:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FBT}} - 1\right) \quad \text{eq. 6}$$

COMPENSATION

The LX1910 is a voltage-mode PWM controller and therefore has a complex pole due to the inductor and output capacitance that requires compensation for stable operation. This complex pole is at a frequency of:

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_O}} \quad \text{eq. 7}$$

Normally a compensating zero is formed with the output capacitor's capacitance and ESR, but if low ESR ceramic capacitors are used then the zero caused is usually much larger than the desired zero cross over frequency. As a result, a zero must be entered into the feedback loop in order to maintain stability.

The LX1910 compensation scheme is shown in Figure 5.

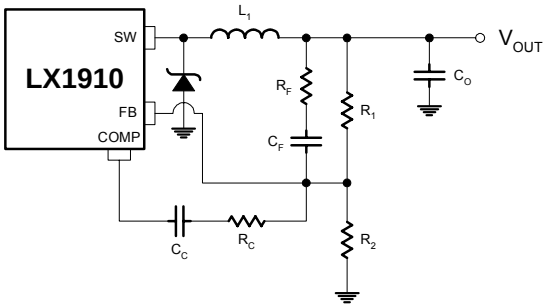

Figure 5 – Compensation

The compensation circuitry comprises of the feed-forward resistor (R_F) and capacitor (C_F) and the COMP pin resistor (R_C) and capacitor (C_C). This circuit compensates the LX1910's feedback such that it will be unconditionally stable regardless of output capacitor value or ESR. This allows for a wide variety of output filtering schemes.

To begin choosing the values for compensation, the Thevinin equivalent of R_1 in parallel with R_2 must be calculated using the following equation.

$$R_{TH} = \frac{R_1 \cdot R_2}{R_1 + R_2} \quad \text{eq. 7}$$

R_C is then chosen such that it is approximately ten times the calculate R_{TH} value.

$$R_C = 10 \cdot \left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right) \quad \text{eq. 8}$$

There are two zeros shown in the compensation scheme: the first set by the R_C/C_C combination and the second set by the R_{TH}/C_F combination given by the following equations:

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} \quad \text{eq. 9}$$

$$F_{Z2} = \frac{1}{2 \cdot \pi \cdot R_{TH} \cdot C_F} \quad \text{eq. 10}$$

Since the maximum phase contribution takes place over a decade of frequency, the first zero is set to be one-tenth that of the complex pole frequency (eq. 7) set by the output inductor and capacitor.

$$F_{Z1} = \frac{1}{10} \cdot F_{P1} \quad \text{yielding}$$

$$\frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} = \frac{1}{10} \cdot \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_O}}$$

Solving for the COMP capacitor (C_C) yields.

$$C_C = \frac{10\sqrt{L \cdot C_O}}{R_C} \quad \text{eq. 11}$$

Next, the second zero (F_{Z2}) is calculated using equation 10 and setting the zero frequency at two octaves or four times that of the complex pole (eq. 7). This second zero acts as an output capacitance ESR emulator. Setting both zero's frequency for maximum phase shift would result in too much gain.

$$F_{Z2} = 4 \cdot F_{P1} \quad \text{yielding}$$

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$$\frac{1}{2\cdot\pi\cdot R_{TH}\cdot C_F} = 4\cdot\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C_O}}$$

Solving for the Feed-Forward capacitor (C_F) yields.

$$C_F = \frac{\sqrt{L\cdot C_O}}{4\cdot R_{TH}} \qquad \text{eq. 12}$$

It is generally good practice to roll off the upper frequency response to prevent any high gain of high frequency noise. This pole is setup by the R_F/C_F combination. The frequency of this pole should be set high enough so as to not counteract the influence of the zeros. Setting the frequency of the pole to ten times the frequency of Z_{F2} yields the following equation:

$$F_{P2} = 10\cdot F_{Z2} \qquad \text{yielding}$$

$$\frac{1}{2\cdot\pi\cdot R_F\cdot C_F} = \frac{10}{2\cdot\pi\cdot R_{TH}\cdot C_F}$$

Solving for the Feed-forward resistor (R_F) yields.

$$R_F = \frac{R_{TH}}{10} \qquad \text{eq. 13}$$

The calculated zeros will yield approximately 50° to 90° of phase margin regardless of the type of output capacitors resulting in an unconditionally stable circuit design. Using the previous equations, both phase margin and close-loop bandwidth are optimized.

LAYOUT CONSIDERATIONS

The high peak currents and switching frequencies present in DC/DC converter applications require careful attention to device layout for optimal performance. Basic design rules include:

1. Maintaining wide traces for power components (e.g., width > 50mils)
2. Place CIN, COUT, the Schottky diode, and the inductor close to the LX1910
3. Minimize trace capacitance by reducing the etch area connecting the SW pin to the inductor
4. Minimizing the etch length to the FB pin to reduce noise coupling into this high impedance sense input.

Other considerations optionally include placing a 0.1uF capacitor between the LX1910 VOUT pin and GND pin to reduce high frequency noise and decoupling the VIN pin using a 0.1uF capacitor.

DIODE SELECTION

A Schottky diode is recommended for use with the LX1910 because it provides fast switching and superior reverse recovery performance. The Microsemi UPS5817 (20V @ 1A) makes an effective choice for most applications.

DESIGN EXAMPLE

Given the following application requirements:

$$V_{IN} = 5.5V \text{ to } 3.3V$$
$$V_{OUT} = 2.5V$$
$$I_{OUT(MAX)} = 600mA$$
$$V_{RIPPLE(MAX)} = 5mV$$
$$f_{OSC} = 1MHz$$
$$ESR = 1.5m\Omega$$

Inductor Calculation:

Calculate the required circuit components. First calculate the output inductor based on the maximum desired inductor ripple current using eq. 2. Since the inductor ripple islargest at higher input voltages, use the maximum V_{IN} specified.

$$L = \frac{1}{f_{OSC}\cdot I_{DC}(20\%)}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$L = \frac{1}{1MHz\cdot 120mA}\cdot\left(1-\frac{2.5V}{5.5V}\right)$$

$$L = 3.38\mu H \Rightarrow 4.7\mu H$$

Output Capacitor Calculation:

Next the output capacitance can be calculated based on the maximum desired ripple voltage using eq. 3.

$$V_{RIPPLE} = I_{RIPPLE}\cdot\left(ESR + \frac{1}{8\cdot f_{OSC}\cdot C_{OUT}}\right)$$

$$5mV = 120mA\cdot\left(1.5m\Omega + \frac{1}{8\cdot 1MHz\cdot C_{OUT}}\right)$$

Solving for C_{OUT} yields:

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APPLICATION NOTE

$$C_{OUT} = \frac{I_{RIPPLE}}{8 \cdot f_{OSC} \cdot (V_{RIPPLE} - I_{RIPPLE} \cdot ESR)}$$

$$C_{OUT} = \frac{120mA}{8 \cdot 1MHz \cdot (5mV - 120mA \cdot 1.5m\Omega)} = 3.11\mu F$$

It is recommended that at least a 10µF output capacitor be used to ensure good transient response. Selecting this value will guarantee that the maximum ripple voltage specification is met.

Input Capacitor Calculation:

Bypass the input terminal of the LX1910 with a 4.7µF capacitor or larger.

Feedback Resistor Calculation:

Before the output voltage resistors are calculated, it should be noted that a good starting value for the Thevinin equivalent value of R_1 and R_2 (eq.7) is 73.2kΩ. If this value is maintained then the compensation components will not need to be changed even if the output voltage requirement is altered. Given eq. 5 and eq. 7:

$$2.5V = 1.17V \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$100k\Omega = \frac{R_1 \cdot R_2}{R_1 + R_2}$$

By substitution R_1 = 158kΩ and R_2 = 137kΩ.

Compensation Components Calculation:

Next the compensation components are selected. Using equations 8 and 11, the COMP pin components are calculated as follows:

$$R_C = 10 \cdot \left(\frac{R_1 \cdot R_2}{R_1 + R_2}\right)$$

$$R_C = 10 \cdot \left(\frac{158 \cdot 137}{158 + 137}\right) \cdot k\Omega = 732k\Omega$$

then

$$C_C = \frac{10\sqrt{L \cdot C_O}}{R_C}$$

$$C_C = \frac{10\sqrt{4.7\mu H \cdot 10\mu F}}{732k\Omega} = 94pF \Rightarrow 100pF$$

Next using equation 12 the C_F capacitor is calculated as follows:

$$C_F = \frac{\sqrt{L \cdot C_O}}{4 \cdot R_{TH}}$$

$$C_F = \frac{\sqrt{4.7\mu H \cdot 10\mu F}}{4 \cdot 73.2k\Omega} = 23pF \Rightarrow 22pF$$

The final step is to calculate the feed-forward resistor in order to roll-off the system response using equation 13.

$$R_F = \frac{R_{TH}}{10}$$

$$R_F = \frac{73.2}{10} \cdot k\Omega = 7.32k\Omega$$

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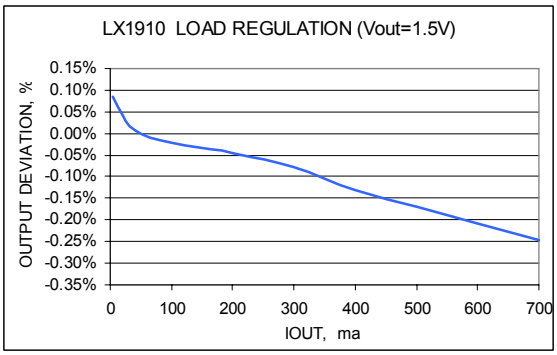
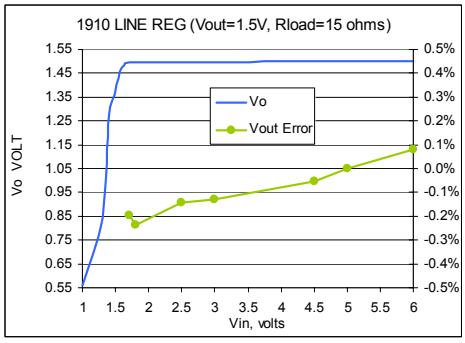
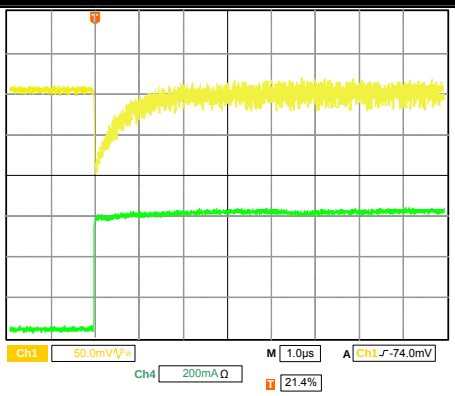
LOAD REGULATION



LINE REGULATION

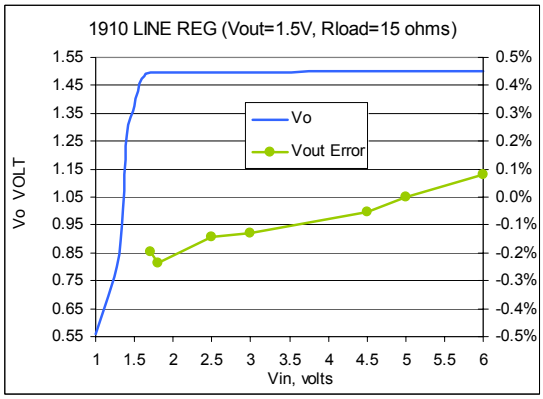


STEP RESPONSE

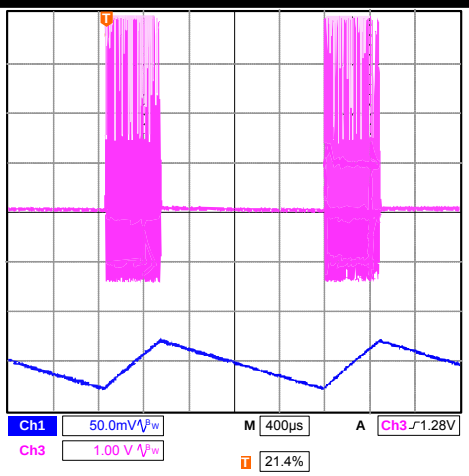


Output Load Step Response: CH1: VOUT and CH4: IOUT; Condition: VIN = 5.0V; ISTEP = 50 to 600mA

LINE REGULATION

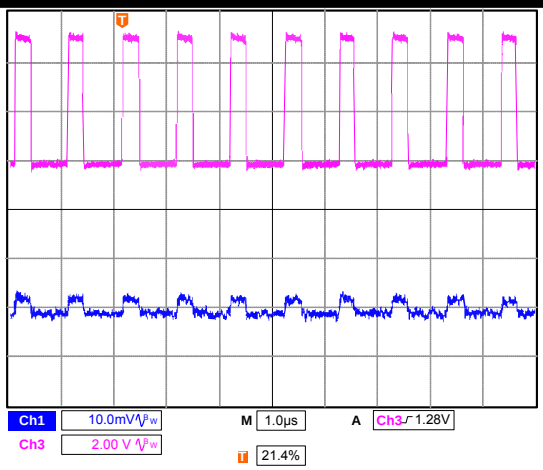


PFM MODE



Switching Waveforms: PFM Mode
CH3: V_{SW} (pin 8) and CH1: V_{OUT}; (V_{IN} = 5.0V; I_{OUT} = 1mA)

PWM MODE



Switching Waveforms: PWM Mode
CH3: V_{SW} (pin 8) and CH1: V_{OUT}; (V_{IN} = 5.0V; I_{OUT} = 10mA)

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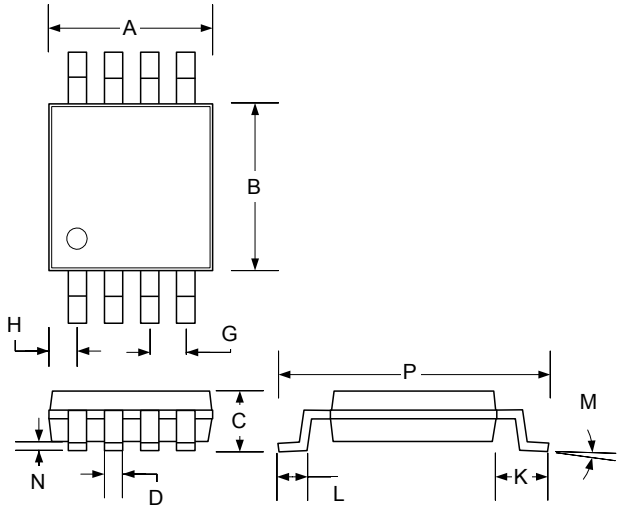
PACKAGE DIMENSIONS

DU 8-Pin Miniature Shrink Outline Package (MSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.85	3.05	.112	.120
B	2.90	3.10	.114	.122
C	–	1.10	–	0.043
D	0.25	0.40	0.009	0.160
G	0.65 BSC		0.025 BSC	
H	0.38	0.64	0.015	0.025
J	0.13	0.18	0.005	0.007
K	0.95 BSC		0.037 BSC	
L	0.40	0.70	0.016	0.027
M	3°		3°	
N	0.05	0.15	0.002	0.006
P	4.75	5.05	0.187	0.198

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES

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