

FEATURES

- ❑ Eight 16-bit High-Speed Pipeline Registers
- ❑ Programmable Multilevel Register Configurations
- ❑ Access time of 15 ns
- ❑ Hold, Shift, and Load Instructions
- ❑ Replaces IDT73200
- ❑ 52-pin PLCC, J-Lead

DESCRIPTION

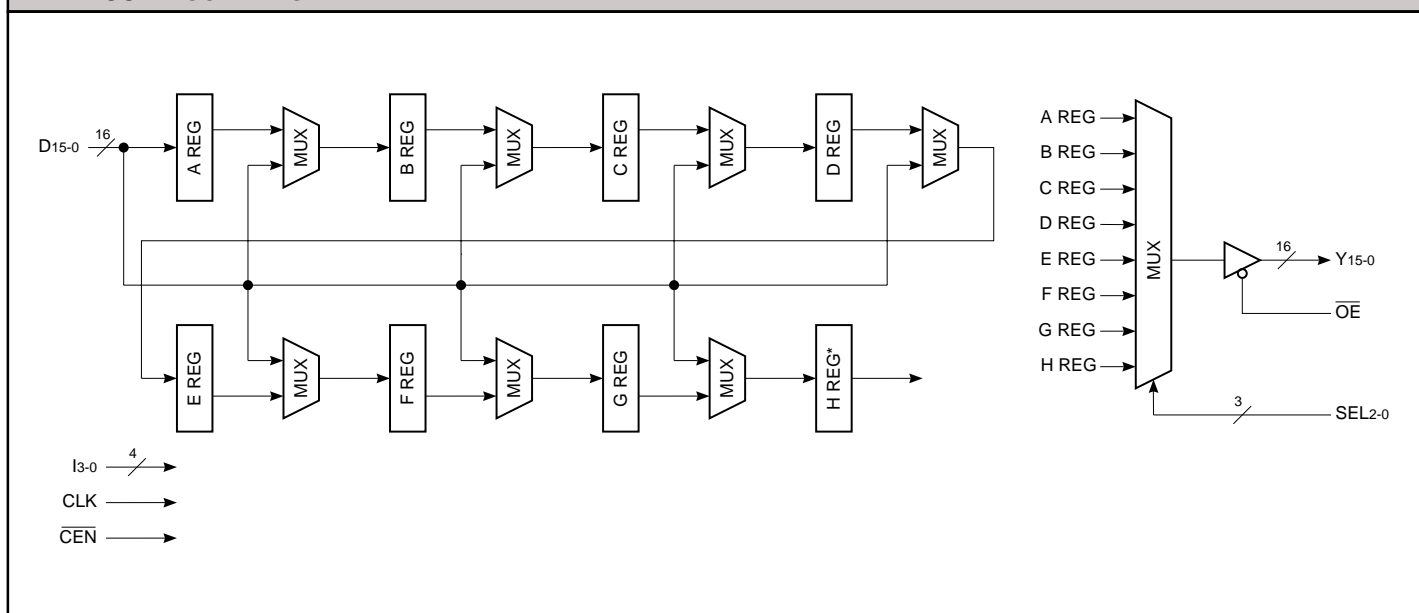
The **LPR200** is a programmable multilevel pipeline register. This device is pin-for-pin compatible with the IDT73200.

The LPR200 contains eight 16-bit high-speed pipeline registers which can be configured as eight independent, 1-level pipelines; four independent, 2-level pipelines; two independent, 4-level pipelines; or as one 8-level pipeline.

The Instruction pins, I3-0, control the loading of the registers. The registers can be configured as an eight-stage delay line with data loaded into A and shifted sequentially through B, C, D, E, F, G and H as shown in Table 1. The Instruction pins may also be set to prevent any register from changing.

The Select lines, S2-0, control an 8-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allow simultaneous write and read operations on different registers.

LPR200 BLOCK DIAGRAM



16-bit Multilevel Pipeline Register

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers.

Inputs

D15-0 — Data Input

16-bit data input port. Data is latched into the registers on the rising edge of CLK.

Outputs

Y15-0 — Data Output

16-bit data output port.

Controls

I3-0 — Instruction Control

The instruction control pins select which register operation will be carried out. Refer to Table 2.

SEL2-0 — Output Select

The output select pins control which register contents will appear at the Y15-0 output pins. Refer to Table 3.

\overline{CEN} — Clock Enable

When \overline{CEN} is LOW, the instruction designated by I3-0 is performed on the registers. When \overline{CEN} is HIGH, no register operations are performed.

TABLE 1. REGISTER LOAD OPERATIONS

Single 8-Level	Two 4-Level
Four 2-Level	Eight 1-Level

\overline{OE} — Output Enable

When \overline{OE} is LOW, the register data specified by SEL2-0 is available on the Y15-0 output pins. When \overline{OE} is HIGH, the output port is in a high-impedance state.

16-bit Multilevel Pipeline Register
TABLE 2. LPR200 INSTRUCTION TABLE

Mnemonics	Inputs				Description
	I ₃	I ₂	I ₁	I ₀	
LDA	0	0	0	0	D ₁₅₋₀ →A
LDB	0	0	0	1	D ₁₅₋₀ →B
LDC	0	0	1	0	D ₁₅₋₀ →C
LDD	0	0	1	1	D ₁₅₋₀ →D
LDE	0	1	0	0	D ₁₅₋₀ →E
LDF	0	1	0	1	D ₁₅₋₀ →F
LDG	0	1	1	0	D ₁₅₋₀ →G
LDH	0	1	1	1	D ₁₅₋₀ →H
LSHAH	1	0	0	0	D ₁₅₋₀ →A A→B B→C C→D D→E E→F F→G G→H
LSHAD	1	0	0	1	D ₁₅₋₀ →A A→B B→C C→D
LSHEH	1	0	1	0	D ₁₅₋₀ →E E→F F→G G→H
LSHAB	1	0	1	1	D ₁₅₋₀ →A A→B
LSHCD	1	1	0	0	D ₁₅₋₀ →C C→D
LSHEF	1	1	0	1	D ₁₅₋₀ →E E→F
LSHGH	1	1	1	0	D ₁₅₋₀ →G G→H
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

**TABLE 3. LPR200
OUTPUT SELECT**

SEL ₂	SEL ₁	SEL ₀	Y ₁₅₋₀
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

16-bit Multilevel Pipeline Register
MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +155°C
Operating ambient temperature	–55°C to +125°C
V _{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V _{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V _{CC} + 0.5 V
Output current into low outputs	50 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

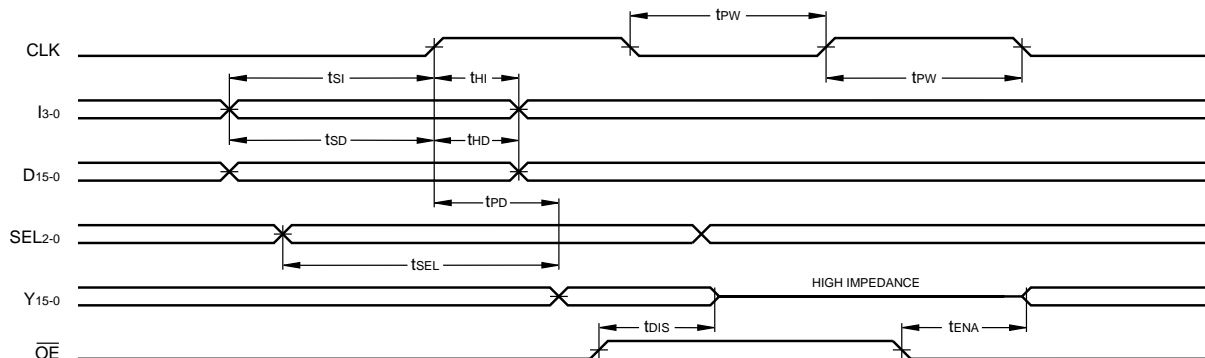
Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = –8.0 mA	2.4			V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 16 mA			0.4	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{Ix}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	(Note 12)			±20	μA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)		2.0	10	mA
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz			10	pF
C _{OUT}	Output Capacitance	T _A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS
COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

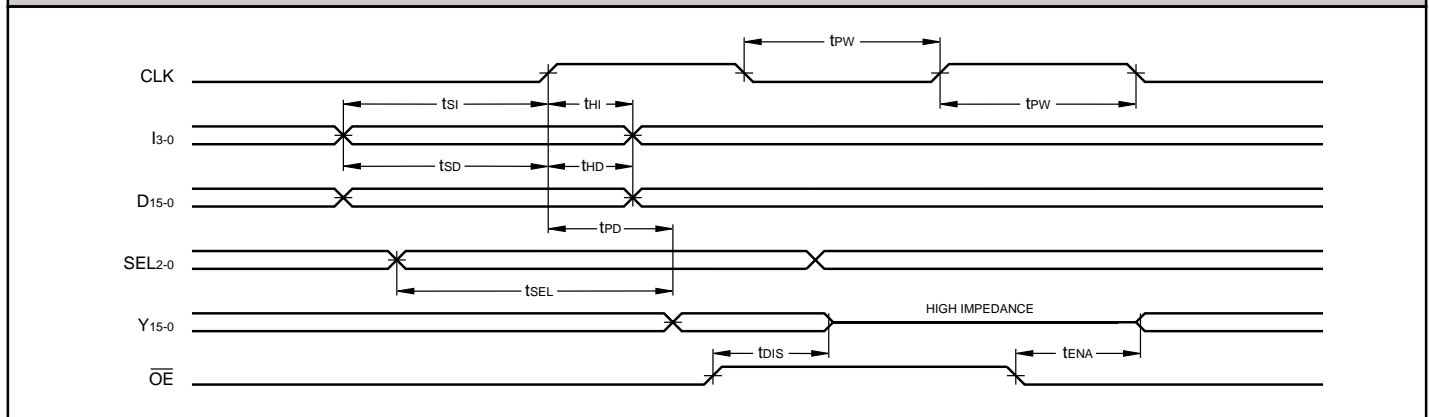
Symbol	Parameter	LPR200–					
		20*		15		12*	
		Min	Max	Min	Max	Min	Max
t _{CYC}	Cycle Time	20		15		12	
t _{PW}	Clock Pulse Width	5		5		5	
t _{PD}	Clock to Output Delay		20		15		12
t _{SEL}	Select to Output Delay		20		15		12
t _{SI}	Instruction Setup Time	5		5		4	
t _{HI}	Instruction Hold Time	2		2		2	
t _{SD}	Data Setup Time	4		4		3	
t _{HD}	Data Hold Time	2		2		1	
t _{SC}	Clock Enable Setup Time	5		5		5	
t _{HC}	Clock Enable Hold Time	2		2		2	
t _{DIS}	Three-State Output Disable Delay (Note 11)		10		9		8
t _{ENA}	Three-State Output Enable Delay (Note 11)		15		10		9

SWITCHING WAVEFORMS


***DISCONTINUED SPEED GRADE**

SWITCHING CHARACTERISTICS
MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LPR200–			
		20*		15*	
		Min	Max	Min	Max
t _{CYC}	Cycle Time	20		15	
t _{PW}	Clock Pulse Width	6		5	
t _{PD}	Clock to Output Delay		20		15
t _{SEL}	Select to Output Delay		20		15
t _{SI}	Instruction Setup Time	6		5	
t _{HI}	Instruction Hold Time	3		2	
t _{SD}	Data Setup Time	5		4	
t _{HD}	Data Hold Time	3		2	
t _{SC}	Clock Enable Setup Time	6		5	
t _{HC}	Clock Enable Hold Time	2		2	
t _{DIS}	Three-State Output Disable Delay (Note 11)		13		9
t _{ENA}	Three-State Output Enable Delay (Note 11)		13		10

SWITCHING WAVEFORMS


***DISCONTINUED SPEED GRADE**

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at -0.6 V and $V_{CC} + 0.6$ V. The device can withstand indefinite operation with inputs in the range of -0.5 V to $+7.0$ V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 10 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

- a. A 0.1 μ F ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.
- b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.
- c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ± 200 mV level from the measured steady-state output voltage with ± 10 mA loads. The balancing voltage, V_{TH} , is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

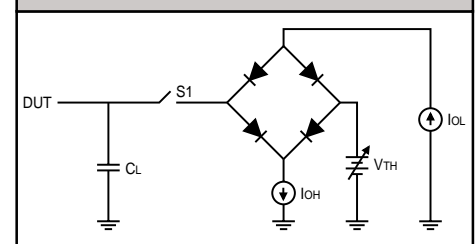
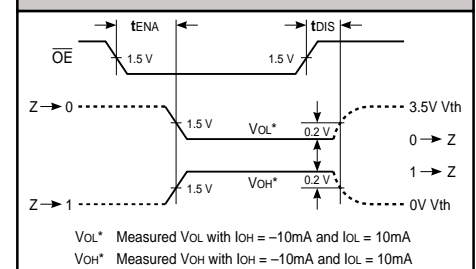


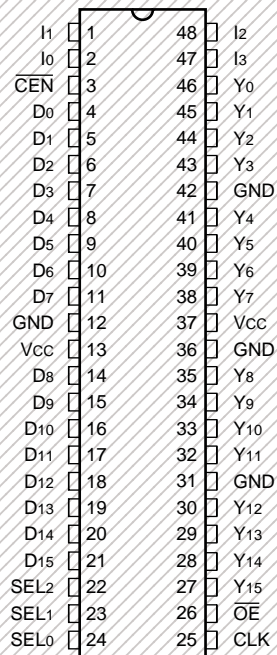
FIGURE B. THRESHOLD LEVELS



16-bit Multilevel Pipeline Register

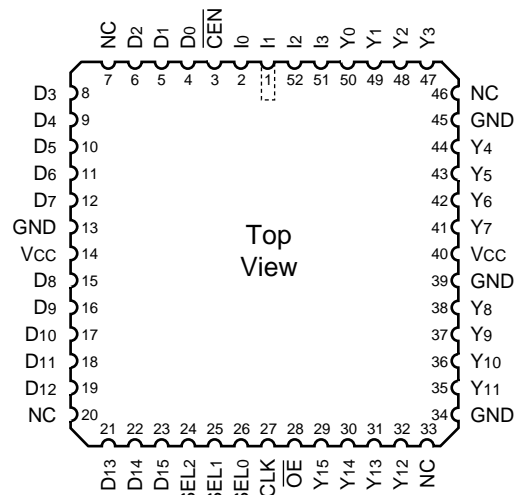
LPR200 — ORDERING INFORMATION

48-pin



Discontinued Package

52-pin



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	
	0°C to +70°C — COMMERCIAL SCREENING			
15 ns			LPR200JC15	
	–55°C to +125°C — COMMERCIAL SCREENING			
	–55°C to +125°C — MIL-STD-883 COMPLIANT			