LMS12
12-bit Cascadable Multiplier-Summer

FEATURES

- 12 x 12-bit Multiplier with Pipelined 26-bit Output Summer
- Summer has 26-bit Input Port Fully Independent from Multiplier Inputs
- Cascadable to Form Video Rate FIR Filter with 3-bit Headroom
- A, B, and C Input Registers Separately Enabled for Maximum Flexibility
- 28 MHz Data Rate for FIR Filtering Applications
- High Speed, Low Power CMOS Technology
- 84-pin PLCC, J-Lead

DESCRIPTION

The **LMS12** is a high-speed 12 x 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high-speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

ARCHITECTURE

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

MULTIPLIER

The $A_{11\text{-}0}$ and $B_{11\text{-}0}$ inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input registers, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 x 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in two's complement format. The multiplication result forms the input to the 24-bit product register.

SUMMER

The $C_{25\text{-}0}$ inputs to the LMS12 form a 26-bit two's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the sign extended contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

OUTPUT

The FTS input is the feedthrough control for the S register. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, data from the S register is output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high-impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 Block Diagram

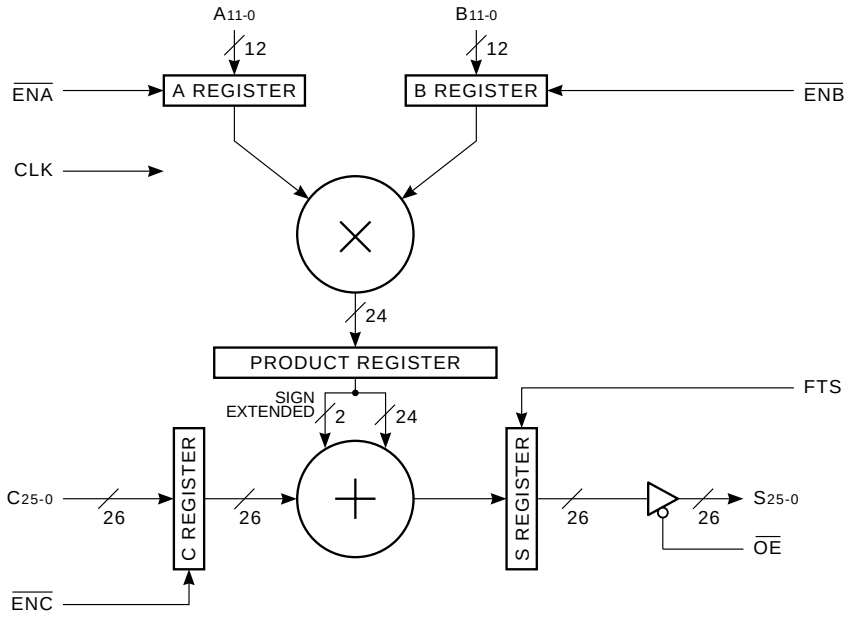
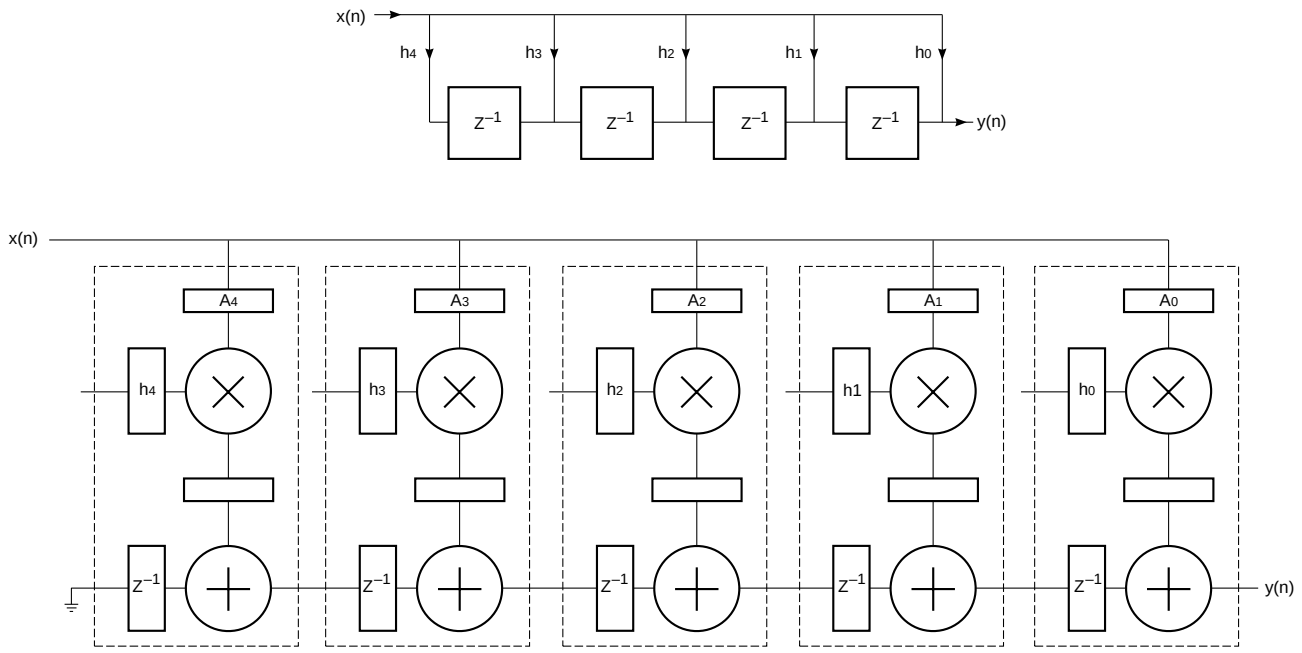


FIGURE 1. FLOW DIAGRAM FOR 5-TAP FIR FILTER



APPLICATIONS

The LMS12 is designed specifically for high-speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Figure 1.

The operation of the 5-tap FIR filter implementation of Figure 1 is depicted in Table 1. The filter weights h_4 - h_0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A register contents and sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S_0 is produced by the rightmost device, which has h_0 as its filter weight and A_0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

TABLE 1. TIMING EXAMPLE FOR 5-TAP NONDECIMATING FIR FILTER

CLK Cycle	1	2	3	4	5	6	7	8	9
$X_{(n)}$	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A_4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A_3 Register Sum 3		X_n	X_{n+1} h_3X_n + h_4X_{n-1}	X_{n+2} h_3X_{n+1} + h_4X_n	X_{n+3} h_3X_{n+2} + h_4X_{n+1}	X_{n+4} h_3X_{n+3} + h_4X_{n+2}	X_{n+5} h_3X_{n+4} + h_4X_{n+3}	X_{n+6} h_3X_{n+5} + h_4X_{n+4}	X_{n+7} h_3X_{n+6} + h_4X_{n+5}
A_2 Register Sum 2		X_n	X_{n+1} h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+2} h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+3} h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+4} h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+5} h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+6} h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}	X_{n+7} h_2X_{n+6} + h_3X_{n+5} + h_4X_{n+4}
A_1 Register Sum 1		X_n	X_{n+1} h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+2} h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+3} h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+4} h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+5} h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+6} h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+7} h_1X_{n+6} + h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}
A_0 Register Sum 0		X_n	X_{n+1} h_0X_n + h_1X_{n-1} + h_2X_{n-2} + h_3X_{n-3} + h_4X_{n-4}	X_{n+2} h_0X_{n+1} + h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+3} h_0X_{n+2} + h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+4} h_0X_{n+3} + h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+5} h_0X_{n+4} + h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+6} h_0X_{n+5} + h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+7} h_0X_{n+6} + h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}

FIGURE 2A. INPUT FORMATS

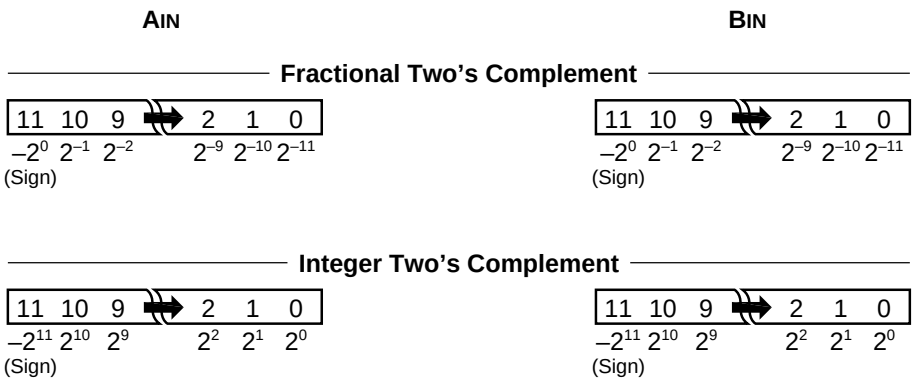
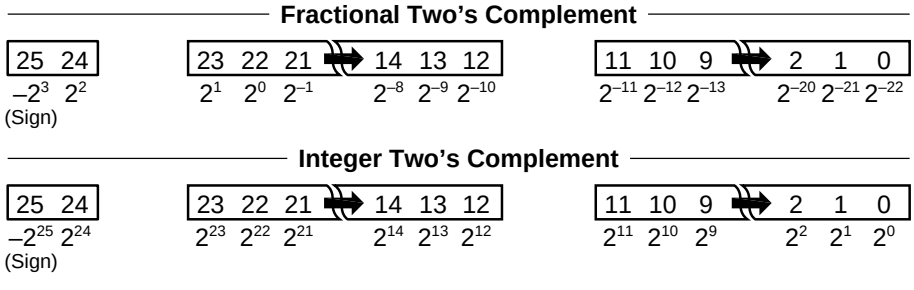


FIGURE 2B. OUTPUT FORMATS



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

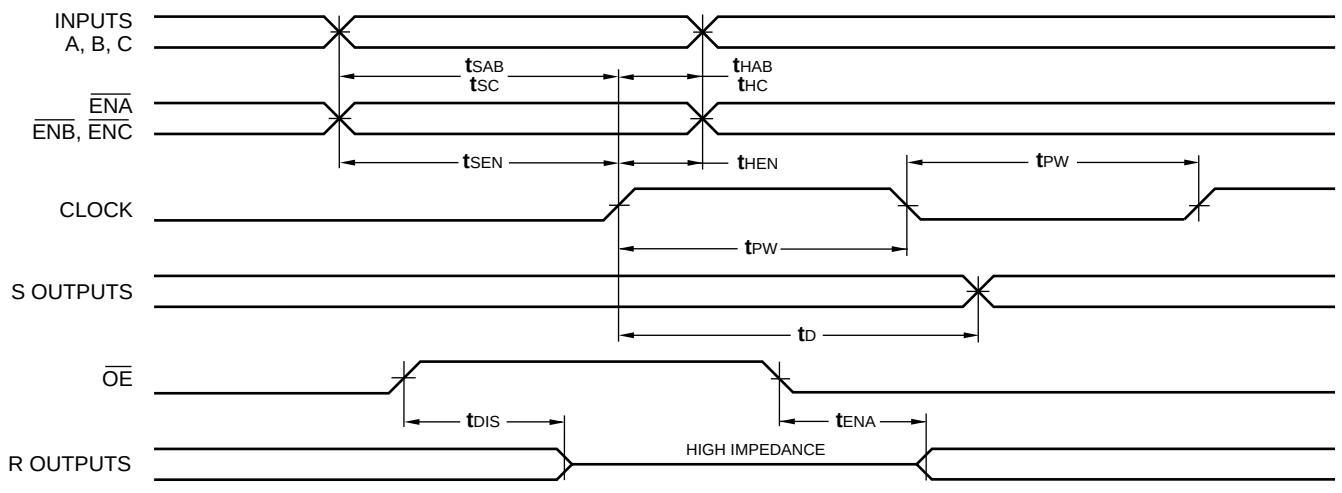
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMS12–							
		65*		50*		40		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CP}	Clock Period	40		35		30		25	
t_{PW}	Clock Pulse Width	15		15		12		8	
t_{SAB}	A, B, Data Setup Time	15		12		12		10	
t_{SC}	C Data Setup Time	15		10		7		7	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12		12		10	
t_{HAB}	A, B, Data Hold Time	5		5		5		2	
t_{HC}	C Data Hold Time	5		5		5		2	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5		2	
t_D	Clock to S–FT = 1		50		40		35		30
	Clock to S–FT = 0		25		25		25		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22		22		20

SWITCHING WAVEFORMS



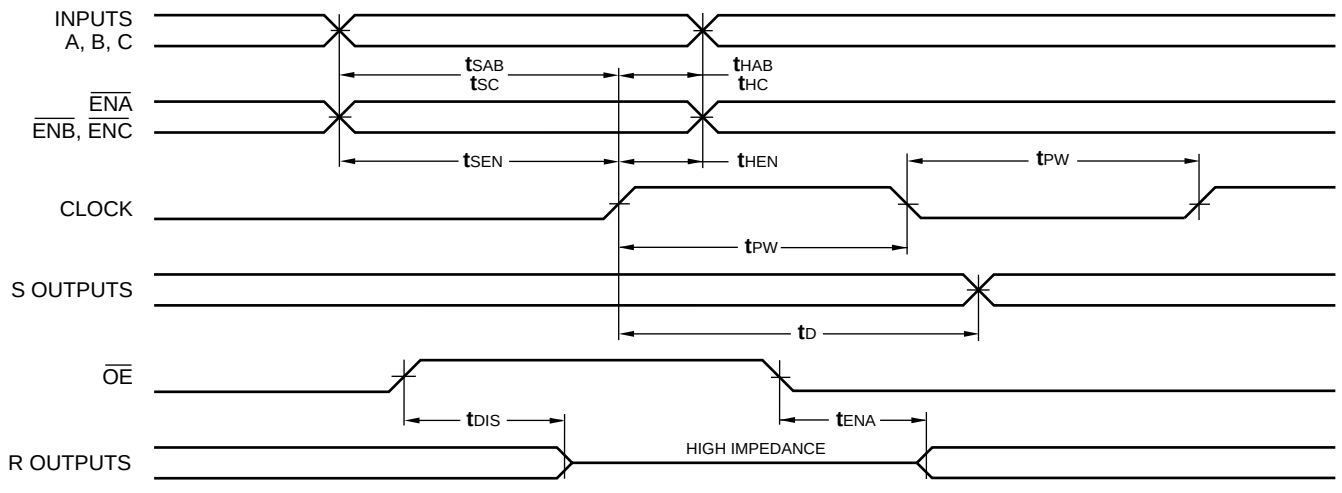
*DISCONTINUED SPEED GRADE

SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMS12– 65* Min	65* Max	50* Min	50* Max	40* Min	40* Max
t_{CP}	Clock Period	40		35		30	
t_{PW}	Clock Pulse Width	15		15		12	
t_{SAB}	A, B, Data Setup Time	15		15		12	
t_{SC}	C Data Setup Time	15		15		12	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		15		12	
t_{HAB}	A, B, Data Hold Time	5		5		5	
t_{HC}	C Data Hold Time	5		5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
t_D	Clock to S–FT = 1		50		45		35
	Clock to S–FT = 0		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22		22

SWITCHING WAVEFORMS



*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

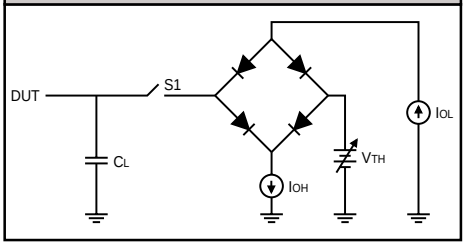
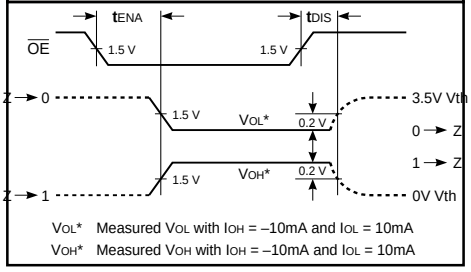
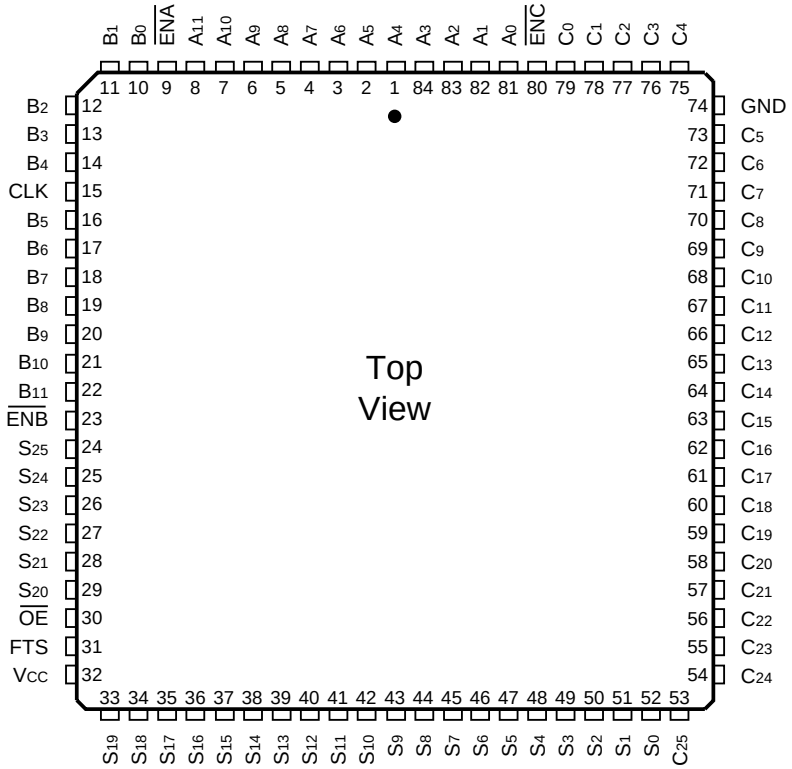


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

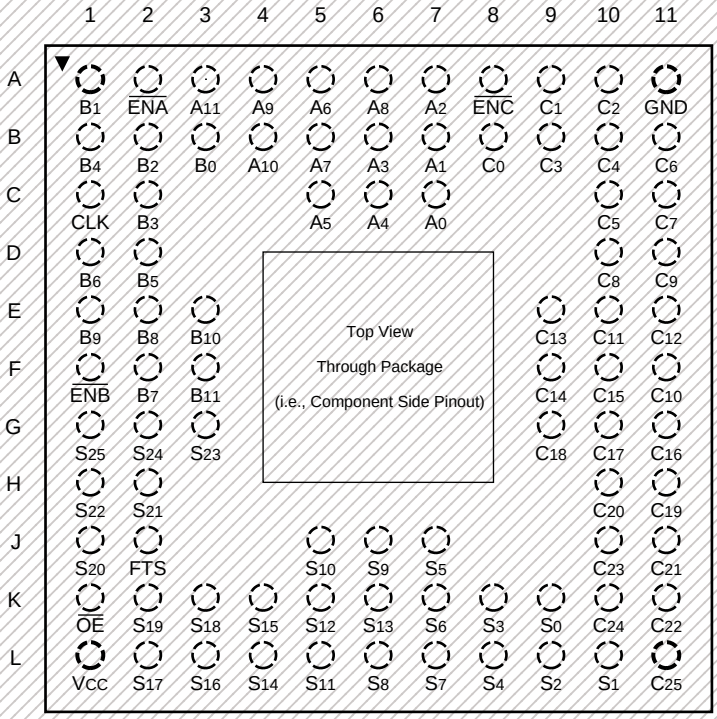
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LMS12JC40
35 ns	LMS12JC35

ORDERING INFORMATION

84-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
	–55°C to +125°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT