

TinyRISC® LR4102

Microprocessor

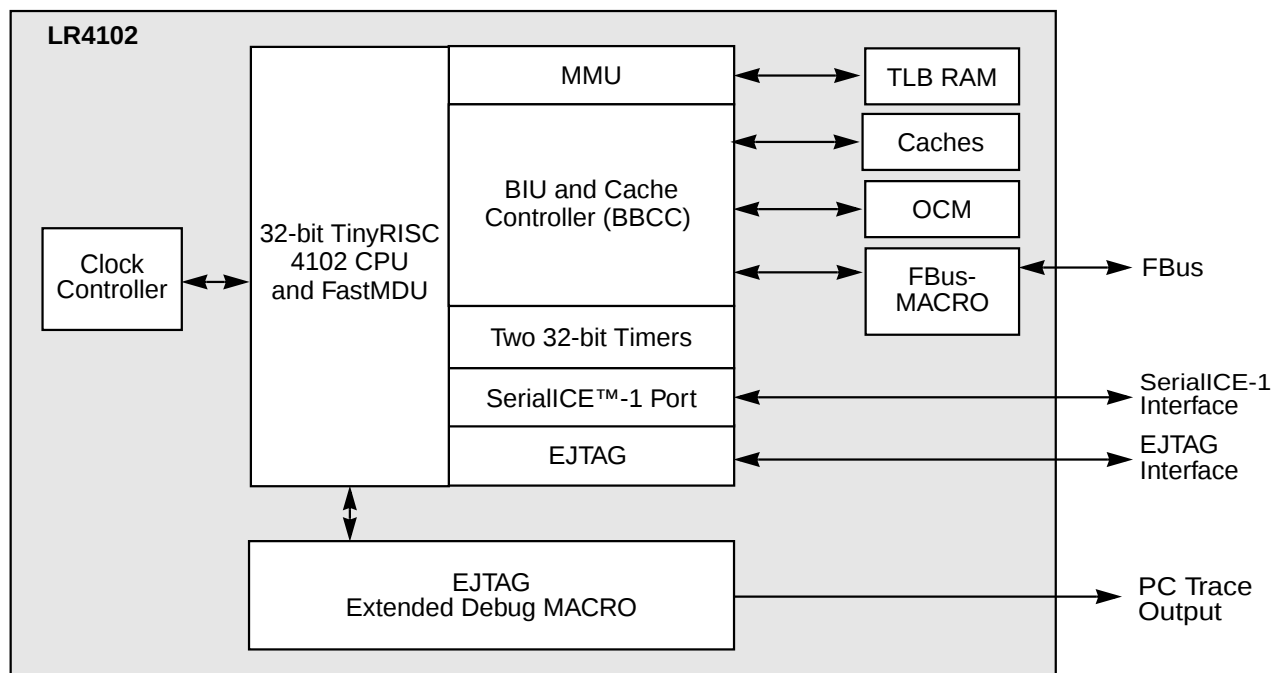
Datasheet

LSI LOGIC®

The TinyRISC LR4102 Microprocessor is a compact, high performance 32-bit microprocessor implemented in the LSI Logic G11™ technology. The LR4102 is a complete microprocessor solution with caches, an external bus interface with built-in memory controllers, and on-chip debug. The LR4102 is built using the EZ4102 EasyMACRO subsystem, available to customers through the LSI Logic CoreWare® program.

The LR4102 provides a 32-bit FBusMACRO to control all off-chip data transactions (including DRAM or SDRAM) and an EJTAG interface for on-chip debug with PC trace output. [Figure 1](#) illustrates the LR4102 chip.

Figure 1 LR4102 Block Diagram



The LR4102 microprocessor is powered by either 2.5 V (for 85 MHz operation) or 1.8 V (for 50 MHz operation). The chip I/O ring requires 3.3 V. With a system clock of 85 MHz, peak performance is 85 MIPS and sustained performance is estimated at 68 MIPS. With a 50 MHz clock, performance is 50 MIPS peak and 40 MIPS sustained.

LR4102 Features

Components

- R3000 MIPS CPU executes MIPS II and MIPS16 instructions
- 32-bit FBus, a fast demultiplexed multimaster bus, with built in control of:
 - RAM, EPROM, or similar simple devices
 - DRAM and SDRAM
 - General-purpose I/O
- Two 32-bit Timers
- FastMDU
 - 4/5 cycle multiply and accumulate (32-bit to 64-bit)
 - 34/35 cycle divide
- BBCC with four writeback buffers included
- MMU with 64-entry TLB RAM
- EJTAG Version 2.0.0:
 - Nonintrusive debug
 - Real-time PC trace
 - Hardware breakpoints
- SerialICE-1 Port included for backward compatibility with other TinyRISC designs
- JTAG Boundary Scan
- On-Chip Memory (OCM), 1 Kbyte

Caches

- 16 Kbytes of two-way set-associative I-Cache
- 8 Kbytes of direct-mapped D-Cache

- Clock module with integrated PLL and programmable clock speeds

Technology

- LSI Logic G11 Technology
 - 0.18 μ L_{eff} (0.25 μ drawn)
 - 2.5 or 1.8 V operation

Performance and Compatibility

- Clock speed is 85 MHz at 2.5 V (85 MIPS peak and estimated 68 MIPS sustained)
- Low power mode allows LR4102 to use minimal power when idle
- Compatible with the full range of MIPS and third-party software development tools
- 16-bit and 32-bit code can be mixed arbitrarily with full support on a subroutine basis
- All instructions execute in one cycle except for Load and Store, Move To Coprocessor, and Move From Coprocessor, which execute in two cycles, and MDU instructions, which execute in several cycles

Block Diagram

This section provides short descriptions of the major components of the LR4102, as shown in [Figure 1](#).

The CPU performs all arithmetic, logical, shift, and address calculations. The CPU supports EJTAG debug and is closely coupled with the FastMDU. The FastMDU calculates all multiply and divide operations for the LR4102, and provides 4/5 cycle multiply and accumulate operations (32 bit to 64 bit), 34/35 cycle divide, saturated math, and overflow indication.

The memory management unit (MMU) translates virtual addresses from the CPU into physical addresses and includes a 64-entry translation look-aside buffer (TLB) RAM.

The BIU and cache controller (BBCC) provides an internal bus interface and connects the CPU to the caches. For the caches, the LR4102 contains 16 Kbytes of two-way set-associative I-Cache and 8 Kbytes of direct-mapped D-Cache. Four Write Buffers are integrated with the BBCC in the LR4102 design.

The 32-bit FBusMACRO (FBM) controls the FBus, a dedicated, multimaster bus that connects off-chip logic with the LR4102. The FBus allows seamless LR4102 connection to a variety of devices, including EPROM, FLASH, RAM, DRAM, SDRAM, and general-purpose I/O pins. The FBus also supports burst read (one cycle) and write, built-in arbitration for an external FBus master, and snooping of external write accesses to memory. Internally, the FBusMACRO interfaces mainly with the BBCC module.

Each 32-bit Timer can count down from a preloaded value, roll over or stop at zero, generate an interrupt on zero, or act as bus watchdog. The CPU can program either of the two internal 32-bit timers.

The LR4102 includes 1 Kbyte of on-chip memory (OCM).

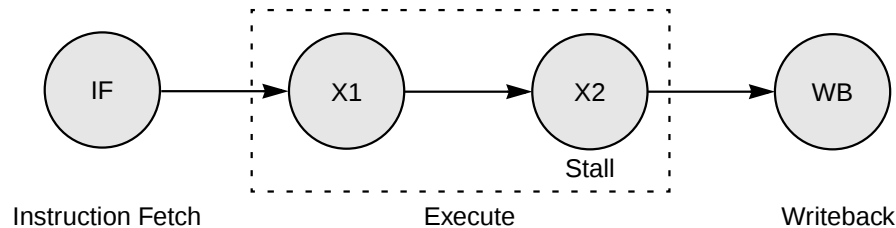
The Clock Controller steps CPU clock speed up or down, and can stop the internal LR4102 clock altogether. The LR4102 also supports a low power mode. The LR4102 Clock Controller is designed to support a crystal or canned oscillator, and has an on-chip PLL for frequency multiplication.

The EJTAG with PC Trace output provides real-time program counter (PC) trace and breakpoint capability in an EJTAG compatible debug design. PC trace outputs are provided through the Extended Debug MACRO for complete and accurate chip debug. A SerialICE-1 Port (UART) is also included in the LR4102 to provide backward compatibility with previous TinyRISC designs.

Pipeline Architecture

The LR4102 implements a 3-stage pipeline (Fetch, Execute, and Writeback) that uses a single adder for the ALU, the data address, and the instruction address. Sharing a single adder dramatically reduces the circuitry required to implement the microprocessor, and eliminates pipeline registers and bypass logic. The LR4102 design does not require a load delay slot. [Figure 2](#) shows the microprocessor CPU 3-stage pipeline.

Figure 2 LR4102 CPU Pipeline with X2 Stall Cycle



The execution of a single LR4102 instruction consists of the following three pipeline stages:

1. Instruction Fetch – The LR4102 fetches the instruction (IF), and if necessary, decompresses a 16-bit instruction into a 32-bit instruction.
2. Execute – The LR4102 executes all ALU instructions, resolves conditional branches, and calculates load and store addresses (X1). The CPU then transfers load or store data from external memory or cache and performs move to/from coprocessor operations in a second execute (stall) cycle (X2), which is only inserted when required.
3. Writeback – The LR4102 writes the results into the register file (WB).

Instruction Set Summary

[Table 1](#) summarizes the 32-bit instruction set for the LR4102, and [Table 2](#) lists the unimplemented MIPS II instructions. [Table 3](#) provides a summary of the LR4102 MIPS16 instruction set.

Table 1 LR4102 32-Bit Instruction Set Summary

Load and Store Instructions			
LB	Load Byte	SB	Store Byte
LBU	Load Byte Unsigned	SH	Store Halfword
LH	Load Halfword	SW	Store Word
LHU	Load Halfword Unsigned	SWL	Store Word Left
LW	Load Word	SWR	Store Word Right
LWL	Load Word Left	SYNC	Synchronize (load/store synchronization)
LWR	Load Word Right	–	–
Arithmetic Instructions: ALU Immediate			
ADDI	Add Immediate	ORI	OR Immediate
ADDIU	Add Immediate Unsigned	SLTI	Set on Less Than Immediate
ANDI	AND Immediate	SLTIU	Set on Less Than Immediate Unsigned
LUI	Load Upper Immediate	XORI	Exclusive OR Immediate
Arithmetic Instructions: Three-Operand, Register-Type			
ADD	Add	SLT	Set on Less Than
ADDU	Add Unsigned	SLTU	Set on Less Than Unsigned
AND	Logical AND	SUB	Subtract
NOR	Logical NOR	SUBU	Subtract Unsigned
OR	Logical OR	XOR	Logical Exclusive OR
(Sheet 1 of 4)			

Table 1 LR4102 32-Bit Instruction Set Summary (Cont.)

Shift Instructions			
SLL	Shift Left Logical	SRAV	Shift Right Arithmetic Variable
SLLV	Shift Left Logical Variable	SRL	Shift Right Logical
SRA	Shift Right Arithmetic	SRLV	Shift Right Logical Variable
Multiply/Divide Instructions			
DIV	Divide	MSUBU ¹	Multiply Subtract Unsigned
DIVU	Divide Unsigned	MTHI	Move To HI
MADD ¹	Multiply Add	MTLO	Move To LO
MADDU ¹	Multiply Add Unsigned	MUL ¹	Three-Operand Multiply
MFHI	Move From HI	MULT	Multiply
MFLO	Move From LO	MULTU	Multiply Unsigned
MSUB ¹	Multiply Subtract	—	—
Jump and Branch Instructions			
BCzF	Branch on Coprocessor z False	BLTZAL	Branch on Less Than Zero and Link
BCzT	Branch on Coprocessor z True	BNE	Branch on Not Equal
BEQ	Branch on Equal	J	Jump
BGEZ	Branch on Greater Than or Equal to Zero	JAL	Jump and Link
BGEZAL	Branch on Greater Than or Equal to Zero and Link	JALR	Jump and Link Register
BGTZ	Branch on Greater Than Zero	JALX	Jump and Link Exchange
BLEZ	Branch on Less Than or Equal to Zero	JR	Jump Register
BLTZ	Branch on Less Than Zero	BGTZL	Branch on Greater Than Zero Likely
BCzFL	Branch on Coprocessor z False Likely	BLEZL	Branch on Less Than or Equal to Zero Likely
(Sheet 2 of 4)			

Table 1 LR4102 32-Bit Instruction Set Summary (Cont.)

Jump and Branch Instructions (Cont.)			
BCzTL	Branch on Coprocessor z True Likely	BLTZALL	Branch on Less Than Zero and Link Likely
BEQL	Branch on Equal Likely	BLTZL	Branch on Less Than Zero Likely
BGEZALL	Branch on Greater Than or Equal to Zero and Link Likely	BNEL	Branch on Not Equal Likely
BGEZL	Branch on Greater Than or Equal to Zero Likely	–	–
Coprocessor Instructions			
BCzF	Branch on Coprocessor z False	MTCz	Move to Coprocessor z
BCzT	Branch on Coprocessor z True	MFCz	Move from Coprocessor z
COPz	Coprocessor Operation	SWCz	Store Word from Coprocessor z (z ≠ 0)
CTCz	Move Control to Coprocessor z	BCzFL	Branch on Coprocessor z False Likely
CFCz	Move Control from Coprocessor z	BCzTL	Branch on Coprocessor z True Likely
LWCz	Load Word to Coprocessor z (z ≠ 0)	–	–
System Control Coprocessor (CP0)			
MFC0	Move from CP0	RFE	Restore from Exception
MTC0	Move to CP0	WAITI ¹	Wait for Interrupt
TLBR	Read Indexed TLB Entry	TLBWI	Write Indexed TLB Entry
TLBWR	Write Random TLB Entry	TLBP	Probe TLB for Matching Entry
Special Control Instructions			
BREAK	Breakpoint	SYSCALL	System Call
Trap Instructions			
TEQ	Trap if Equal	TLT	Trap if Less Than
(Sheet 3 of 4)			

Table 1 LR4102 32-Bit Instruction Set Summary (Cont.)

Trap Instructions (Cont.)			
TEQI	Trap if Equal Immediate	TLTI	Trap if Less Than Immediate
TGE	Trap if Greater Than or Equal	TLTIU	Trap if Less Than Immediate Unsigned
TGEI	Trap if Greater Than or Equal Immediate	TLTU	Trap if Less Than Unsigned
TGEIU	Trap if Greater Than or Equal Immediate Unsigned	TNE	Trap if Not Equal
TGEU	Trap if Greater Than or Equal Unsigned	TNEI	Trap If Not Equal Immediate
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint	DERET	Debug Exception Return
(Sheet 4 of 4)			

1. LR4102/EZ4102-specific instruction.

Table 2 Unimplemented Instructions Summary

Unimplemented MIPS II Instructions			
COP1	All floating-point instructions	ERET	Exception Return
LL	Load Linked Word	LDCz	Load Doubleword to Coprocessor
SC	Store Conditional Word	SDCz	Store Doubleword to Coprocessor

Table 3 LR4102 16-Bit Instruction Set Summary

Load and Store Instructions			
LB ¹	Load Byte	LW ¹	Load Word
LBU ¹	Load Byte Unsigned	SB ¹	Store Byte
LH ¹	Load Halfword	SH ¹	Store Halfword
LHU ¹	Load Halfword Unsigned	SW ¹	Store Word
Arithmetic Instructions: ALU Immediate			
LI ¹	Load Immediate	SLTIU ¹	Set on Less Than Immediate Unsigned
ADDIU ¹	Add Immediate Unsigned	CMPI ¹	Compare Immediate
SLTI ¹	Set on Less Than Immediate	–	–
Arithmetic Instructions: Two/Three Operand, Register Type			
ADDU	Add Unsigned	AND	Logical AND
SUBU	Subtract Unsigned	OR	Logical OR
SLT	Set on Less Than	XOR	Exclusive Logical OR
SLTU	Set on Less Than Unsigned	NOT	Logical NOT
CMP	Compare	MOVE	Move
NEG	Negate	–	–
Shift Instructions			
SLL ¹	Shift Left Logical	SLLV	Shift Left Logical Variable
SRL ¹	Shift Right Logical	SRLV	Shift Right Logical Variable
SRA ¹	Shift Right Arithmetic	SRAV	Shift Right Arithmetic Variable
(Sheet 1 of 2)			

Table 3 LR4102 16-Bit Instruction Set Summary (Cont.)

Multiply/Divide Instructions			
MULT	Multiply	DIVU	Divide Unsigned
MULTU	Multiply Unsigned	MFHI	Move From HI
DIV	Divide	MFLO	Move From LO
Jump and Branch Instructions			
JAL	Jump and Link	BNEZ ¹	Branch on Not Equal to Zero
JALX	Jump and Link Exchange	BTEQZ ¹	Branch on T Equal to Zero
JR	Jump Register	BTNEZ ¹	Branch on T Not Equal to Zero
JALR	Jump and Link Register	B ¹	Branch Unconditional
BEQZ ¹	Branch on Equal to Zero	–	–
Special Instructions			
EXTEND	Extend	BREAK	Breakpoint
EJTAG Debug Instructions			
SDBBP	Software Debug Breakpoint	–	–
(Sheet 2 of 2)			

1. Extensible instruction; for details, please see the documentation on the MIPS16 Application Specific Extension to the MIPS ISA, which is available from MIPS Technologies Incorporated.

LR4102 Register Map

Table 4 shows the LR4102 microprocessor register memory map.

Table 4 LR4102 Register Memory Map

Register Name	Physical Address	Description
System configuration registers in BBCC		
SCR1	0x1FFF.0000	System Configuration Register 1
SCR2	0x1FFF.0004	System Configuration Register 2
SCR3	0x1FFF.0008	System Configuration Register 3
Timer registers		
T0ICR	0x1FFF.0100	Timer 0 Initial Count Register
T0CCR	0x1FFF.0104	Timer 0 Current Count Register
T1ICR	0x1FFF.0108	Timer 1 Initial Count Register
T1CCR	0x1FFF.010C	Timer 1 Current Count Register
TMR	0x1FFF.0110	Mode Register
TISR	0x1FFF.0114	Interrupt Status Register
SerialICE-1 Port (UART) registers		
RxStatus	0x1FFF.0200	Receive (Rx) Status Register (Reading)
RxSetup	0x1FFF.0200	Receive (Rx) Setup Register (Writing)
RxData	0x1FFF.0204	Receive (Rx) Data Register
TxStatus	0x1FFF.0208	Transmit (Tx) Status Register
TxData	0x1FFF.020C	Transmit (Tx) Data Register
Reserved registers		
Reserved	0x1FFF.0300–.03FF	Reserved for LSI Logic use
FBus registers		
FACFG0	0x1FFF.0400	Configuration for address range 0
FACFG1	0x1FFF.0404	Configuration for address range 1
(Sheet 1 of 2)		

Table 4 LR4102 Register Memory Map (Cont.)

Register Name	Physical Address	Description
FBus registers (Cont.)		
FACFG2	0x1FFF.0408	Configuration for address range 2
FACFG3	0x1FFF.040C	Configuration for address range 3
FACFG4	0x1FFF.0410	Configuration for address range 4
FACFG5	0x1FFF.0414	Configuration for address range 5
FBUSTA	0x1FFF.0418	Bus turnaround register for address range 0–5
FACMP0	0x1FFF.0440	Address compare register address range 0
FACMP1	0x1FFF.0444	Address compare register address range 1
FACMP2	0x1FFF.0448	Address compare register address range 2
FACMP3	0x1FFF.044C	Address compare register address range 3
FACMP4	0x1FFF.0450	Address compare register address range 4
FACMP5	0x1FFF.0454	Address compare register address range 5
FBUSCMP	0x1FFF.0470	Address compare register for FBus address range.
FBUSAC	0x1FFF.0474	Address compare register for FBus I/O, memory, and configuration address range.
FBUSCFG	0x1FFF.0480	Configuration for FBus when accessing outside programmable address range 0–5.
FSDRAM	0x1FFF.0490	Configuration for external EDO (S)DRAM
FDRAMT	0x1FFF.0494	Timing parameters for external EDO DRAM
FSDRAMT	0x1FFF.0498	Timing parameters for external SDRAM
FGPCFG	0x1FFF.04C0	Configuration for General-Purpose I/O
FGPOUTPUT	0x1FFF.04C4	Output value for General-Purpose Outputs
FGPINPUT	0x1FFF.04C8	Input value for General-Purpose Inputs
Reserved registers		
Reserved	0x1FFF.0500–.06FF	Reserved for LSI Logic use
On Chip Memory (OCM), 1 Kbytes		
OCM area	0x1FFF.8000–.83FF	On chip memory. Placed on CBus, 1 cycle access
(Sheet 2 of 2)		

Signal Descriptions

The signals are described in alphabetical order by mnemonic. Each signal definition contains the mnemonic and the full signal name. Mnemonics for signals that are active LOW end in an “N”, and mnemonics for signals that are active HIGH end in a “P.” In the descriptions that follow, the verb *assert* means to drive active. The verb *deassert* means to drive inactive.

The LR4102 signals are divided into the following groups:

- Control Signals
- Clocking Interface
- Timer Interface
- SerialICE-1 Interface
- EJTAG Interface and JTAG boundary scan signals
- PC Trace Output
- FBus Interface
- Test Interface
- Power Lines

[Table 5](#) lists all of the LR4102 signals, grouped by interface.

Table 5 **LR4102 Signal List**

Signal Group	Mnemonic Name	Functional Description	I/O
Control Signals	RESETN	Asynchronous system reset	Input
	BIG_ENDIANP	Big/Little Endian select	Input
	CWAITIP	Wait for interrupt (low power mode)	Output
	INTP[5:0]	Condition/Interrupt	Input
	DEBUGMP	Debug mode	Output
(Sheet 1 of 4)			

Table 5 LR4102 Signal List (Cont.)

Signal Group	Mnemonic Name	Functional Description	I/O
Clocking Interface	EXTAL	Input from crystal/Oscillator	Input
	XTAL	Output to crystal	Output
	PBCLKP	FAPI clock	Output
	SDCLKP	SDRAM clock	Output
	DIVC[1:0]	The divide value for DIV C upon reset	Input
	DIVA[1:0]	The divide value for DIV A	Input
	SELECT_PLLN	Control clock source MUX	Input
	RESET_OUTN	Delayed reset signal for FAPI bus	Output
	PLLENP	Enable PLL	Input
	PLLENARSTP	Enable PLL auto reset	Input
Timer Interface	T0_OUTN	Timer 0 output	Output
	T1_OUTN	Timer 1 output	Output
SerialICE-1 Interface	ICECLKP	SerialICE-1 Port clock	Input
	ICERXP	SerialICE-1 Port receive	Input
	ICETXP	SerialICE-1 Port transmit	Output
EJTAG Interface and JTAG boundary scan signals	TCK	EJTAG Interface clock	Input
	TMS	EJTAG Interface mode select	Input
	TDI_DINT	EJTAG Interface data in/Debug interrupt	Input
	TDO_TPC	EJTAG Interface data out/PC out	Output
	TRST	EJTAG Interface reset	Input
PC Trace Output	DCLK	PC Trace clock output	Output
	PCST1[2:0]	PC Trace status set 1 [2:0]	Output
	TPC[4:2]	PC Trace PC out [4:2]	Output
(Sheet 2 of 4)			

Table 5 LR4102 Signal List (Cont.)

Signal Group	Mnemonic Name	Functional Description	I/O
FBus Interface	CBEN[3:0]	Command/byte enable	Bidirectional
	DEVSELN	Device select	Bidirectional
	FADDRP[28:0]	Demultiplexed address bus	Output
	FADP[31:0]	Multiplexed address/Data bus	Bidirectional
	FALEP	Address latch enable	Output
	FRAMEN	Cycle frame indicating a bus transaction is beginning	Bidirectional
	GNTN	Grant the FBus	Output
	GP[5:0]	General-purpose pins	Bidirectional
	GPIO[3:0]	General-purpose I/O pins	Bidirectional
	GPRDN	General-purpose read enable	Output
	GPWEN[3:0]	General-purpose write byte enable	Output
	IRDYN	Initiator ready	Bidirectional
	REQN	Request FBus	Input
	SD_CASN0_DMP0	DRAM CAS0 or SDRAM data mask 0	Output
	SD_CASN1_DMP1	DRAM CAS1 or SDRAM data mask 1	Output
	SD_CASN2_DMP2	DRAM CAS2 or SDRAM data mask 2	Output
	SD_CASN3_DMP3	DRAM CAS3 or SDRAM data mask 3	Output
	SD_OEN_CASN	DRAM output enable or SDRAM CAS	Output
	SDONEP	Snooping done	Output
	SD_RASN	SDRAM RAS	Output
	SD_RASN0_CSN0	DRAM RAS bank 0 or SDRAM CAS0	Output
	SD_RASN1_CSN1	DRAM RAS bank 1 or SDRAM CAS1	Output
	SD_WEN_WEN	DRAM write enable or SDRAM write enable	Output
	STOPN	Stop transaction	Bidirectional
(Sheet 3 of 4)			

Table 5 LR4102 Signal List (Cont.)

Signal Group	Mnemonic Name	Functional Description	I/O
FBus Interface	TRDYN	Target ready	Bidirectional
Test Interface	CSHTSTP	Cache test enable	Input
	IDDTN	IDD test	Input
	JTAGALSOP	JTAG controller present	Input
	PMON_OUTP	Process monitor output	Output
	SCAN_ENABLEP	Enable scan chain loading	Input
	SCAN__INP	Input to the scan chain	Input
	SCAN_MODEP	Enable scan testing	Input
	SCAN_OUTP	Output from the scan chain	Output
	SCAN_RAMWEP	RAM write enable	Input
	SELECT_CKOUT1N	Select PLL test	Input
	TN	3-state all LR4102 output and bidirectional signals	Input
Power Lines	VDD, VDD2	V _{DD} for CPU core and oscillator 2.5 V or 1.8 V	Power
	VDD4	V _{DD} for I/O 3.3 V	Power
	PLLVDD1	V _{DD} to PLL 2.5 V. Requires V _{DD} CPU core and oscillator at 2.5 V, since PLL must be disabled for V _{DD} CPU core and clock at 1.8 V	Power
	VSS, VSS2, VSS4, PLLVSS1	V _{SS} for CPU core, clock, I/O and PLL	Power
(Sheet 4 of 4)			

LR4102 Specifications

This section specifies the LR4102 electrical characteristics and includes the following subsections:

- “AC Timing”
- “Electrical Requirements”

AC Timing

This section describes the AC timing characteristics of the LR4102 interface. Figures 3 and 4 show the EXTAL and TCK clocks. Figures 5 through 9 illustrate the input and output timing relationship with respect to various clocks (PBCLKP, SDCLKP, and DCLKP). Tables 6 through 14 list the minimum and maximum input and output values for the LR4102 interface signals. Note that all output signals have a 65 pF load.

Figure 3 **EXTAL Clock Timing**

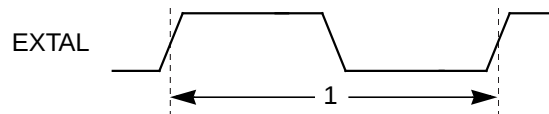


Figure 4 **TCK Clock Timing**

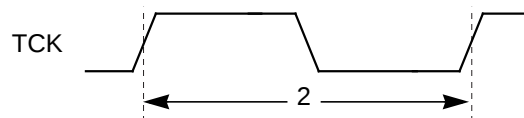
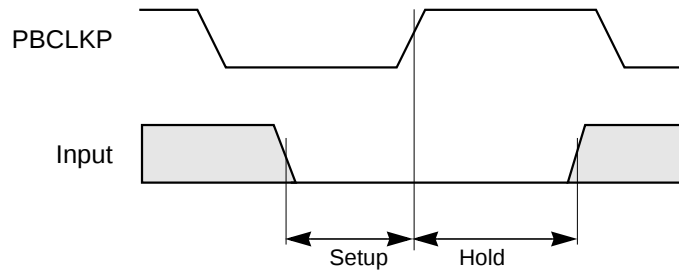


Figure 5 Input Timing with Respect to PBCLKP



Note: PBCLKP equals the system clock (PCLKP) when the DIV C value in the Clock module is 0b01. DIV C = 0b01 is used to show timing for signals related to the system clock. The setting of DIV C only affects PBCLKP and the timing for signals related to the FAPI clock (PBCLKP).

Figure 6 Output Timing with Respect to PBCLKP

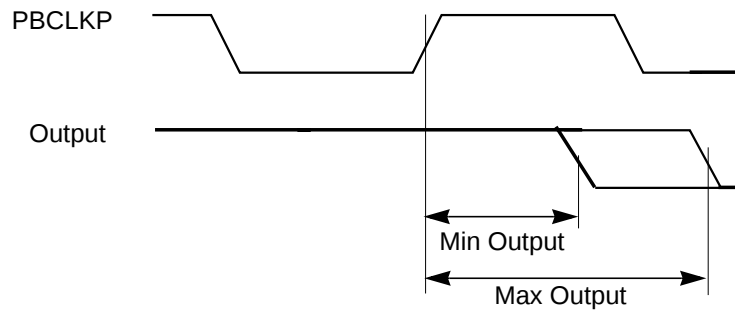


Figure 7 Input Timing with Respect to SDCLKP

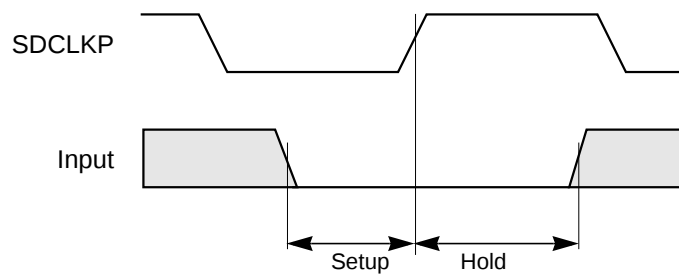


Figure 8 Output Timing with Respect to SDCLKP

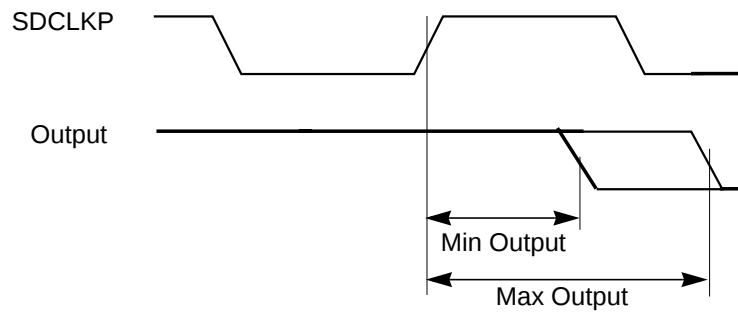


Figure 9 Output Timing with Respect to DCLK

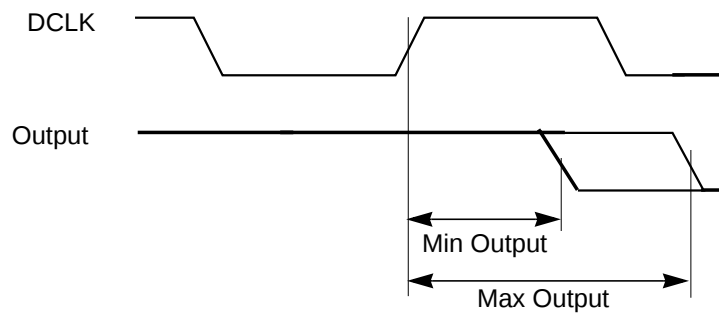


Table 6 EXTAL Input Timing

Parameter	Input Signal	Clock Period	Frequency		
			Min	Max	Units
1	EXTAL	5.88 ns	–	170	MHz

Table 7 TCK Input Timing

Parameter	Input Signal	Clock Period	Frequency		
			Min	Max	Units
2	TCK	11.76 ns	–	85	MHz

Table 8 AC Input Timing with respect to rising edge of PBCLKP¹

Input Signal	Setup	Hold	Units
CBEN[3:0]	7.2	1.4	ns
DEVSELN	4.7	2.2	ns
FADP[31:0] ³	2.9	2.7	ns
FRAMEN	7.4	2.2	ns
GP[5:0] ²	2.8	2.6	ns
GPIO[3:0] ²	1.8	2.8	ns
IRDYN	7.5	1.9	ns
REQN	3.5	1.5	ns
STOPN	4.7	1.7	ns
TRDYN	4.6	2.0	ns

1. With 65 pF load
2. This signal is related to the system clock, but not to the FAPI bus (see [Figure 5](#) note).
3. This signal is related to both the system clock and the FAPI bus (see [Figure 5](#) note).

Table 9 AC Input Timing with respect to rising edge of SDCLKP¹

Input Signal	Setup	Hold	Units
FADP[31:0]	2.0	3.4	ns

1. With 65 pF load.

Table 10 AC Input Timing with respect to rising edge of TCK

Input	Setup	Hold	Units
TDI_DINT	1.9	1.1	ns
TMS	1.6	0.7	ns

Table 11 AC Output Timing with respect to rising edge of PBCLKP¹

Output Signal ¹	Min	Max	Units
CBEN[3:0]	1.0	8.0	ns
CWAITIP ²	2.8	8.8	ns
DEBUGMP	3.1	9.3	ns
DEVSELN	0.8	7.2	ns
FADDRP[28:0] ²	1.3	6.2	ns
FADP[31:0] ³	0.8	7.4	ns
FALEP	1.6	6.1	ns
FRAMEN	1.0	7.5	ns
GNTN	2.3	7.0	ns
GP[5:0] ²	0.4	7.0	ns
GPIO[3:0] ²	0.3	6.8	ns
GPRDN ²	1.7	5.8	ns
GPWEN[3:0] ²	1.4	6.2	ns
IRDYN	1.0	7.5	ns
RESET_OUTN ²	2.1	7.3	ns
SD_CASN[3:0]_DMP[3:0] ²	1.3	6.0	ns
SD_OEN_CASN ²	1.4	5.9	ns
SDONEP	1.8	6.4	ns
SD_RASN[1:0]_CSN[1:0] ²	1.3	5.9	ns
SD_WEN_WEN ²	1.4	5.7	ns
STOPN	0.8	7.2	ns
T0_OUTN ²	2.6	8.8	ns
(Sheet 1 of 2)			

Table 11 AC Output Timing with respect to rising edge of PBCLKP¹ (Cont.)

Output Signal ¹	Min	Max	Units
T1_OUTN ²	2.7	8.9	ns
TRDYN	0.8	7.2	ns
(Sheet 2 of 2)			

1. With 65 pF load
2. This signal is related to the system clock, but not to the FAPI bus (see [Figure 5](#) note).
3. This signal is related to both the system clock and the FAPI bus (see [Figure 5](#) note).

Table 12 AC Output Timing with respect to rising edge of SDCLKP¹

Output Signal ¹	Min	Max	Units
FADDRP[28:0]	1.7	6.9	ns
FADP[31:0]	1.2	8.3	ns
SD_CASN[3:0]_DMP[3:0]	1.7	6.9	ns
SD_OEN_CASN	1.8	6.6	ns
SD_RASN	1.7	6.4	ns
SD_RASN[1:0]_CSN[1:0]	1.7	6.8	ns
SD_WEN_WEN	1.8	6.6	ns

1. With 65 pF load.

Table 13 AC Output Timing with respect to falling edge of TCK

Output Signal ¹	Min	Max	Units
TDO_TPC	2.1	8.9	ns

1. With 65 pF load

Table 14 EZ4102 AC Output Timing with respect to rising edge of DCLK¹

Output Signal ¹	Min	Max	Units
PCST1[2:0]	–2.9	1.9	ns
TDO_TPC	–3.2	1.8	ns
TPC[4:2]	–3.2	2.0	ns

1. With 65 pF load.

Note: there is no setup/hold time requirements for the interrupt pins, INTP[5:0], because they are synchronized internally within the LR4102.

Electrical Requirements

This section contains the electrical parameters for the TinyRISC LR4102 Microprocessor in the following tables:

- [Table 15](#) lists the absolute maximum ratings
- [Table 16](#) defines the recommended operating supply voltage and temperature
- [Table 17](#) shows the pin capacitance
- [Table 18](#) lists the DC characteristics

Table 15 Absolute Maximum Rating¹

Symbol	Parameter	Limits	Unit
$V_{DD/DD2}$	DC Supply Voltage ² , core and oscillator	–0.3 to 3.1	V
V_{DD4}	3.3 V DC Supply Voltage ² , I/O	–0.3 to 3.9	V
V_{IN}	3.3 V Drive Input Voltage ²	–1.0 to $V_{DD4} + 0.3$	V
T_{STG}	Storage Temperature Range (Plastic)	–40 to 125	°C

1. Exceeding these values may cause damage to the LR4102.

2. Referenced to V_{SS} .

Table 16 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
$V_{DD/DD2}$	DC Supply Voltage ¹ at V_{DD}/V_{DD2} nominal 1.8 V at V_{DD}/V_{DD2} nominal 2.5 V	1.71 to 1.89 2.38 to 2.63	V V
T_A	Ambient Temperature	0 to 70	°C

1. Referenced to V_{SS} .

Table 17 Capacitance

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Capacitance	4.6	–	5.2	pF
C_{OUT}	Output Capacitance	4.6	–	5.2	pF

Table 18 DC Characteristics

Symbol	Parameter	Condition ¹	Min	Typ	Max	Units
V_{DD4}	Supply Voltage, I/O	–	3.0	3.3	3.6	V
V_{IL}	Voltage Input Low	–	–0.5	–	0.8	V
V_{IH}	Voltage Input High	–	2.0	–	$V_{DD4} + 0.3$	V
I_{IL}	Current Input Leakage Inputs with no Pull-up/-down Resistor Inputs with Pull-down Resistor Inputs with Pull-up Resistor	$V_{IN} = V_{SS}/V_{DD4}$ $V_{IN} = V_{DD4}$ $V_{IN} = V_{SS}$	–10 35 –35	± 1 115 –115	10 222 –214	μA μA μA
V_{OL}	Voltage Output Low	–	–	0.2	0.4	V
V_{OH}	Voltage Output High	–	2.4	–	V_{DD4}	V
I_{DD}	Quiescent Supply Current	–	<1	20	100	μA
I_{CC}	Dynamic Supply Current	–	–	170	–	mA
I_{OZ}	Z-state Output Leakage Current	$V_{OH} = V_{SS}/V_{DD4}$	–10	± 1	10	μA

1. Specified at V_{DD4} equals $3.3\text{ V} \pm 5\%$ at ambient temperature over the specified range.

Pinouts

Table 19 provides an alphabetical pinout list for the LR4102 256-pin PBGA.

Table 19 LR4102 256-pin PBGA Pinout

Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball
BIG_ENDIANP	E18	FADP7	E20	INTP4	A11	VDD2	U3
CBEN0	A20	FADP8	F20	INTP5	A10	VDD2	V11
CBEN1	F18	FADP9	F19	IRDYN	Y10	VDD2	U11
CBEN2	Y9	FADP10	G20	JTAGALSOP	C9	VDD2	U16
CBEN3	W5	FADP11	G19	PBCLKP	Y12	VDD2	V17
CWAITIP1	D10	FADP12	H20	PCST10	T3	VDD2	J 17
CSHTSTP	B18	FADP13	H19	PCST11	R3	VDD2	E17
DCLK	T1	FADP14	J20	PCST12	P3	VDD2	D18
DEBUGMP	P4	FADP15	J19	PLLENARSTP	G18	VDD2	D5
DEVSELN	Y11	FADP16	W9	PLLENP	H18	VDD2	C4
DIVA0	G17	FADP17	Y8	PLLVD1	A17	VDD4	D6
DIVA1	K17	FADP18	W8	PLLVS1	A18	VDD4	D11
DIVC0	K18	FADP19	Y7	PMON_OUTP	B11	VDD4	D15
DIVC1	L18	FADP20	W7	REQN	V1	VDD4	F4
EXTAL	B16	FADP21	Y6	RESET_OUTN	A14	VDD4	F17
FADDRP0	K20	FADP22	W6	RESETN	A15	VDD4	K4
FADDRP1	K19	FADP23	Y5	SCAN_ENABLEP	C17	VDD4	L17
FADDRP2	L20	FADP24	Y4	SCAN_INP	J18	VDD4	R4
FADDRP3	L19	FADP25	W4	SCAN_MODEP	C14	VDD4	R17
FADDRP4	M20	FADP26	Y3	SCAN_OUTP	B17	VDD4	U6
FADDRP5	M19	FADP27	W3	SCAN_RAMWEP	D16	VDD4	U10
FADDRP6	N20	FADP28	Y2	SD_CASN0_DMP0	N18	VDD4	U15
FADDRP7	N19	FADP29	W2	SD_CASN1_DMP1	P17	VSS	A1
FADDRP8	P20	FADP30	Y1	SD_CASN2_DMP2	Y14	VSS	C15
FADDRP9	P19	FADP31	W1	SD_CASN3_DMP3	W14	VSS	C16
FADDRP10	R20	FALEP	Y13	SD_OEN_CASN	M18	VSS2	D3
FADDRP11	R19	FRAMEN	W10	SD_RASN	R18	VSS2	E4
FADDRP12	T20	GNTN	V2	SD_RASN0_CSN0	P18	VSS2	M3
FADDRP13	T19	GP0	V15	SD_RASN1_CSN1	W15	VSS2	M4
FADDRP14	U20	GP1	U14	SD_WEN_WEN	M17	VSS2	V4
FADDRP15	U19	GP2	V14	SDCLKP	Y15	VSS2	U5
FADDRP16	V20	GP3	V13	SDONEP	W13	VSS2	V12
FADDRP17	V19	GP4	U7	SELECT_CKOUT1N	B14	VSS2	U12
FADDRP18	W20	GP5	V6	SELECT_PLLN	B15	VSS2	U18
FADDRP19	Y20	GPIO0	T18	STOPN	W12	VSS2	T17
FADDRP20	W19	GPIO1	V16	T0_OUTN	C10	VSS2	C18
FADDRP21	Y19	GPIO2	V5	T1_OUTN	B10	VSS2	A19
FADDRP22	V18	GPIO3	V3	TCK	U1	VSS2	D9
FADDRP23	Y18	GPRDN	U9	TDI_DINT	T2	VSS4	D4
FADDRP24	W18	GPWEN0	V10	TDQ_TPC	R2	VSS4	D8
FADDRP25	Y17	GPWEN1	V9	TMS	U2	VSS4	D13
FADDRP26	W17	GPWEN2	V8	TN	C11	VSS4	D17
FADDRP27	Y16	GPWEN3	V7	TPC2	R1	VSS4	H4
FADDRP28	W16	ICECLKP	A8	TPC3	P2	VSS4	H17
FADP0	B19	ICERXP	B9	TPC4	P1	VSS4	N4
FADP1	B20	ICETXP	A9	TRDYN	W11	VSS4	N17
FADP2	C19	IDDTN	D12	TRST	N3	VSS4	U4
FADP3	C20	INTP0	A13	VDD	D14	VSS4	U8
FADP4	D19	INTP1	B13	VDD2	L3	VSS4	U13
FADP5	D20	INTP2	C13	VDD2	L4	VSS4	U17
FADP6	E19	INTP3	A12	VDD2	T4	XTAL	A16

Input/Output Drivers

Table 20 lists the I/O driver types.

Table 20 I/O Driver Types

Signal Name	I/O Driver Type	Description
BIG_ENDIANP	IBUFULS	Input buffer with pull-up
CBEN[3:0]	BD12CLS	12 mA Bi-directional buffer
CSHTSTP	IBUFULS	Input buffer with pull-up
CWAITIP	BT8LS	8 mA output buffer
DCLK	BT24LS	24 mA output buffer
DEBUGMP	BT8LS	8 mA output buffer
DEVSELN	BD12CULS	12 mA Bi-directional buffer with pull-up
DIVA[1:0]	IBUFLS	Input buffer
DIVC[1:0]	IBUFLS	Input buffer
EXTAL, XTAL	OSCIM	Oscillator
FADDRP[28:0]	BT12LS	12 mA output buffer
FADP[31:0]	BD12CLS	12 mA Bi-directional buffer
FALEP	BT12LS	12 mA output buffer
FRAMEN	BD12CULS	12 mA Bi-directional buffer with pull-up
GNTN	BT12LS	12 mA output buffer
GP[5:0]	BD12SCUHO	12 mA Bi-directional buffer with Schmidt trigger input and pull-up
GPIO[3:0]	BD12SCUHO	12 mA Bi-directional buffer with Schmidt trigger input and pull-up
GPRDN	BT12LS	12 mA output buffer
GPWEN[3:0]	BT12LS	12 mA output buffer
ICECLKP	SCHMITCUHO	Schmidt trigger input with pull-up
(Sheet 1 of 3)		

Table 20 I/O Driver Types (Cont.)

ICERXP	SCHMITCUHO	Schmidt trigger input with pull-up
ICETXP	BT6LS	6 mA output buffer
IDDTN	IIDDTNLS	IDD test input buffer
INTP[5:0]	IBUFULS	Input buffer with pull-up
IRDYN	BD12CULS	12 mA Bi-directional buffer with pull-up
JTAGALSOP	IBUFULS	Input buffer with pull-up
PBCLKP	BT8LS	8 mA output buffer
PCST[12:10]	BD8CDLS	8 mA Bi-directional buffer with pull-down
PLLENARSTP	IBUFLS	Input buffer
PLLENP	IBUFLS	Input buffer
PLLVDD1	PLLVDD	PLL Vdd
PLLVSS1	PLLVSS	PLL Vss
PMON_OUTP	PROCMONLS	PROCMON test output driver
REQN	IBUFULS	Input buffer with pull-up
RESET_OUTN	BT8LS	8 mA output buffer
RESETN	IBUFULS	Input buffer with pull-up
SCAN_ENABLEP	IBUFLS	Input buffer
SCAN_INP	IBUFLS	Input buffer
SCAN_MODEP	IBUFDLS	Input buffer with pull-down
SCAN_OUTP	BT8LS	8 mA output buffer
SCAN_RAMWEP	SCHMITCHO	Schmidt trigger input buffer
SD_CASN0_DMP0	BT12LS	12 mA output buffer
SD_CASN1_DMP1	BT12LS	12 mA output buffer
SD_CASN2_DMP2	BT12LS	12 mA output buffer
SD_CASN3_DMP3	BT12LS	12 mA output buffer
(Sheet 2 of 3)		

Table 20 I/O Driver Types (Cont.)

SD_OEN_CASN	BT12LS	12 mA output buffer
SD_RASN	BT12LS	12 mA output buffer
SD_RASN0_CSN0	BT12LS	12 mA output buffer
SD_RASN1_CSN1	BT12LS	12 mA output buffer
SD_WEN_WEN	BT12LS	12 mA output buffer
SDCLKP	BT8LS	8 mA output buffer
SDONEP	BT12LS	12 mA output buffer
SELECT_CKOUT1N	IBUFLS	Input buffer
SELECT_PLLN	IBUFLS	Input buffer
STOPN	BD12CULS	12 mA Bi-directional buffer with pull-up
T0_OUTN	BT8LS	8 mA output buffer
T1_OUTN	BT8LS	8 mA output buffer
TCK	IBUFULS	Input buffer with pull-up
TDI_DINT	IBUFULS	Input buffer with pull-up
TDO_TPC	BT8LS	8 mA output buffer
TMS	IBUFULS	Input buffer with pull-up
TN	IBUFULS	Input buffer with pull-up
TPC[4:2]	BD8CDLS	8 mA Bi-directional buffer with pull-down
TRDYN	BD12CULS	12 mA Bi-directional buffer with pull-up
TRST	IBUFULS	Input buffer with pull-up
(Sheet 3 of 3)		

Package and Ordering Information

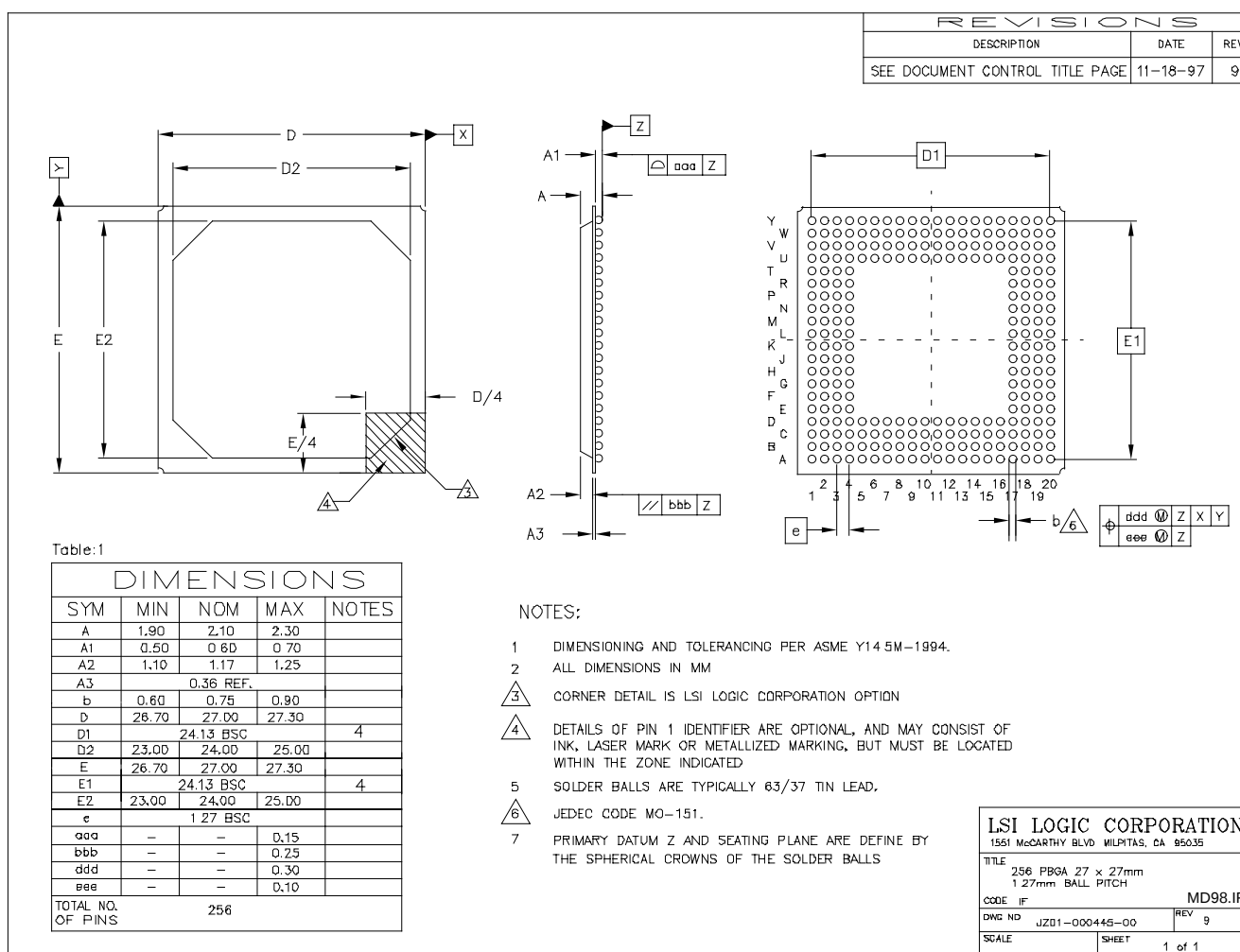
The LR4102 is available in a 256-lead Plastic Ball Grid Array (PBGA). [Table 21](#) provides the LR4102 order number and [Figure 10](#) contains the package mechanical drawing.

Table 21 LR4102 Ordering Information

Order Number	Clock Frequency	Package Type	Operating Range
L9A0212 ¹	85 MHz	256-lead PBGA	Commercial

1. Order number subject to change

Figure 10 LR4102 256 PBGA (IF) Mechanical Drawing



Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code IF.

Notes

Notes

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