

Bidirectional 3.3 V I/O Transceiver for SCSI-2, SCSI-3, and SCSI-3 Fast-20 Buses (LCBG10P)

Datasheet

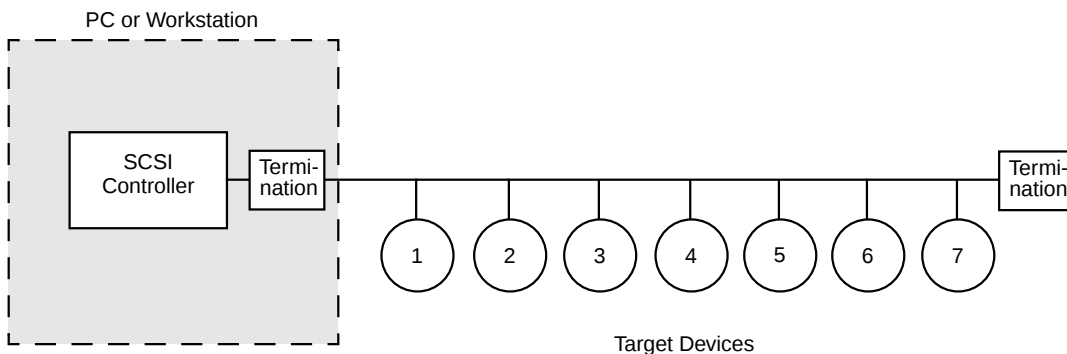
LSI LOGIC

LSI Logic's bidirectional transceiver for SCSI is used to transmit and receive data on a SCSI-2 or SCSI-3 bus. The bus operates at rates up to 20 MHz, with a cable length up to 3 m and maximum stub lengths of 0.1 m. Implementations that limit transfer rates to 5 MHz can extend the cable length to 6 m. SCSI bus termination is assumed to be external to the SCSI device.

This transceiver conforms to the *Information Technology—SCSI-3 Parallel Interface Specification* as well as to the *American National Standard for Information Systems—SCSI-3 Fast-20*, published by the X3T9.2 and X3T10 committees.

This transceiver can operate with SCSI-2, SCSI-3 10-MHz interfaces, or SCSI-3 Fast-20 interfaces. These I/O cells operate at up to 20 MHz. This transceiver is implemented in G10™ technology.

Figure 1 SCSI Bus Interface



Features and Benefits

- ◆ Compliant with *SCSI-3 Parallel Interface Specification*
- ◆ Compliant with the *American National Standard for Information Systems—SCSI-3 Fast-20*
- ◆ Reduces engineering effort of designing an interconnect to SCSI bus
- ◆ V/I characteristics that meet the SCSI bus drive requirements
- ◆ Provides for direct silicon interconnect to a SCSI transmission line
- ◆ On-chip 48 mA drivers
- ◆ 3.3-V V_{DD} (5-V–tolerant)
- ◆ Bidirectional I/O transceiver that provides maximum flexibility in I/O path design
- ◆ Available in the G10 cell-based product families (0.4 micron drawn gate length, 0.29 micron effective channel length)
- ◆ Transfer rates up to 20 MHz
- ◆ Active negation driver

Specifications

The following subsections provide the specifications for the SCSI bidirectional 3.3-V transceivers.

SCSI Bidirectional Transceiver

Name:	BDSESCSIF
Description:	SCSI 3.3-V bidirectional transceiver used with the SCSI-2, SCSI-3, and SCSI-3 Fast-20 buses
Width:	226.8 μm high, 112.0 μm wide
Coding Syntax:	$U(\text{IO}, \text{ZI}, \text{PO}) = \text{BDSESCSIF}(\text{IO}, \text{A}, \text{PI}, \text{EN}, \text{TN}, \text{NEG}, \text{HTPLG}, \text{IDDTN})$

Figure 2 shows the schematic symbol for the bidirectional transceiver.

Figure 2 Bidirectional Transceiver Logic Diagram

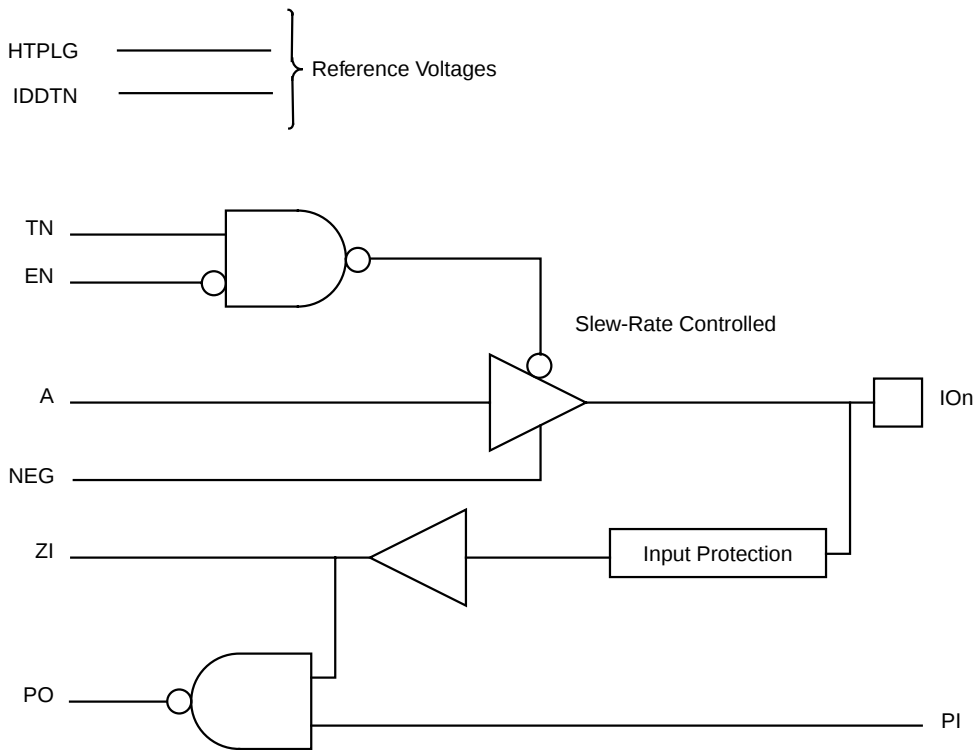


Table 1 provides the loading characteristics for the input portion for the bidirectional transceiver. Values are in standard loads.

Table 1 Bidirectional Transceiver's Loading Characteristic

Version	Technology	A	EN	TN	PI	NEG	iddtn	htplg
BDSESCSIF	LCBG10P	1.3	0.9	1.3	1.4	0.8	5.0	4.4

Input Portion of Bidirectional Transceiver

Table 2 provides the truth table for the input portion.

Table 2 Bidirectional Transceiver's Input Portion Truth Table

IO _n	PI	ZI	PO
0	X	0	1
1	0	1	1
1	1	1	0

Table 3 lists the DC characteristics and Table 4 the AC timing for the bidirectional transceiver's input portion. These specifications are valid only for the commercial operating range: junction temperature = 0 °C to 125 °C, $V_{DD} = 3.3 \text{ V} \pm 5\%$.

Table 3 Bidirectional Transceiver's Input Portion DC Characteristics for 3.3-V and 5.0-V Signaling

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{ih}	Input High Voltage ¹	Signal FALSE State	1.9		5.25	V
V_{il}	Input Low Voltage	Referenced to V_{SS} Signal TRUE State	-0.5		1.0	V
V_{ik}	Input Clamp Voltage	$V_{DD} = \text{Min}$; $I_i = -20 \text{ mA}$			-0.75	V
V_{th}	Threshold, High to Low		1.00		1.30	V
V_{tl}	Threshold, Low to High		1.60		1.90	V
$V_{th}-V_{tl}$	Hysteresis		300			mV
I_{il}	Low Level Input Current	$V_i = 0.5 \text{ V}$, Power ON or Power OFF, except during Hot Plug			+/- 20	μA
(Sheet 1 of 2)						

Table 3 Bidirectional Transceiver's Input Portion DC Characteristics for 3.3-V and 5.0-V Signaling (Cont.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{ih}	High Level Input Current	$V_i = 2.7\text{ V}$, Power ON or OFF, except during Hot Plug			+/- 20	μA
$I_{ih.hp}$	Hot Plug High Level Current Peak	Transient duration to 10% of peak = 20 μs . Applies during physical insertion only.			+1.5	mA
V_{DD}	Supply Voltage		3.14	3.30	3.45	V
T_j	Junction Temp		0		125	$^{\circ}\text{C}$
I_{lu}	Latch Up Current	$-2\text{ V} < V_{pin} < +8\text{ V}$			+/- 100	mA
ESD	Electrostatic Discharge	MIL-STD-883C, Method 3015.7, 100 pF@1.5K Ω	2001			V
(Sheet 2 of 2)						

1. Note: absolute maximum of 8.0 V.

Table 4 Bidirectional Transceiver's Input Portion AC Timing for 3.3-V and 5.0-V Signaling (ns)

Delay Path	Output	Standard Load					
		0	2	4	8	12	16
ION to ZI	tpLH	0.31	0.35	0.37	0.43	0.48	0.54
	tpHL	0.24	0.26	0.29	0.34	0.38	0.43

Note:

- ◆ Max values apply over all V_{CC} , temperature, and process conditions.
- ◆ AC Timing measurements are made with T_r , T_f (0.5 V – 2.3 V, 2.3 V – 0.5 V) less than 6 ns.

Output Portion of Bidirectional Transceiver

Table 5 shows the truth table for the output portion of the bidirectional transceiver.

Table 5 Bidirectional Transceiver's Output Portion Truth Table

IDDTN	NEG	A	TN	EN	IO _n
1	0	X	X	1	High Z
1	0	X	0	X	High Z
1	0	0	1	0	0
1	0	1	1	0	1
1	1	X	X	1	High Z
1	1	X	0	X	High Z
1	1	0	1	0	0
1	1	1	1	0	High Z
0	X	X	X	X	High Z

Note: On a SCSI bus, a HIGH is negated, and a LOW is asserted.

Table 6 lists the DC characteristics and Table 7 the AC timing for the output portion of the bidirectional transceiver. These specifications are valid only for the commercial operating range: junction temperature = 0 °C to 125 °C, $V_{DD} = 3.3 \text{ V} \pm 5\%$. Figure 3 shows the timing test circuit for the output portion of the bidirectional transceiver.

Table 6 Bidirectional Transceiver's Output Portion DC Characteristics for 3.3-V and 5.0-V Signaling

Symbol	Parameter	Min	Typ	Max	Units	Test Condition
V_{OL}	Output Low Voltage	0.0		0.5	V	$I_{OL} = 48 \text{ mA}$ Signal TRUE State
V_{OH}	Output High Voltage	2.0		3.24	V	$I_{OH} = -7 \text{ mA}$ Signal FALSE State Requires $V_{DD} = 4.75 - 5.25 \text{ V}$
I_{IL}	Low Level Output Current			+/- 20	μA	High Z State: $V_I = 0.5 \text{ V}$, Power ON or Power OFF, except during Hot Plug
I_{IH}	High Level Output Current			+/- 20	μA	High Z State: $V_I = 2.7 \text{ V}$, Power ON or OFF, except during Hot Plug
$I_{IH.hp}$	Hot Plug High Level Current Peak			+1.5	mA	High Z State: Transient duration to 10% of peak = 20 μs . This applies during physical insertion only.
I_I	Output Leakage			+/-10	μA	High Z State, $V_{DD} = \text{MAX}$
V_{DD}	Supply Voltage	3.14	3.30	3.45	V	V_{OL} and High Z only
T_j	Junction Temp	0		125	°C	
I_{LU}	Latch Up Current			+/- 100	mA	$-2 \text{ V} < V_{pin} < +8\text{V}$
ESD	Electrostatic Discharge	2001			V	MIL-STD-883C, Method 3015.7, 100 pF@1.5 K Ω

Figure 3 SCSI Output Timing (Rise Time) Test Circuit

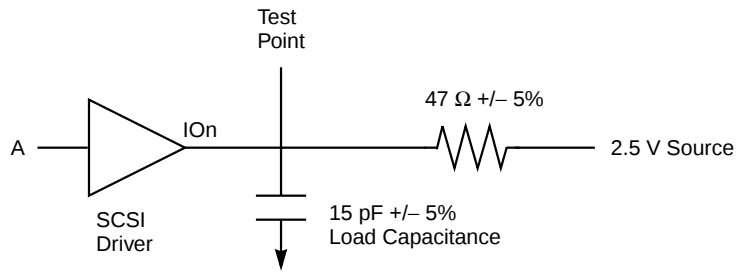


Table 7 provides the AC timing of the buffer's output portion.

Table 7 Bidirectional Transceiver's Output Portion AC Timing (ns, Slew)

Delay Path	Output	Load (pF)			
		15	50	85	100
A to IOOn	tpLH	6.12	6.68	7.09	7.25
	tpHL	8.08	8.79	9.41	9.65
	tpZL	6.17	7.51	8.22	8.50
	tpLZ	10.18	9.95	9.73	9.66
EN to IOOn	tpZH	2.52	4.03	5.80	6.56
	tpZL	6.76	7.56	8.27	8.55
	tpLZ	10.19	9.95	9.74	9.67
	tpHZ	1.55	1.55	1.55	1.55
TN to IOOn	tpZH	2.30	4.07	5.85	6.61
	tpZL	6.63	7.44	8.15	8.43
	tpLZ	10.10	9.87	9.66	9.58
	tpHZ	1.42	1.42	1.42	1.42

Note:

- ♦ Values apply over all V_{CC} , temperature, and process conditions.
- ♦ PADS = 1.
- ♦ Slew rate of signal from HIGH to LOW = 520 mV/ns Max Slew (0.7–2.3 V), best case process, temperature, voltage, with 15-pF load, 10–90% of full amplitude.

Cell Placement Restrictions

The following cells are designed to be used with BDSESCSIF in LCBG10p technology:

- ◆ pvdd2_sescsi: To supply vdd2
- ◆ pvdd_sescsi: To supply 3.3 V to the I/O buffer
- ◆ pvss2_sescsi: To supply vss2
- ◆ dvdd_sescsi: Dummy cell for single-ended SCSI cells

The first three cells in this list supply vdd2, 3.3-V I/O buffer, and vss2 to the SCSI buffers. The dvdd_sescsi cell provides a protection diode between vddsescsi and vssio. Adhere to the following guidelines when placing these cells:

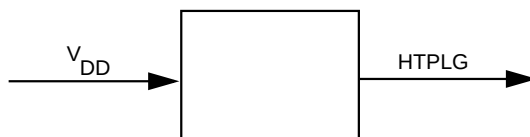
1. At least one dummy cell must be placed at both ends of the SCSI section.
2. There must be at least one pvdd_sescsi cell per five SCSI buffers; one V_{SS} per two SCSI buffers.

Power On Reset Cell

Name:	SCSIPOR
Description:	Provides power-up timing to the output and bidirectional cells. This cell must be used; only one is needed for all I/O transceivers.
Width	226.8 μm high, 144.2 μm wide
Coding Syntax	$U(\text{HTPLG}) = \text{SCSIPOR}()$; for 3.3 VDD

Figure 4 shows the schematic symbol for the power on reset cell.

Figure 4 Power On Reset Cell



Recommended Operating Conditions

Table 8 provides the recommended operating conditions for the bidirectional SCSI I/O transceiver.

Table 8 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	DC Supply Voltage	3.14	3.3	3.47	V
T_j	Junction Temperature	0	30	125	$^{\circ}\text{C}$

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