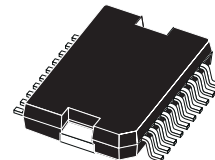


## DUAL 5V MULTIFUNCTION VOLTAGE REGULATOR

- STANDBY OUTPUT VOLTAGE PRECISION 5V  $\pm 2\%$
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 260 $\mu$ A, IN STANDBY MODE
- OUTPUT CURRENTS :  $I_{O1} = 50\text{mA}$ ,  $I_{O2} = 500\text{mA}$
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



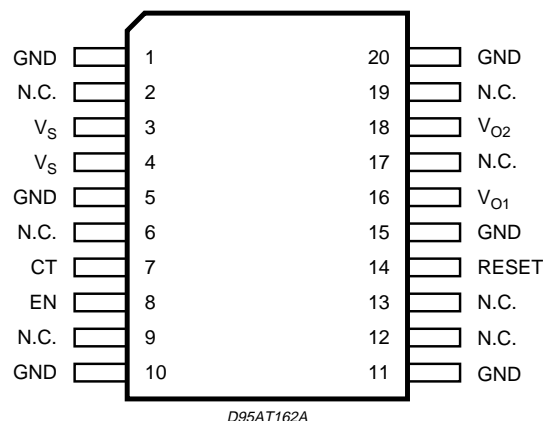
**PowerSO20**

**ORDERING NUMBER:** L4937NPD

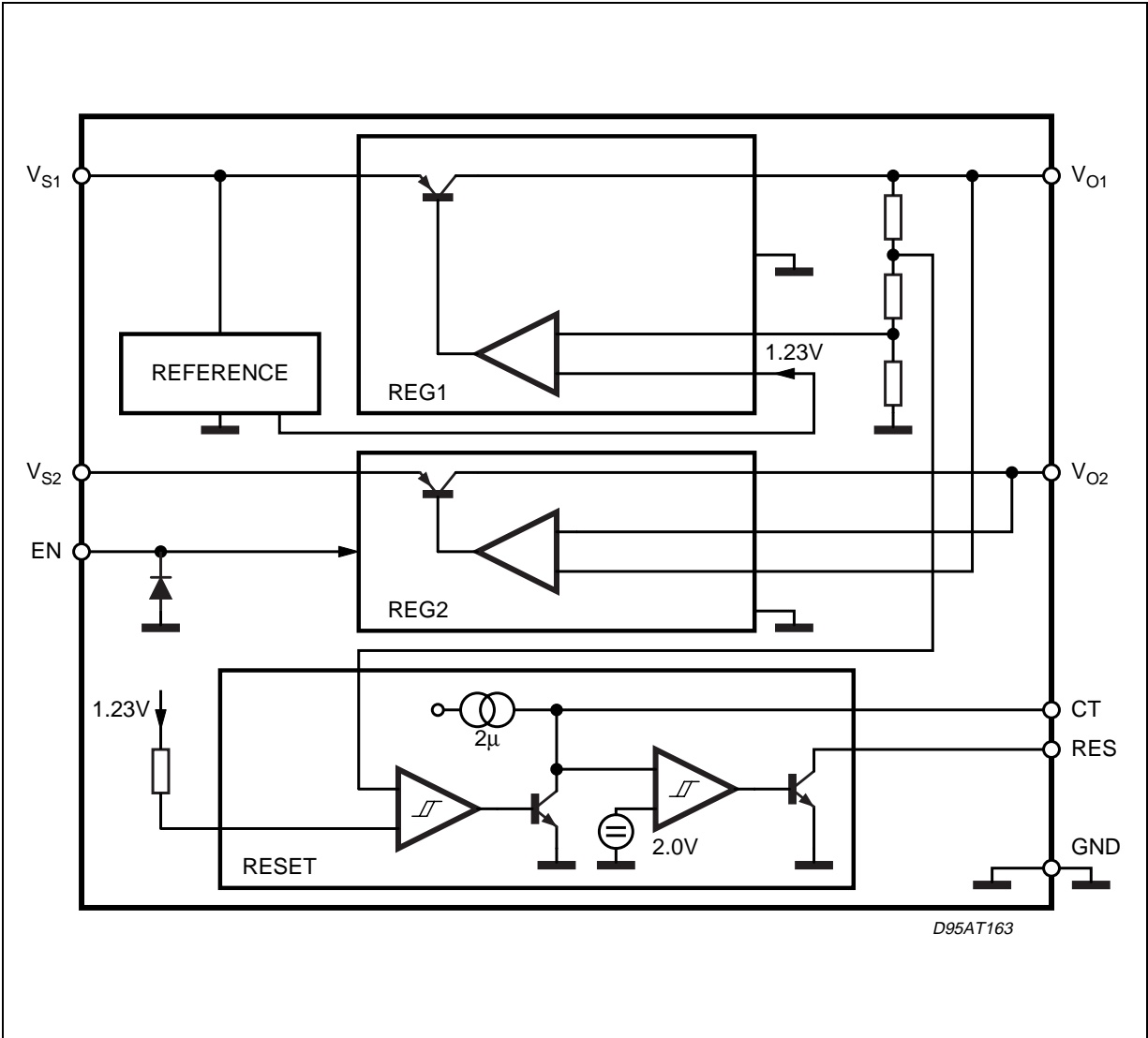
### DESCRIPTION

The L4937NPD is a monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. They are designed for supplying microcomputer controlled systems specially in automotive applications.

### PIN CONNECTION (top view)



BLOCK DIAGRAM



THERMAL DATA

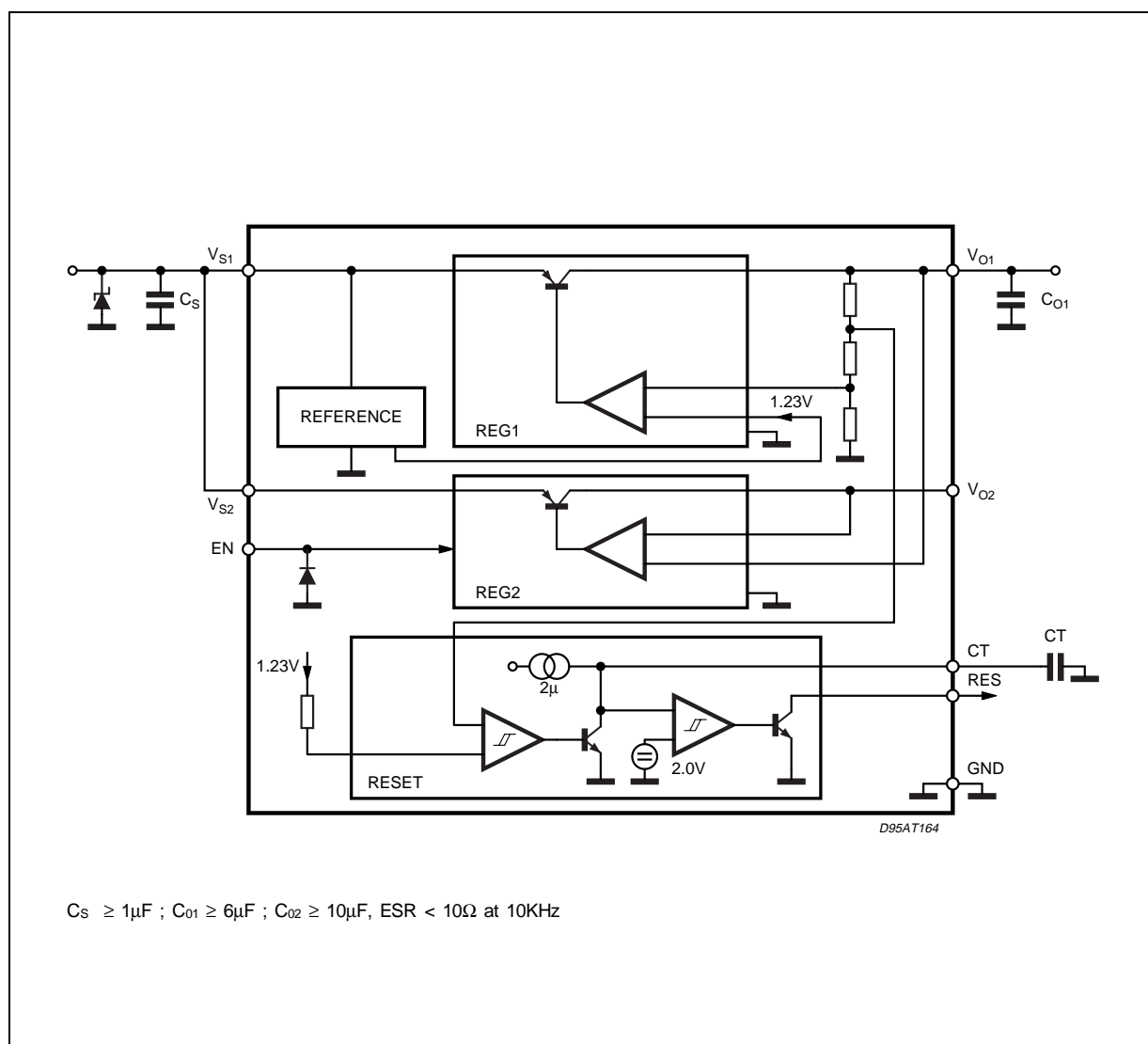
Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-Case	Max. 1.5	°C/W

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	DC Supply Voltage	28	V
	Transient Supply Voltage ( $T < 1s$ )	40	V
$T_j, T_{stg}$	Junction and Storage Temperature Range	-55 to 150	°C
$I_{EN}$	Enable Input Current ( $V_{EN} \leq 0.3V$ )	$\pm 1$	mA
$V_{EN}$	Enable Input Voltage	$V_S$	
$V_{RES}$	Reset Output Voltage	20	V
$I_{RES}$	Reset Output Current	5	mA
$P_D$	Power Dissipation	875	mW

**Note :** The circuit is ESD protected according to MIL-STD-883C.

## APPLICATION CIRCUIT



**ELECTRICAL CHARACTERISTICS** ( $V_S = 14V$ ;  $-40^{\circ}C \leq T_J \leq 125^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_S$	Operating Supply Voltage				25	V
$V_{O1}$	Standby Output Voltage	$6V \leq V_S \leq 25V$ $1mA \leq I_{O1} \leq 50mA$	4.90	5.00	5.10	V
$V_{O2} - V_{O1}$	Output Voltage 2 Tracking Error	$6V \leq V_S \leq 25V$ $5mA \leq I_{O2} \leq 500mA$ Enable = LOW	-25		+25	mV
$V_{DP1}$	Dropout Voltage 1	$I_{O1} = 10mA$ $I_{O1} = 50mA$		0.1 0.2	0.25 0.4	V V
$V_{IO1}$	Input to Output Voltage Difference in Undervoltage Condition	$V_S = 4V$ , $I_{O1} = 35mA$			0.4	V
$V_{DP2}$	Dropout Voltage 2	$I_{O1} = 100mA$ $I_{O1} = 500mA$		0.2 0.3	0.3 0.6	V V
$V_{IO2}$	Input to Output Voltage Difference in Undervoltage Condition	$V_S = 4.6V$ , $I_{O1} = 350mA$			0.6	V
$V_{OL1,2}$	Line Regulation	$6V \leq V_S \leq 25V$ $I_{O1} = 1mA$ ; $I_{O2} = 5mA$			20	mV
$V_{OLO1}$	Load Regulation 1	$1mA \leq I_{O1} \leq 50mA$			25	mV
$V_{OLO2}$	Load Regulation 2	$5mA \leq I_{O2} \leq 500mA$			50	mV
$I_{LIM1}$	Current Limit 1	$V_{O1} = 4.5V$ $V_{O1} = 0V$ (note 1)	55 25	100 50	200 100	mA mA
$I_{LIM2}$	Current Limit 2	$V_{O2} = 0V$	550	1000	1700	mA
$I_{QSB}$	Quiescent Current Standby Mode (output 2 disabled)	$I_{O1} = 0.3mA$ ; $T_J < 100^{\circ}C$ $V_{EN} \geq 2.4V$ $V_S = 14V$ $V_S = 3.5V$		210 340	290 850	$\mu A$ $\mu A$
$I_Q$	Quiescent Current	$I_{O1} = 50mA$ $I_{O1} = 500mA$			30	mA

**ENABLE**

$V_{ENL}$	Enable Input LOW Voltage (output 2 active)		-0.3		1.5	V
$V_{ENH}$	Enable Input HIGH Voltage		2.4		7	V
$V_{ENhyst}$	Enable Hysteresis		30	75	200	mV
$I_{EN}$	Enable Input Current	$0V < V_{EN} < 1.2V$ $2.5V < V_{EN} < 7V$	-10 -1	-1.5 0	-0.5 +1	$\mu A$ $\mu A$

## ELECTRICAL CHARACTERISTICS (continued)

## RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{Rt}$	Reset Low Threshold Voltage		$V_{o1} - 0.4$	4.7	$V_{o1} - 0.1$	V
$V_{Rth}$	Reset Threshold Hysteresis		50	100	200	mV
$t_{RD}$	Reset Pulse Delay	$C_T = 100\text{nF}$ ; $t_R > 100\mu\text{s}$	55	100	180	ms
$t_{RR}$	Reset Reaction Time	$C_T = 100\text{nF}$	1	10	50	$\mu\text{s}$
$V_{RL}$	Reset Output LOW Voltage	$R_{RES} = 10\text{K}\Omega$ to $V_{o1}$ $V_S = 1.5\text{V}$			0.4	V
$I_{LRES}$	Reset Output HIGH Leakage	$V_{RES} = 5\text{V}$			1	$\mu\text{A}$
$V_{CTh}$	Delay Comparator Threshold			2.0		V
$V_{CTh, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

**Note :** 1: Foldback characteristic

## FUNCTIONAL DESCRIPTION

The L4937ND is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

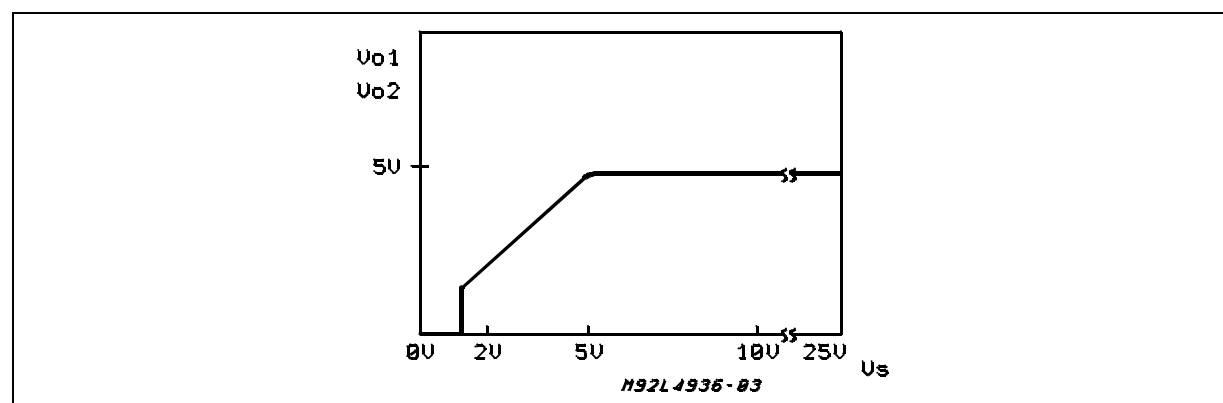
Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

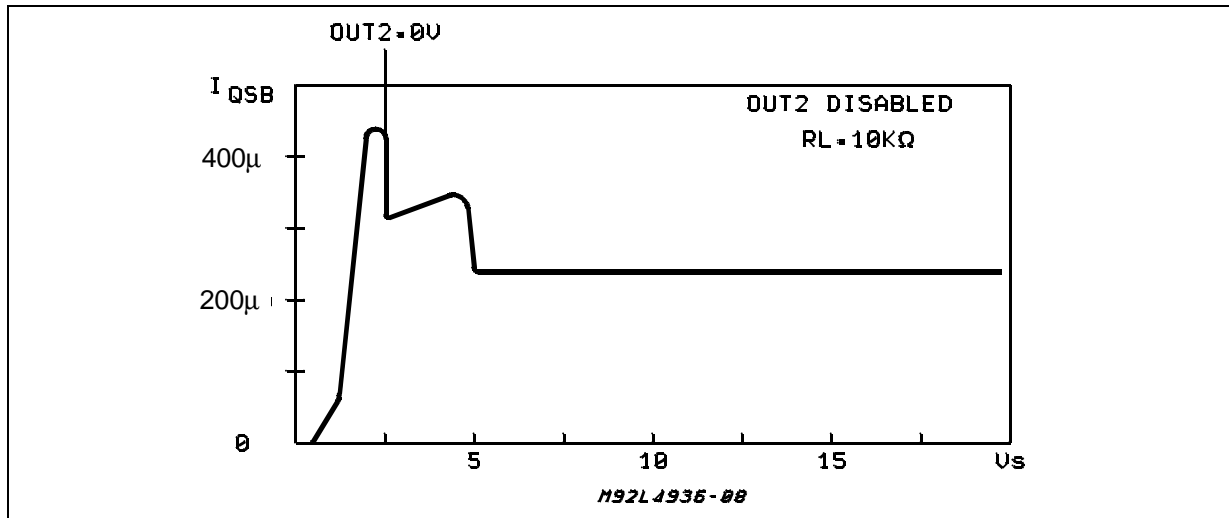
## STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

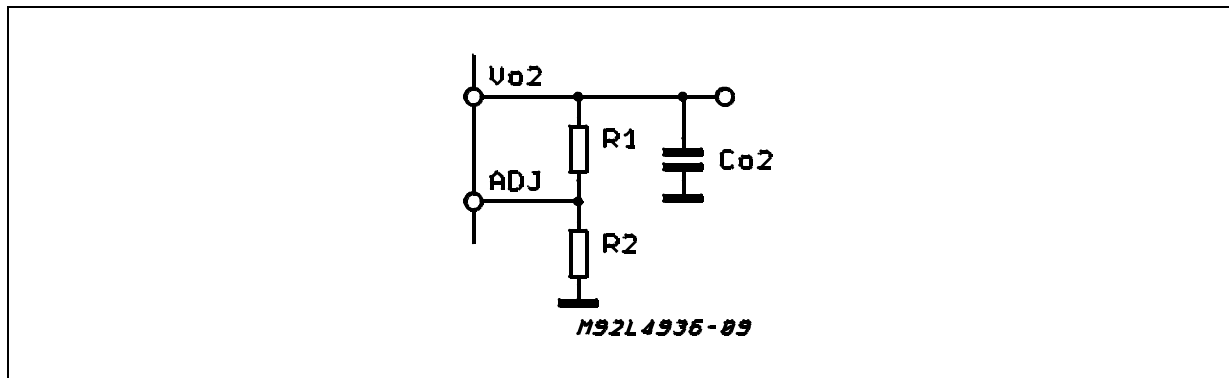
**Figure 1 :** Output Voltage vs. Input Voltage.



**Figure 2 :** Quiescent Current vs. Supply Voltage.



**Figure 3 :** Programmable Output 2 Voltage with External Resistors.



#### RESET CIRCUIT

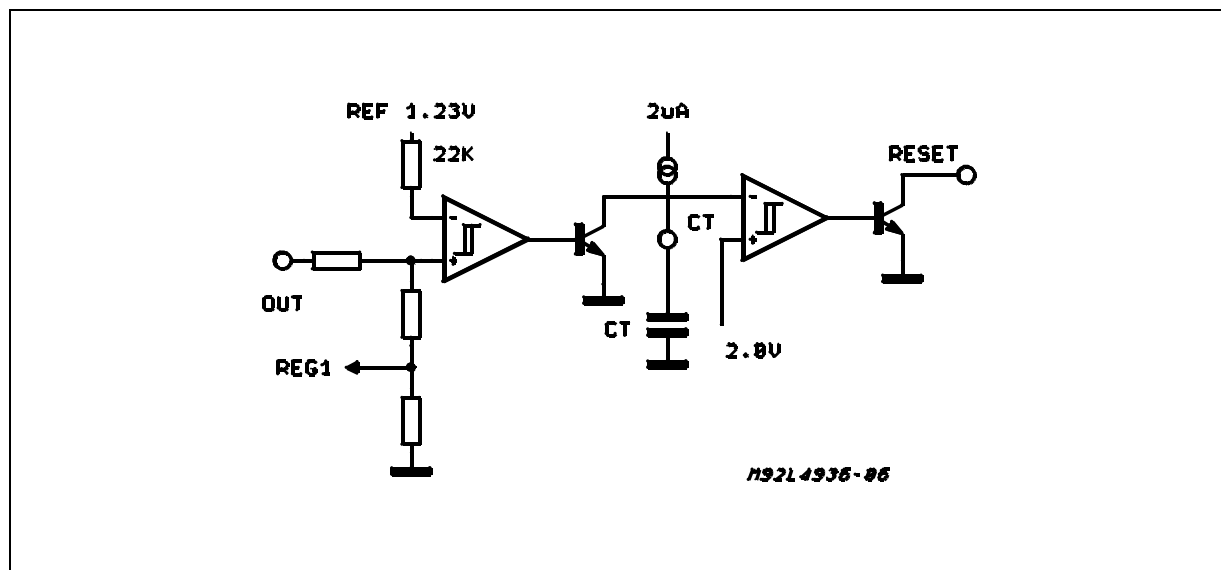
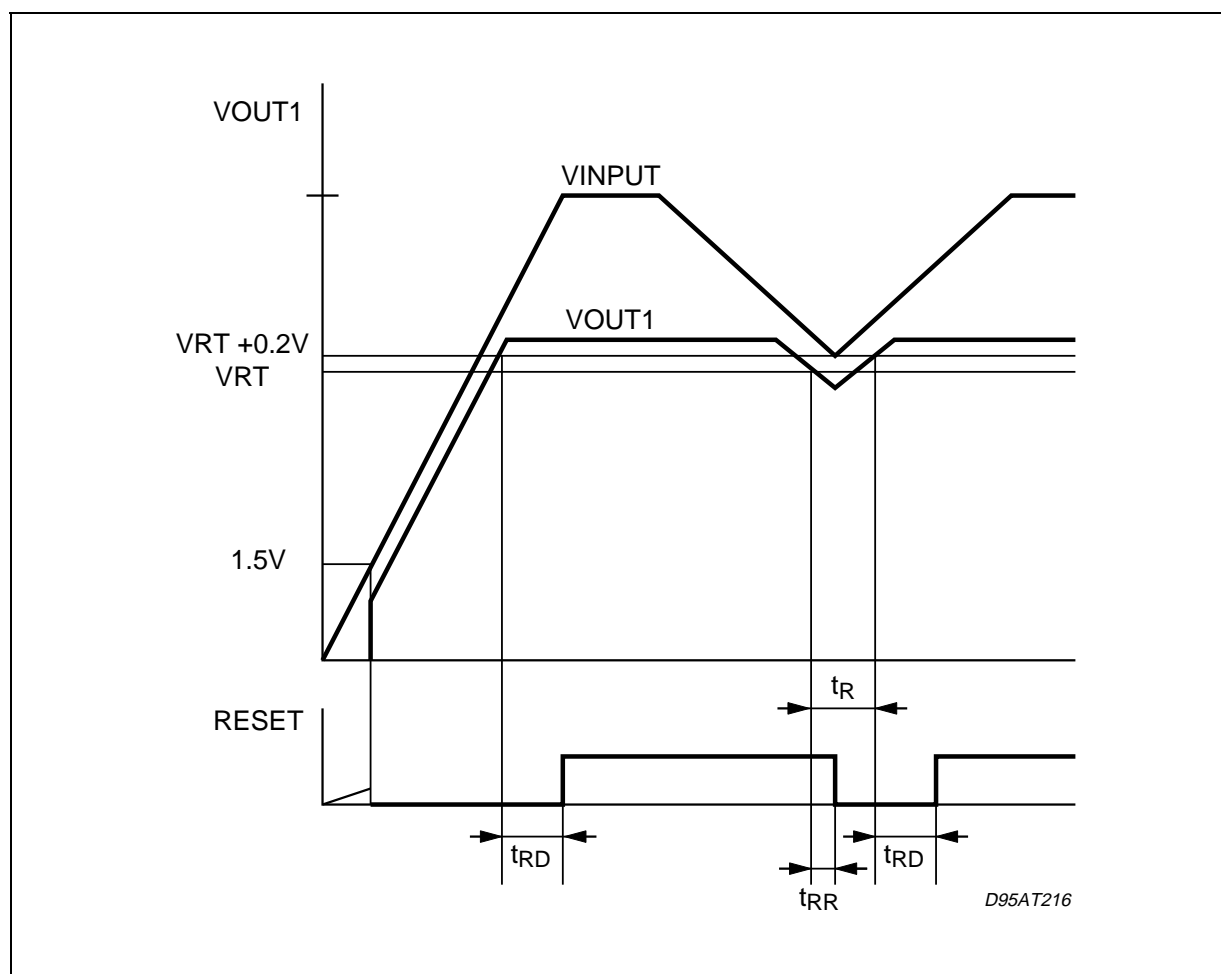
The block circuit diagram of the reset circuit is shown in fig. 4. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time  $t_{RD}$ , is defined by the charge time of an external capacitor  $C_T$  :

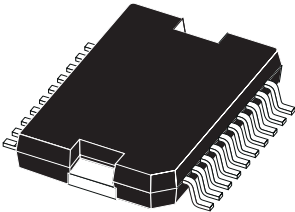
$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor  $C_T$  and is proportional to the value of  $C_T$ .

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time  $t_{RR}$ , no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor  $C_T$ . This time is typically equal to 50µs if  $C_T = 100nF$ . The typical reset output waveforms are shown in fig. 5.

**Figure 4** :Block Diagram of the Reset Circuit.**Figure 5** : Typical Reset Output Waveforms.

# OUTLINE AND MECHANICAL DATA

A 3D perspective view of a JEDEC MO-166 PowerSO20 package. The package is a black, rectangular component with a central notch. It features 20 pins: 10 pins on the left side and 10 pins on the right side, all bent at a 90-degree angle. The package is shown from an isometric perspective, highlighting its profile and the pin arrangement.

## JEDEC MO-166

# PowerSO20

Technical drawing of a 20-pin D-subminiature connector, showing front, top, and detail views with dimensions and labels.

**Front View (Top Left):** Shows the connector's profile with dimensions  $N$  (pin height),  $a2$  (pin pitch),  $A$  (overall height),  $b$  (pin width),  $e$  (pin offset),  $e3$  (pin spacing), and  $H$  (overall length). A callout indicates **DETAIL A**.

**Top View (Bottom Left):** Shows the connector's footprint with dimensions  $D$  (overall width),  $E1$  (overall height),  $E2$  (mounting hole spacing),  $T$  (mounting hole diameter), and  $h \times 45$  (mounting hole diameter). Pin positions are labeled 1, 10, 11, and 20. A callout indicates **DETAIL B**.

**Detail A (Top Right):** Shows the pin profile with dimensions  $R$  (fillet radius),  $a1$  (pin width), and  $c$  (pin thickness). A callout indicates **DETAIL B**.

**Detail B (Middle Right):** Shows the pin profile with dimensions  $a3$  (pin width),  $lead$  (lead length), and  $slug$  (slug length). A callout indicates **DETAIL B**.

**Bottom View (Bottom Right):** Shows the connector's footprint with dimensions  $D1$  (overall width) and  $E3$  (overall height). A callout indicates **DETAIL B**.

**Additional Labels:** **lead**, **slug**, **Gage Plane**, **SEATING PLANE**, **COPLANARITY**, **PSO20MEC**.



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