LXT6155 155 Mbps SDH/SONET/ ATM Transceiver

Application Note

January 2002

Order Number: 249280-003

As of January 15, 2001, this document replaces the Level One document known as *AN141*.

Application Note

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Revision History

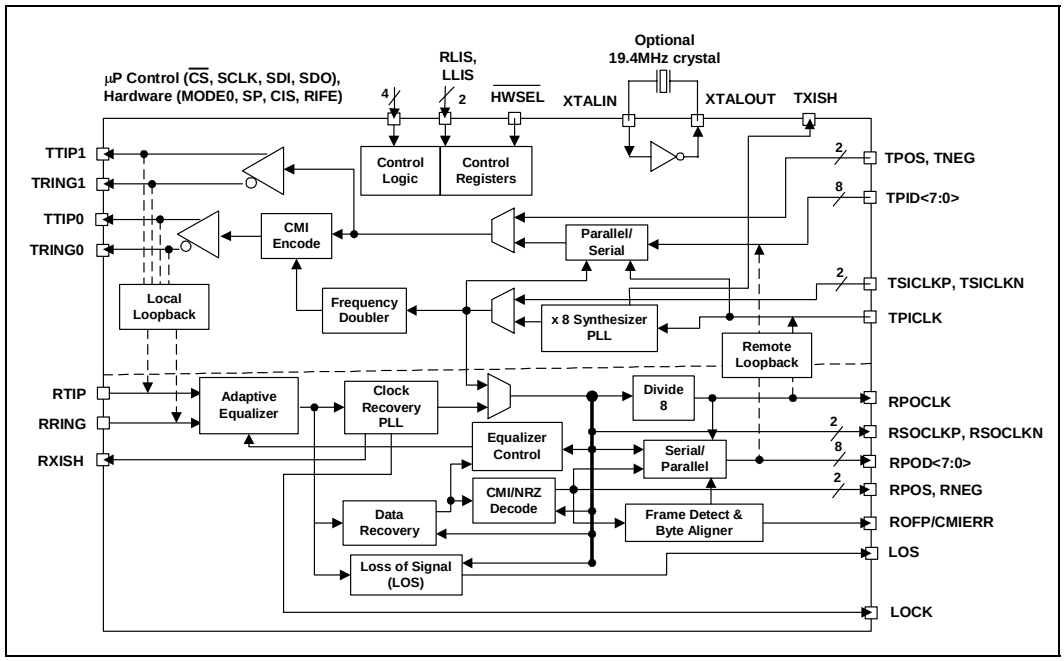
Date	Revision	Description
January 2002	003	Replaced “Receive Output Frame Pulse Operation” section with “Software Development Guide” section.
March 2001	002	Changed the format.
January 2001	001	This was the first publication of this document.

1.0 Product Overview

1.1 General Description

The LXT6155 SDH/SONET/ATM Transceiver is a high-speed, fully integrated transceiver designed for 156-Mbps SDH/SONET/ATM transmission system applications. The block diagram for the device is shown in Figure 1.

Figure 1. LXT6155 Block Diagram



The LXT6155 SDH/SONET/ATM Transceiver provides a LVPECL interface, for fiber-optic modules, and a CMI interface, for coax cable. These circuits are implemented using Intel's low-power 3.3-V, CMOS analog, and digital technology.

The transmitter incorporates a parallel-to-serial converter, a frequency multiplier PLL, CMI/NRZ line encoders, and line drivers for both coax and fiber applications.

The receiver incorporates an adaptive equalizer, a clock recovery PLL, Loss-of-Signal (LOS) detector, CMI/NRZ decoders, serial-to-parallel converters, and an SHD/SONET frame-byte detector/aligner.

The LXT6155 SDH/SONET/ATM Transceiver provides both a parallel and serial transmit and receive interface. The LXT6155 SDH/SONET/ATM Transceiver can be controlled through hardware or a serial microprocessor (µP) interface.

1.2 Features

- Complies with:
  - Bellcore SONET GR-253
  - ITU-T G.703/813/958 STM1
- Line interface formats:
  - Fiber LVPECL NRZ
  - Coax CMI
- Transmit synthesizer PLL
- Receive clock-recovery PLL
- Adaptive CMI equalizer
- Analog circuitry for transformer drive
- Programmable LOS function
- CMI/NRZ encoder and decoder
- Serial/Parallel and Parallel/Serial conversion
- Two modes of operation:
  - Microprocessor-controlled, software mode
  - Stand-alone, hardware mode
- No external crystal required. (A 19.44-MHz crystal is optional.)
- Low power consumption (less than 760 mW typical)
- Operates from a single 3.3-V supply

1.3 Applications

The LXT6155 SDH/SONET/ATM Transceiver provides a single-chip solution for several SDH/SONET/ATM, 156-Mbps applications. The LXT6155 SDH/SONET/ATM Transceiver is well suited for the following:

- OC-3/STM-1 transmission systems
- OC-3/STM-1 SDH/SONET add/drop mux
- OC-3/STM-1 SDH/SONET cross-connect
- OC-3/STM-1 WAN/ATM transmission systems
- OC-3/STM-1 WAN/ATM access systems

2.0 Interfaces

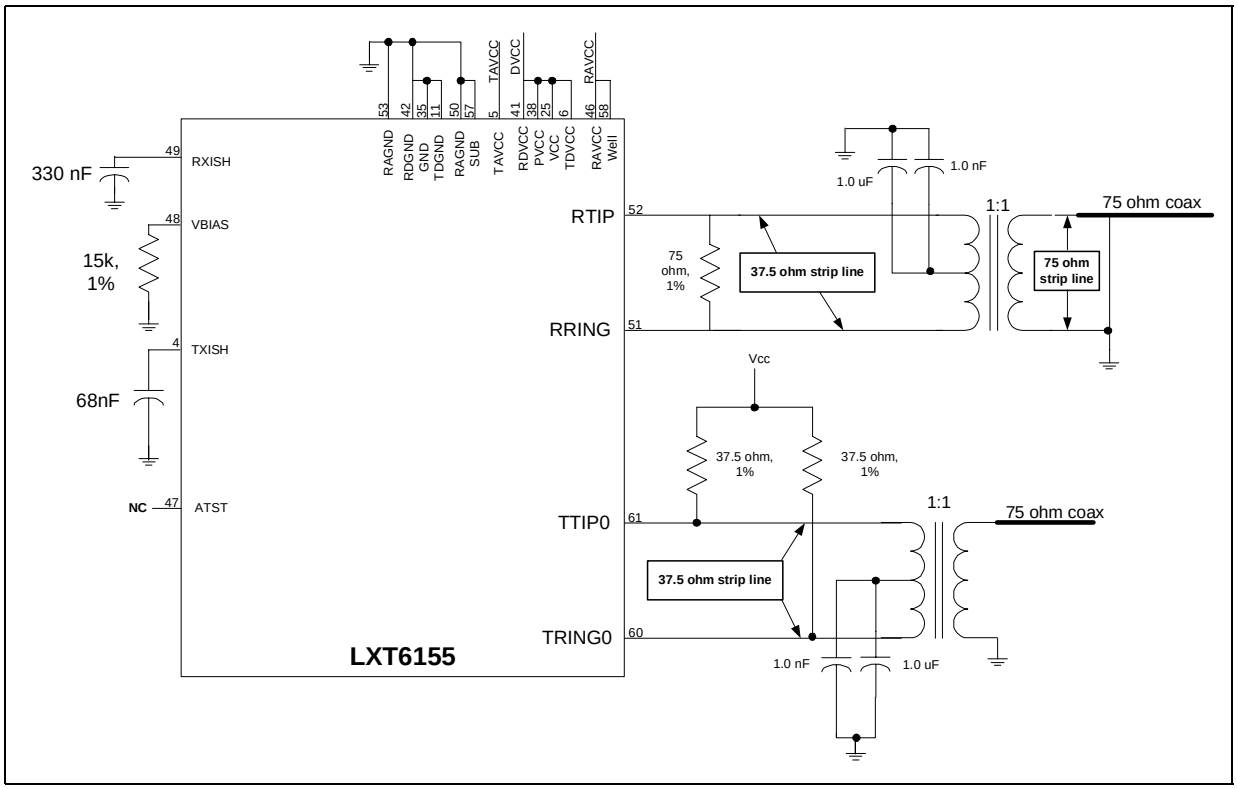
2.1 Coax Line Interface

The LXT6155 SDH/SONET/ATM Transceiver supports coaxial line interface in both the receive and transmit paths. An adaptive equalizer and CMI encoder/decoder are incorporated on chip, eliminating the need for external components to complete the coax interface.

The transmit drivers must be pulled up with two 37.5-Ω resistors and laid out with 37.5-Ω, constant-impedance strip lines.

The receiver must be terminated with a 75-Ω +- 1% resistor. The receiver connections also must be laid out with 37.5-Ω strip line.

Figure 2. LXT6155 SDH/SONET/ATM Transceiver Coax Interface Circuit



To comply with SONET/SDH coax interface standards, transformers T1 and T2 should meet the values listed in Table 1.

Table 1. Transformer Specification

Parameter	Min	Typ	Max	Unit	Notes
Transmission, S12	-		10	MHz	-3 dB Hi Pass
	320		-	MHz	-3 dB Low Pass
Return loss, S11	-		5	MHz	-20 dB Hi Pass
	250		-	MHz	-20 dB Low Pass
Transmission In-band loss	-		0.5	dB	30 MHz ~ 300 MHz
Common mode rejection	-		-10	dB	DC~250 MHz
Cross-talk in dual packages	-		-40	dB	DC~156 MHz
Turns ratio	0.97	1.0	1.03		

Table 2 lists the part(s) that have met the above transformer requirements.

Table 2. Pulse Engineering

Part Number	Description	Web
ST6200, R4006	320-MHz CMI Transformer Package	www.pulseeng.com/

2.2 Fiber Optic Line Interface

The LXT6155 SDH/SONET/ATM Transceiver supports fiber-optic line interface in both the receive and transmit paths. An on chip NRZ encoder/decoder provides the proper fiber interface. Direct coupling of a 3.3-V, optical module and the LXT6155 SDH/SONET/ATM Transceiver is accomplished though the network pictured in Figure 3.

Note: The PCB connections from the fiber module to the LXT6155 SDH/SONET/ATM Transceiver are a 50-Ω, impedance-controlled strip line.

2.2.1 LXT6155 SDH/SONET/ATM Transceiver and PECL (5.0 V) Interface

AC coupling must be carefully done in order to terminate drivers and provide proper DC-biased inputs to the fiber-optic modules and to the LXT6155 SDH/SONET/ATM Transceiver. See Figure 3 for the proper interface.

Figure 3. Direct Fiber Optic Module Interface Circuit

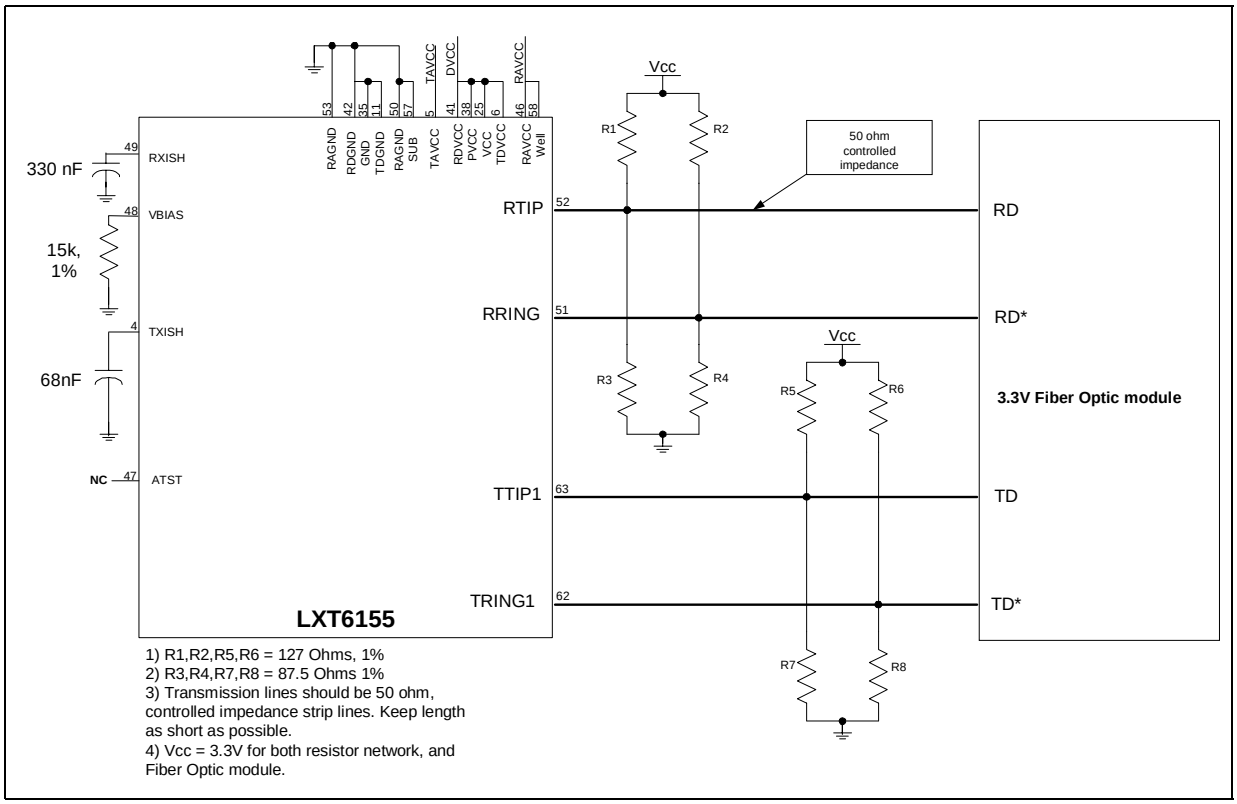


Figure 4. AC Coupling Between A 5 V PECL Module and LXT6155 SDH/SONET/ATM Transceiver

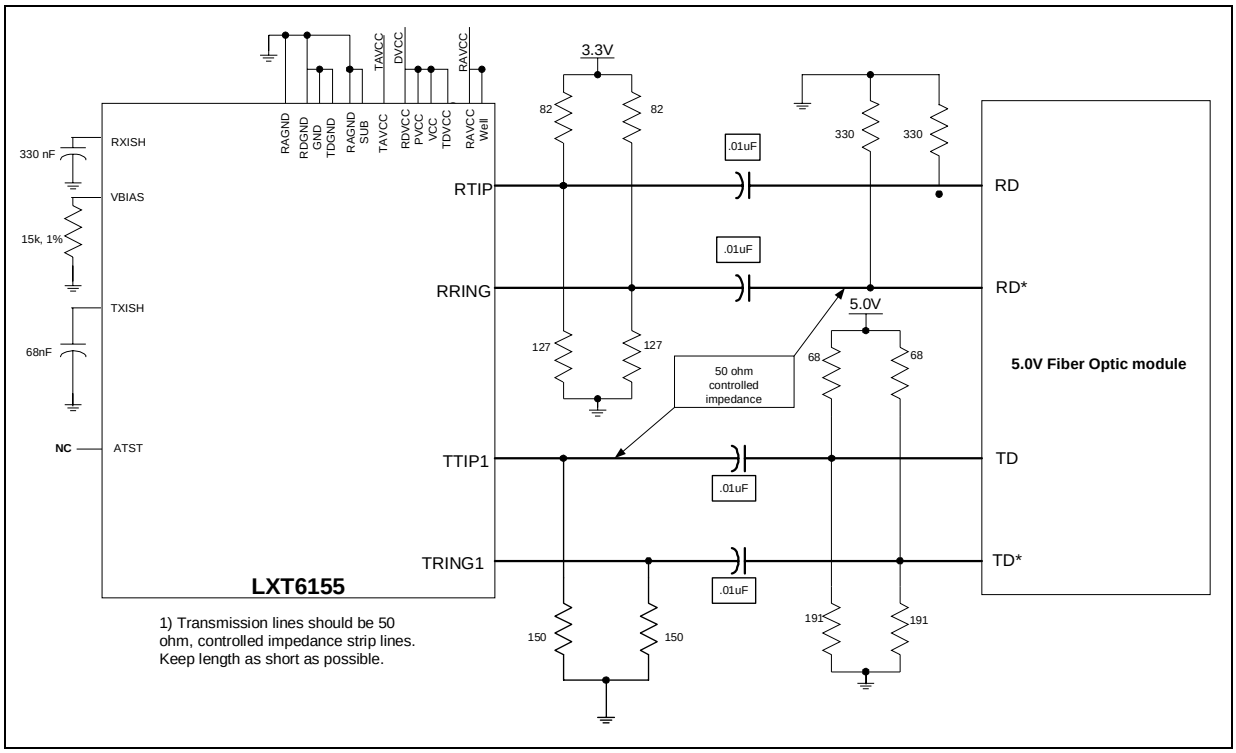


Table 3 lists the fiber modules that are recommended with the LXT6155 SDH/SONET/ATM Transceiver.

Table 3. Recommended Fiber Modules for LXT6155 SDH/SONET/ATM Transceiver

Sumitomo Electric	Hewlett Packard	Siemens
SDT 8211-T, SDT 8511-R; 40-km Range, SMFFC Pigtail.	XMT5170 (Transmitter), RCV1551 (Receiver); 40-km Range, SMF FC Pigtail	V23826-H18-C373; 3.3-V SMF SC Duplex Transceiver.
SDT 8201-T, SDT 8501-R; 15-km Range. SMF FC Pigtail.	XMT5370 (Transmitter), RCV1551 (Receiver); 15-km Range, SMF FC Pigtail	V23806-A84-C2; SMF SC Duplex Transceiver.
SCM7101-XC, 3.3-V SMF SC Duplex Transceiver	HFBR 5205B; MMF SC Duplex Transceiver.	
SDM4201-XC. MMF SC Duplex Transceiver.	HFCT 5205B; SMF SC Duplex Transceiver.	

3.0 Software Development Guide

Table 4 through Table 13 list register settings and options for the software development. The tables include:

Table 4. Register Settings: Initialization

Register	Bit	Default	Functional
11	6	1	This register is “write only”. Upon Power-up, this register should be set to 0 every time.

Table 5. Register Settings: Basic Settings

Register	Bit	Default	Functional
0	5	0	PLL reference clock control: 0 = Use TPICLK or TSICLKP,N 1 = Use external crystal XTALIN **NOTE:** The default setting for Reg 0 Bit 5 will conflict with the default setting in Reg 1 Bit 0 (Tx monitoring function).
0	1	0	System interface selection 0 = Serial mode 1 = Parallel mode
0	0	0	Line side selection 0 = Fiber NRZ 1 = Coax CMI

Table 6. Register Settings: Tx-Clock Monitoring (System Side)

Register	Bit	Default	Functional
1	0	1	Tx clock monitor enable. This bit must be disable in SW mode when Register 0 Bit 5 = 0 0 = Disable 1 = Enable
NOTE: For parallel, serial modes, if there is no tx clock within 200 ns, the Tx output will stop sending data to the line until the Tx clock is detected again. However, if the PLL reference clock is Tx clock, the chip will not be active without Tx clock input.			

Table 7. Register Settings: Rx-Output Clock Recovery (System Side)

Register	Bit	Default	Functional
10	7	1	Rx clock switching under LOS/LOCK condition 0 = Disable 1 = Enable
NOTE: If the LOS (LOS = High) or Rx PLL loss of lock (LOCK = Low) happened, RPOCLK or RSOCLK P/N is switched to the reference clock (Register 0 Bit 5 - Tx input clock or external crystal). The output of system side will be forced to all zeros.			

Table 8. Register Settings: Loopback Operation

Register	Bit	Default	Functional
0	7	0	Local loopback 0 = Disable 1 = Enable
0	6	0	Remote loopback 0 = Disable 1 = Enable
NOTE: Local loopback routes Tx line-side output signals to the Rx line-side input. TTIP and TRING are still active. Remote lookback routes Rx system-output signals (data and clock) to Tx system-side input. RPOD/RSOD and RPOCLK/RSOCLK are still active.			

Table 9. Frame-Detect and Media Options

Frame Detect	Coax/Serial	Coax/Parallel	Fiber/Serial	Fiber/Parallel
Enable	X[2]	ROFP	X[2]	ROFP
Disable	CMI Error	CMI Error	X[2]	X[2]

NOTES:
1. LXT6155 SDH/SONET/ATM Transceiver provides the indication for received frame detection/byte alignment or CMI line-code errors. ROFP/CMIERR (Pin 43) will send out the indication pulses.
2. This feature is not available.

Table 10. Register Settings: Received Output Frame Pulse / CMI Error

Register	Bit	Default	Functional
12	3	0	Frame detection/Byte align enable. This feature must apply during the system configuration. 0 = Disable 1 = Enable
NOTE: In software mode, the recommended method of enabling the receive frame-detection is to set Bit 3 of Register 12 to high, prior to applying data to RTIP/RRING. If the network management system prevents the user from enabling the receive-frame detection prior to applying data to RTIP/RRING, the following sequence of events must happen during configuration. After power up, during SW configuration, you must: 1. Disable the DLOS (Digital LOS) function via Register 12 Bit 4. 2. Enable the receive-output-frame detection via Register 12 Bit 3. 3. Enable DLOS function via Register 12 Bit 4.			

Table 11. Register Settings: Tx Amplitude Trim

Register	Bit	Default	Functional
1	4:1	0000	Transmit amplitude trim 0000 = -21% 1111 = +24%
NOTE: The trim range is from -21% to +24% in 3% steps.			

Table 12. Register Settings: Loss Of Signal (LOS) (Sheet 1 of 2)

Register	Bit	Default	Functional
12	6	1	ALOS1 threshold trim. 0 = Reduced ALOS deassert threshold (-3db) 1 = Nominal ALOS threshold
1. ALOS: Amplitude LOS of coax, CMI mode. 2. DLOS: Digital LOS of fiber, NRZ mode.			

Table 12. Register Settings: Loss Of Signal (LOS) (Sheet 2 of 2)

Register	Bit	Default	Functional
12	5:4	1.1	LOS enable controls (5:4 = ALOS: DLOS) 0 = Disable 1 = Enable
13	2:1	1.0	DLOS2: If there is no transition count within certain period of time, DLOS asserted. 00 = 128 bits ~ 0.8 µs 01 = 512 bits ~ 3.3 µs 10 = 3,112 bits ~ 20 µs 11 = 4,096 bits ~ 26.4 µs ALOS: If the incoming signals fall below the threshold within certain period of time, ALOS asserted. 00 = 2,048 bits 01 = 512 bits 10 = 128 bits 11 = 32 bits
13	0	1	DLOS: Transition density count for deassertion. 0 = 4/32 at least 4 transition/32 bits-sliding window 1 = SONET-compliant: Two valid frames received without LOS events in the interval. ALOS: If line signals rises above asserted threshold of 2 db within certain period of time, ALOS deasserted. 0 = 0 bits 1 = 128 bits
1. ALOS: Amplitude LOS of coax, CMI mode. 2. DLOS: Digital LOS of fiber, NRZ mode.			

Table 13. Register Settings: Minor Setting

Register	Bit	Default	Functional
12	7	0	Combine LOS/LOCK (logical OR) function into LOS pin: 0 = Disable 1 = Enable
13	6:3	0.0.0.0	Frame pulse position: 0000 is for third A2-frame word For the exact position, see the “Functional Description” section of *LXT6155 155 Mbps SDH/SONET/ATM Transceiver Datasheet* (249612).

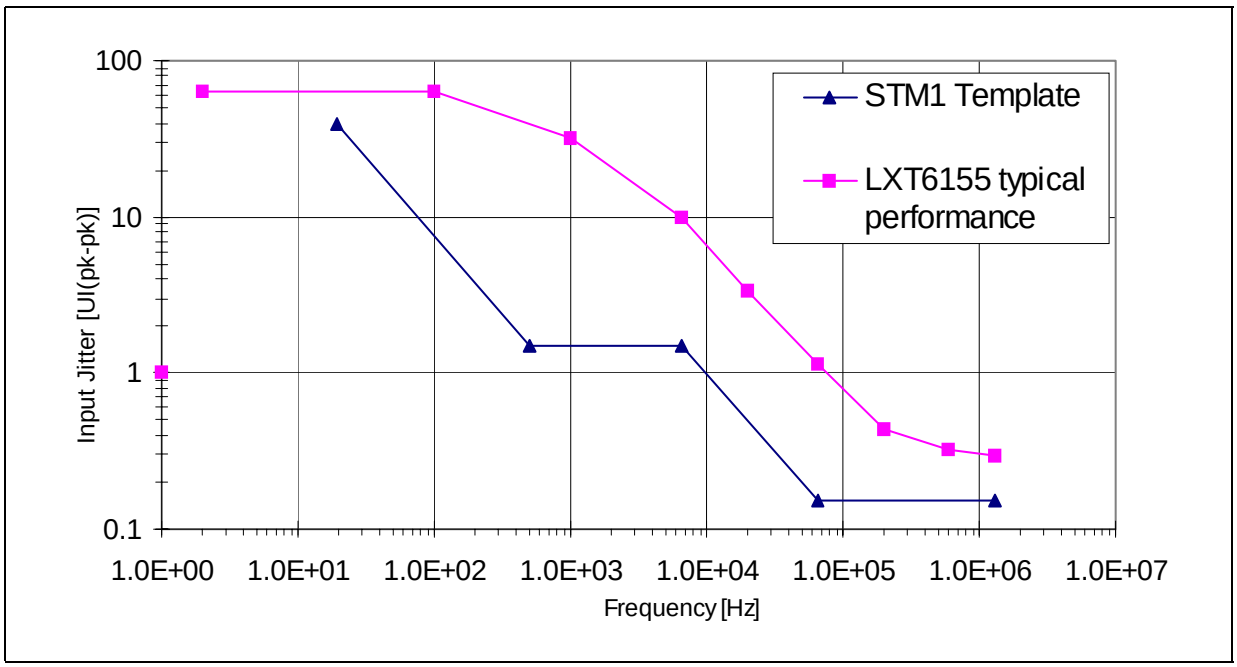
4.0 Jitter Measurement and Jitter Performance

The LXT6155 SDH/SONET/ATM Transceiver is fully compliant with all Bellcore GR-253 and ITU G.958A/G825 (SONET/SDH) jitter tolerance and jitter generation specifications.

4.1 Jitter Tolerance

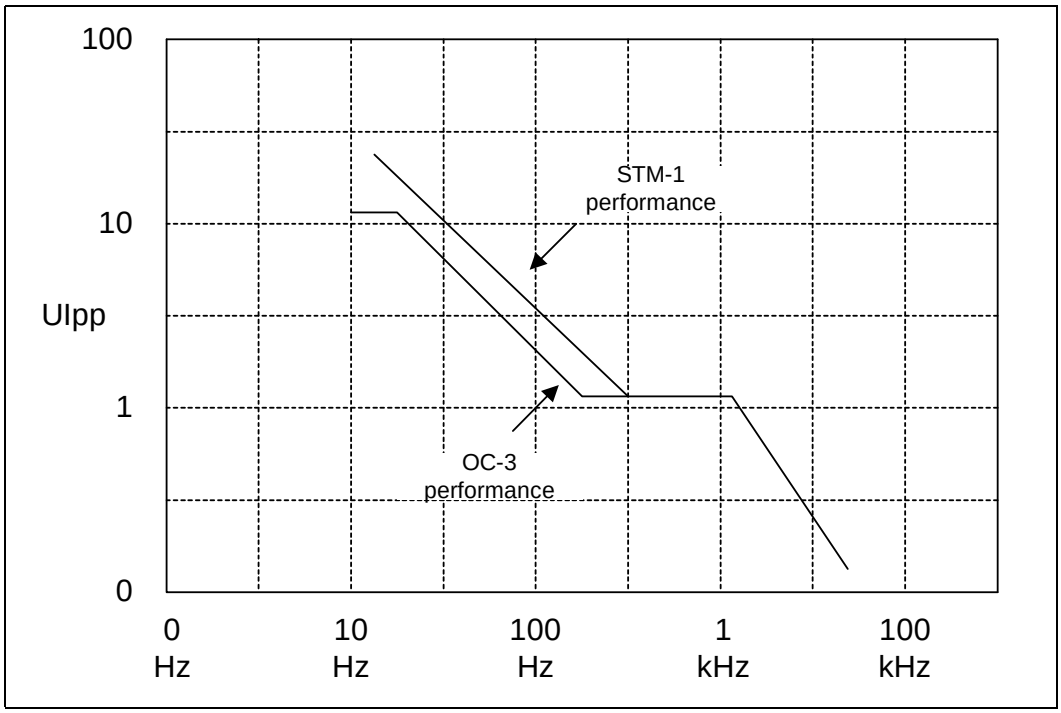
The typical jitter tolerance of the LXT6155 SDH/SONET/ATM Transceiver is shown in Figure 5.

Figure 5. LXT6155 SDH/SONET/ATM Transceiver Typical Jitter Tolerance



The test conditions for measuring jitter tolerance are shown in Figure 6.

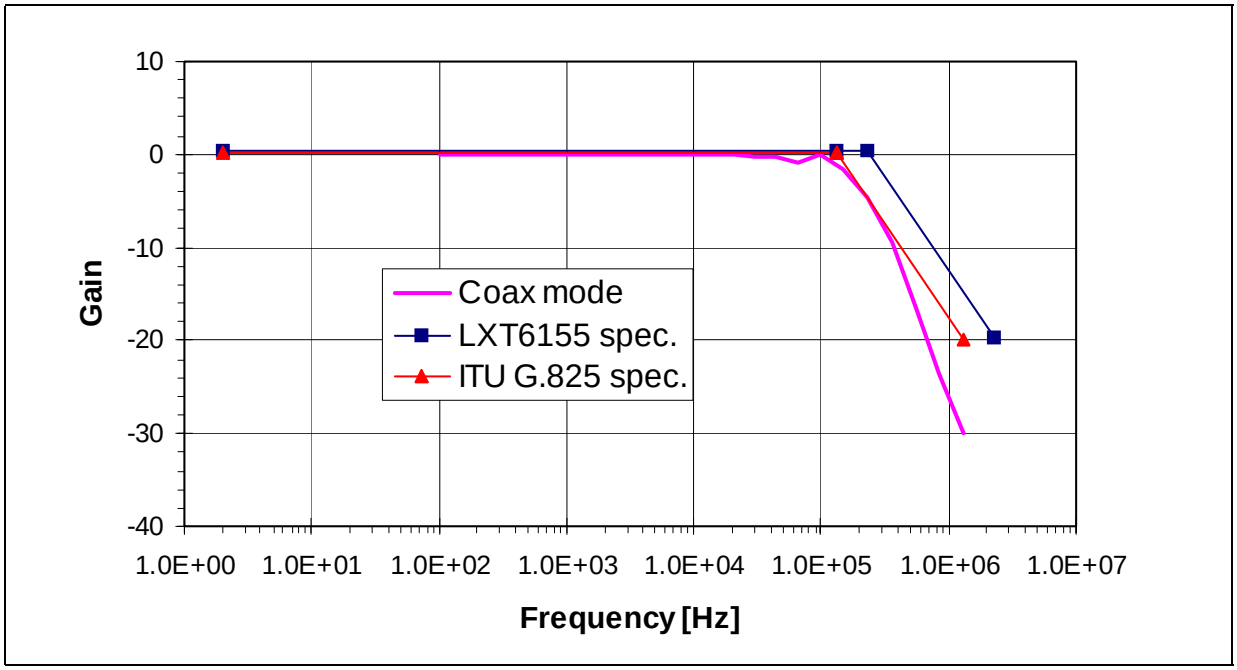
Figure 6. Jitter Tolerance Setup



4.2 Jitter Transfer

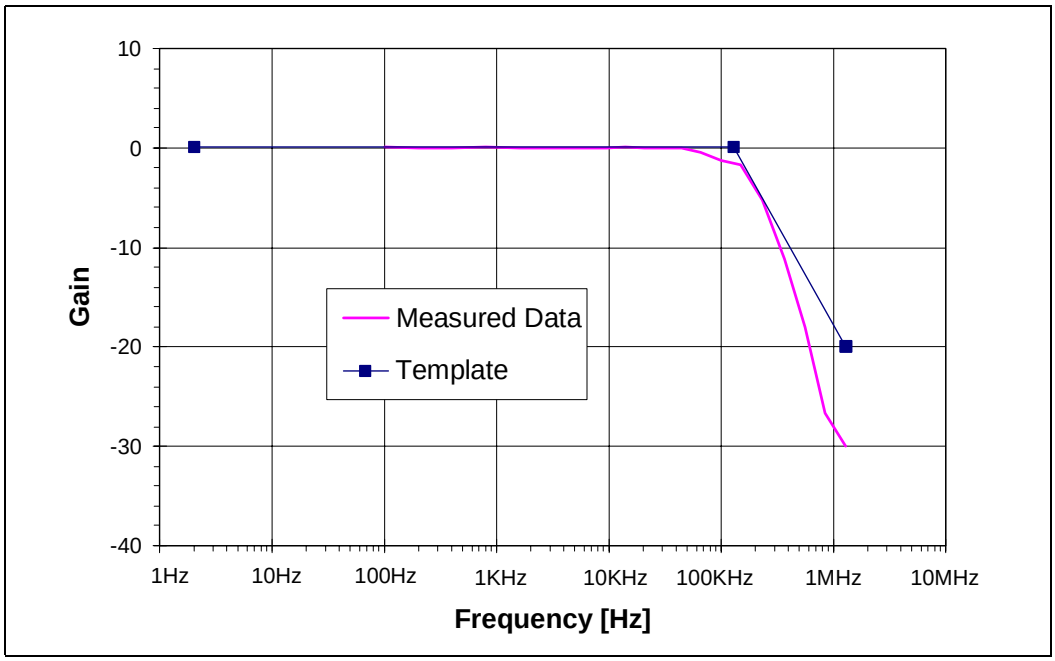
The typical jitter transfer of the LXT6155 SDH/SONET/ATM Transceiver is shown in Figure 7.

Figure 7. LXT6155 SDH/SONET/ATM Transceiver Typical Coax Jitter Transfer



Test conditions for measuring the jitter transfer of the LXT6155 SDH/SONET/ATM Transceiver is shown in Figure 8.

Figure 8. Jitter Transfer Setup



4.3 Jitter Generation

The typical transmit and receive jitter generation of the LXT6155 SDH/SONET/ATM Transceiver is shown in Figure 9 and Figure 10.

Figure 9. LXT6155 SDH/SONET/ATM Transceiver Typical Transmit Jitter Generation

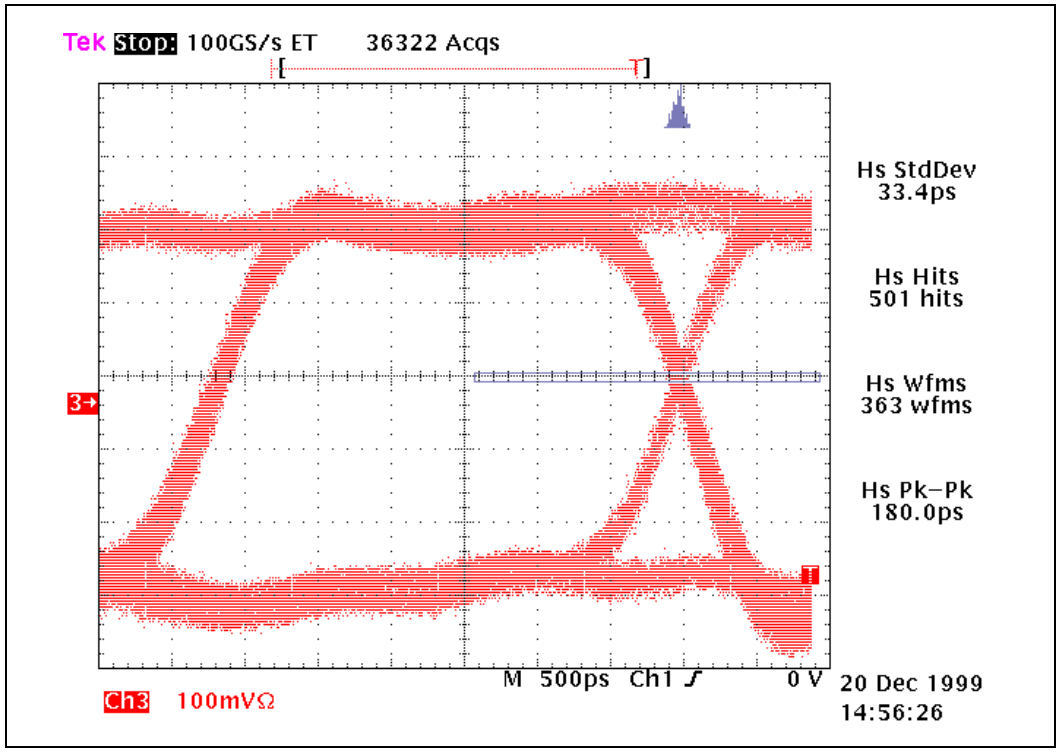
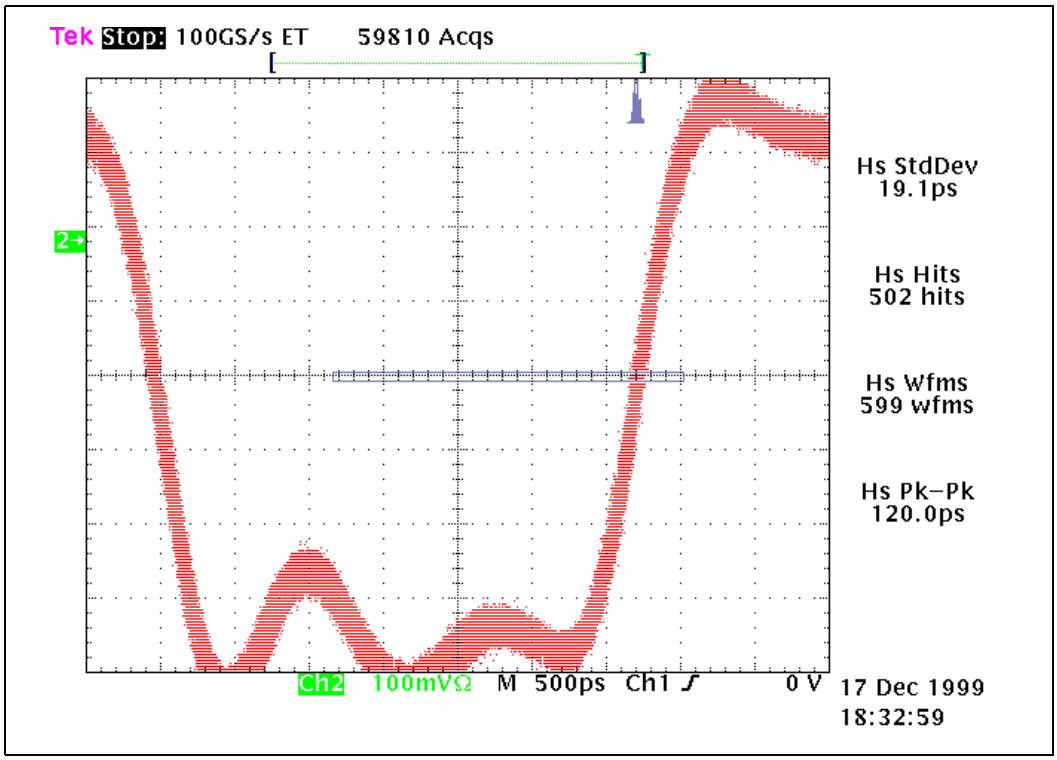


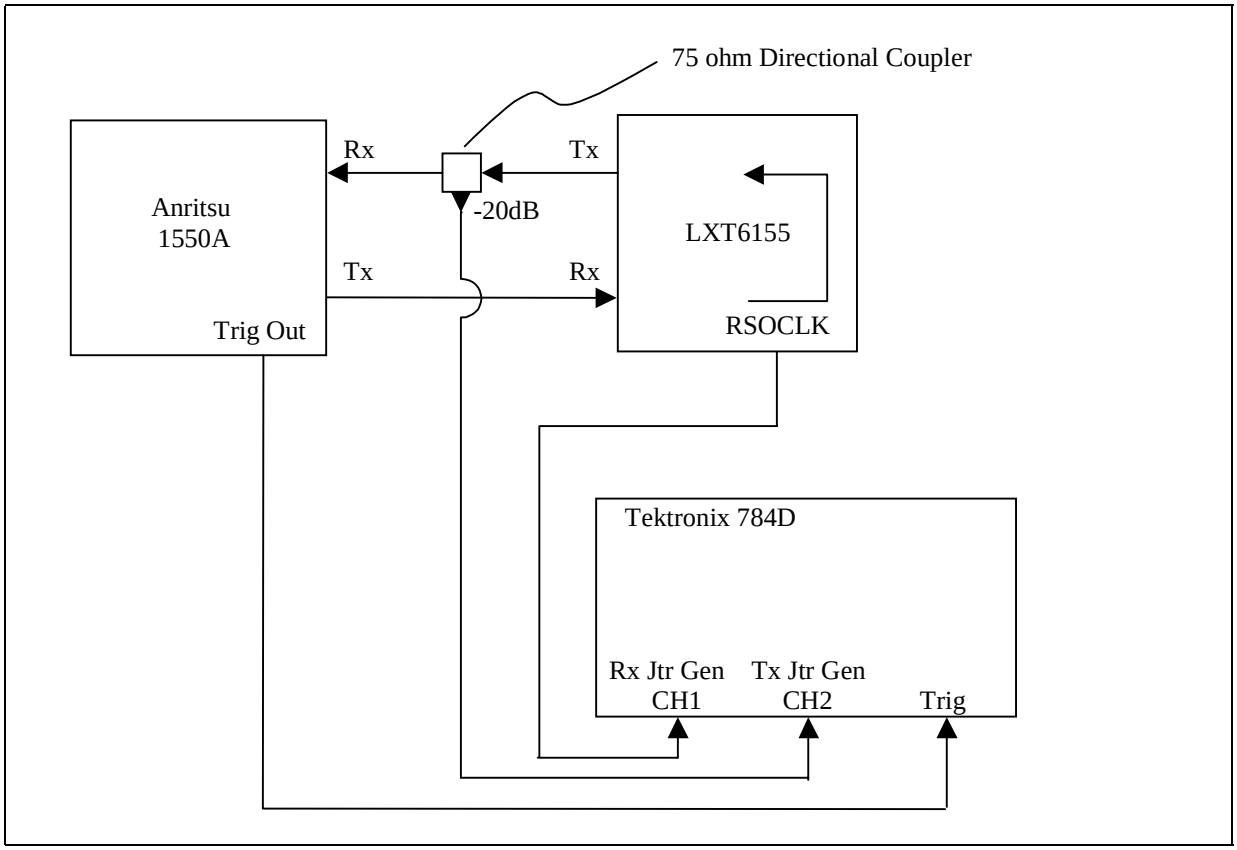
Figure 10. LXT6155 SDH/SONET/ATM Transceiver Typical Receive Jitter Generation



Test conditions for measuring the jitter generation of the LXT6155 SDH/SONET/ATM Transceiver is shown in Figure 11.

5.0 PCB Layout Guidelines

Figure 11. Jitter Generation Setup



High-speed switching circuits produce noise transients that can adversely affect the operation of the LXT6155 SDH/SONET/ATM Transceiver. In order to reduce the effects of these transients, proper PCB layout is critical.

The guidelines presented in this section will help ensure the surrounding environment is as noise-free as possible.

5.1 Ground Planes

It is important to maintain low-impedance, large area ground plane(s) that act as the return path for high-frequency currents. The large ground plane also will help minimize EMI emissions.

Two separate ground planes should be used. One plane is used for digital signals and the other plane for analog. If the LXT6155 SDH/SONET/ATM Transceiver operates in coax mode, it is extremely important to use a separate analog ground plane for noise isolation. The analog ground plane should be as quiet as possible, particularly within the proximity of the RTIP and RRING pins.

All ground planes should converge at the power entry point. All LXT6155 SDH/SONET/ATM Transceiver ground pins should be directly soldered to their respective ground plane to minimize series inductance.

5.2 PECL Traces

The differential signals (PECL) should be smooth, of equal length, and free of abrupt angle changes.

The PECL signal lines must be a controlled impedance of 50 Ω for fiber interface. The lines should be as short as possible. A practical limit is 2” from end to end.

5.3 Power Supply Filtering

The digital and analog VCC planes should be coupled by an inductor. The inductor isolates noisy digital VCC from the quiet analog VCC plane.

Careful capacitive decoupling also must be used. The capacitors must be placed as close to the VCC pins as possible. The other end of the cap must connect directly to the digital ground plane. It is best to keep the capacitor connection trace lengths to a minimum.

Figure 12. Power Supply Filtering