Advance Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU5X31F
Gigabit Ethernet Transceiver

Overview

The LU5X31F is a low-cost, low-power gigabit Ethernet transceiver. It is used for data transmission over fiber or coaxial media in conformance with *IEEE** 802.3z Gigabit Ethernet specification and Fibre Channel *ANSI*† X3T11 at 1.0 Gbit/s and 1.25 Gbits/s.

The transmitter section accepts parallel 10-bit, 8b/10b encoded data that is latched on the rising edge of REFCLK. It also uses this clock to synthesize the internal high-speed serial bit clock. The serialized data is then available at the differential PECL outputs, terminated in 50 Ω or 75 Ω to drive either an optical transmitter or coaxial media.

The receive section receives high-speed serial data at its differential PECL input port. This data is fed to the digital clock recovery section, which generates a recovered clock and retimes the data. The retimed data is deserialized and presented as 10-bit parallel data on the output port. A divided-down version of the recovered clock, synchronous with parallel data bytes, is also available as a TTL compatible output. The receive section recognizes the comma character and aligns the comma containing byte on the word boundary, when ENCDET = 1.

Features

- Designed to operate in Ethernet, fibre channel, *FireWire*‡ or backplane applications.
- Operationally compliant to *IEEE* 802.3z Gigabit Ethernet specification.
- Operationally compliant to Fibre Channel *ANSI* X3T11. Provides FC-0 services at 1.0 Gbit/s—1.25 Gbits/s (10-bit encoded data rate).
- 100 MHz—125 MHz differential or single-ended reference clock.
- 10-bit parallel interface.
- 8b/10b encoded data.
- High-speed comma character recognition (K28.1, K28.5, K28.7) for latency-sensitive applications and alignment to word boundary.
- Two 62.5 MHz receive-byte clocks.
- Single analog PLL design requires no external components for the frequency synthesizer.
- Novel digital data lock in receiver avoids the need for multiple analog PLLs.
- Expandable beyond single-channel SERDES.
- PECL high-speed interface I/O for use with optical transceiver or coaxial copper media.
- Requires one external resistor for PECL output reference level definition.
- Available in both 64-pin MQFP (14 mm) and 64-pin TQFP (10 mm) packages.
- Low-power digital 0.25 µm CMOS technology.
- 3.3 V ± 5% power supply.
- 0 °C—70 °C ambient temperature.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† *ANSI* is a registered trademark of American National Standards Institute.
‡ *FireWire* is a registered trademark of Apple Computer, Inc.

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Functional Description

The LU5X31F transceiver provides for data transmission over fiber or coaxial media at 1.0 Gbits/s to 1.25 Gbits/s. The block diagram of single channel is shown in Figure 1. The input/output designations are given in Table 3.

Transmitter Section

The transmitter accepts 8B/10B encoded bits in 10-bit parallel form and converts to serial format for up to 1.25 Gbits/s transmission. The serial nonreturn to zero (NRZ) bits are shifted out of the device at a maximum rate of 1.25 Gbits/s. Internally, the device uses two parallel shift registers that operate at half rate (i.e., a maximum of 625 MHz) for reduced power consumption. The two shift registers drive the PECL output buffer in an interleaved manner to construct the 1.25 Gbits/s output data stream.

The typical transmit and receive high-speed I/O interfacing is shown in Figures 8 and 9, for a single-channel application.

The transmit shift register and other circuits are driven with clocks generated from a 500 MHz—625 MHz internal clock. This internal clock is sourced from a voltage-controlled oscillator (VCO) that is locked to the external reference of 100 MHz—125 MHz. The internal transmit phase-lock loop multiplies the frequency of the input reference clock by a factor of 5, and controls the transmit jitter bandwidth with appropriate design of the jitter transfer function. The transmit phase-lock loop generates multiple clock phases that are all used by each of the four receiver circuits. The clock phases are derived from the transmit VCO.

Receiver Section

The receiver circuit extracts the clock from and retimes the serial input data. The data is input to the receiver on differential PECL buffers. External termination resistors are supplied by the user in accordance with *ANSI* standard, X3T11. The serial differential inputs, HDINP and HDINN, are ac-coupled to the device and internally biased to the PECL input common-mode range center. See Figures 8 and 9 for the typical termination of the transmission lines.

The receiver data retiming circuit uses a digital timing recovery loop that compares the phase of the input data to multiple phases of the on-device VCO in the transmit section. One of the phases is chosen to retime the receive data. A digital low-pass filter is used in the timing recovery loop to reject jitter from the data input. A novel phase interpolation circuit permits the retiming clock's phase to be stepped with fine resolution for precise alignment of the sampling clock within the data eye. Use of this digital data locking scheme avoids the use of multiple analog phase-lock loops on-device that can potentially injection lock to one another when expanded to multiple receivers. Additionally, the digital data locking loop maintains precise loop dynamics, hence, the jitter transfer function is process and temperature independent.

Lock to Reference

The receive circuit has two modes of operation, lock to reference, and lock to data with retiming. When no data or invalid data is present on HDINP and HDINN input pins, the user can program the device to ignore the input data by setting LCKREFN equal to logic 0. In this mode, neither the PECL input buffer nor the RX parallel data bus toggles. In normal operation, LCKREFN is a logic one and the receiver attempts to lock to incoming data. If the input data is invalid or outside the normal ± frequency range, the receive digital PLL will simply ramp the phase of the output clock until it locks to data.

Table 1. Receiver Circuit Operating Modes*

Mode	Lock to Reference	Lock to Receive Data
LCKREFN = 1 (normal operation)	Not applicable.	Continually attempts to lock to data.
LCKREFN = 0	Lock to clock, output data does not toggle. Disable PECL input buffer.	Not applicable.

* REFCLK requirements are given in Table 4 and receive PLL Specifications are given in Table 5.

Functional Description (continued)

Byte Alignment

When ENCDET = 1, the LU5X31F recognizes the comma character and aligns this 10-bit character to the word boundary, bits RX[0:9].

COMDET = 1 when the parallel output word contains a byte-aligned comma character. The COMDET flag will continue to pulse a logic 1 whenever a byte-aligned comma character is at the parallel output port, independent of ENCDET. When ENCDET = 0, there are two possible scenarios, depending upon when the comma character is received:

1. If byte-alignment had been previously achieved when ENCDET had been a logic 1, the COMDET flag will continue to pulse a logic 1 whenever a byte-aligned comma character is at the parallel output port. If a comma character occurs that is not on the word boundary, no attempt will be made to align this comma character, and the COMDET flag will remain at a logic 0.
2. If byte-alignment had **not** been previously achieved when ENCDET had been a logic 1, then the first (and only the first) comma character received will be aligned to the word boundary. COMDET will pulse when the comma character is aligned to the word boundary.

Parallel Output Port

Timing for the parallel output data and the 62.5 MHz receive-byte clock is given in Table 14.

Two low data-rate, receive-byte clocks are available as outputs during use of the parallel output port in 10-bit mode. RXCLK1 is the receive-byte clock used by the protocol device to register bytes 0 and 2. RXCLK0 is the receive-byte clock used by the protocol device to register bytes 1 and 3, and it is 180 degrees out of phase with RXCLK1. Both RXCLK1 and RXCLK0 can be stretched during byte alignment but not truncated or slivered. The maximum allowable frequency of these two clocks under all circumstances, excluding start-up, will not exceed 80 MHz. The start-up time is specified as 1 ms.

Loopback Mode Operation

A control signal input, EWRAP, selects between two possible sets of inputs: normal data (HDINP, HDINN) or internal loopback data. When EWRAP = 1, the serial output ports, HDOUTP and HDOUTN, remain active. The serial transmit data prior to the PECL output driver is directed to the data recovery circuit, where the clock is recovered and data is resynchronized to the recovered clock. Retimed data and clock then go to the serial-to-parallel converter.

Table 2. Definition of Bit Transmission/Reception Order

Serial Transmit/ Receive Rate	TX[9:0]	RX[9:0]
1.0 Gbits/s to 1.25 Gbits/s	TX[0] bit serially transmitted first at HDOUTP, HDOUTN.	RX[0] bit received first at serial inputs, HDINP, HDINN.

Functional Description (continued)

Powerup Sequence

The power ramp time for the LU5X31F is specified at V_{DD} > 2.7 V within 20 µs of start-up. Once 2.7 V is reached, the device is held in reset for 15 µs—70 µs. The REFCLK must be active and within specification at this point and remain active while the device is powered up, unless in Reset.

When signals RESETN, BYPPLL, and LPWR are all low, the following start-up sequence occurs:

1. 0 µs—32 µs, the analog PLL is held at minimum frequency to allow dc bias to settle.
2. 32 µs—262 µs, the analog PLL has locked in and receiver analog circuits start to lock in.
3. 262 µs—326 µs, the receiver analog circuits are locked; receiver starts to lock onto incoming data.
4. After 358 µs, the receiver is locked onto incoming data and can be viewed at the parallel output ports. The comma-detect circuit is enabled at this point allowing byte alignment if ENCDET = 1.

Device Reset

The RESETN input to the device is an active-low. When activated with a pulse duration of 1 µs, the RESETN signal globally resets the device and the following is performed:

1. The single analog PLL is forced to operate at the minimum frequency possible for its VCO. The PLL will not be locked in this condition.
2. The HDOUTP, HDOUTN outputs are forced to a PECL logic 0.
3. The deserializer clocks are reset, input data at HDINP, HDINN is ignored, and the RX[9:0] signals remain in their previous state.
4. The phase interpolation/selection circuits are deactivated and the selected phase is reset.
5. The receiver digital low-pass filter in the DPLL is reset. Normally, a reset is not necessary for correct operation, although a reset can aid rapid lock-in of the internal PLL circuitry. This signal is internally pulled high.

Functional Description (continued)

Block Diagram

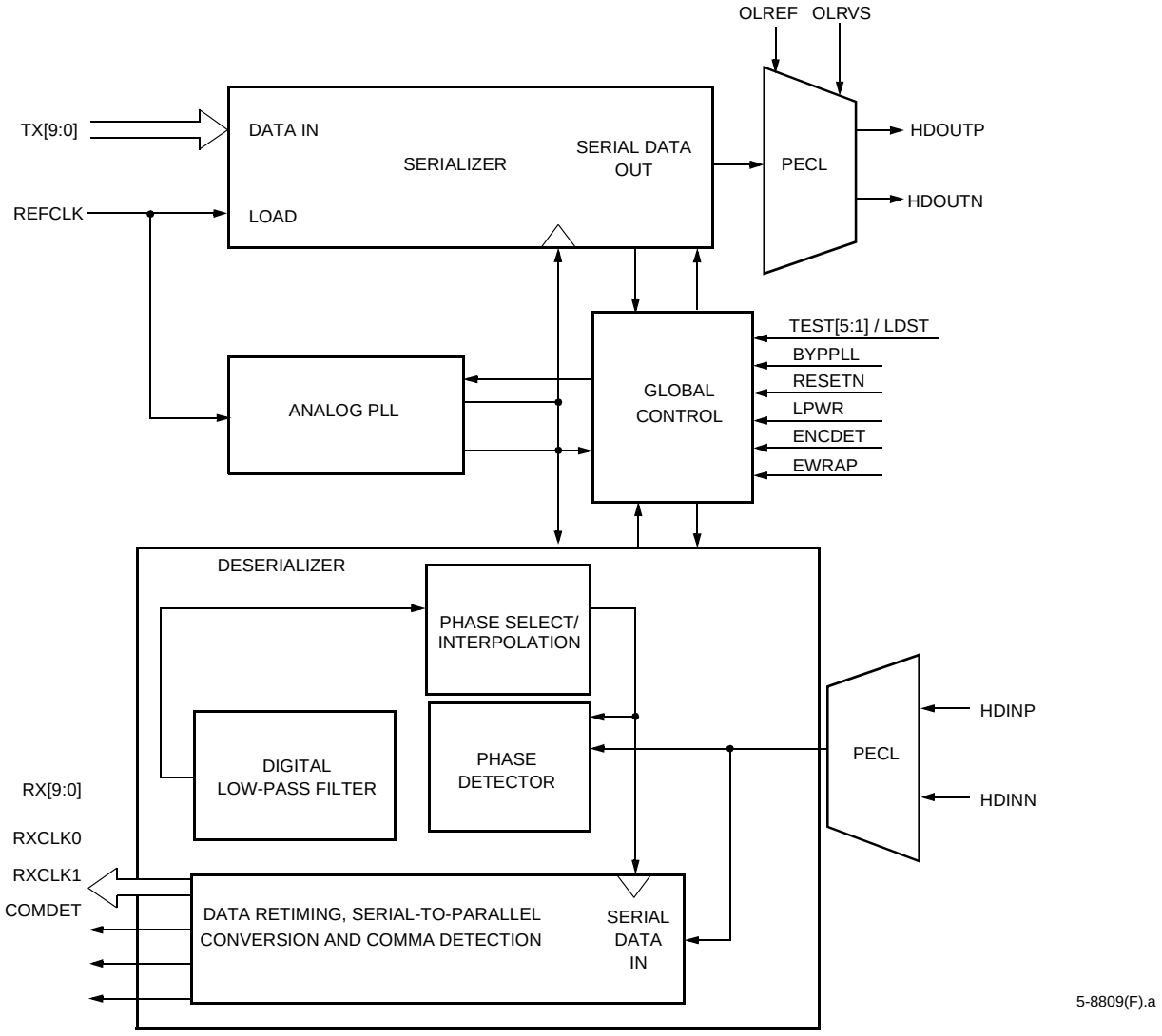

Figure 1. LU5X31F Single-Channel Gigabit Ethernet Transceiver Functional Diagram

Input/Output Information

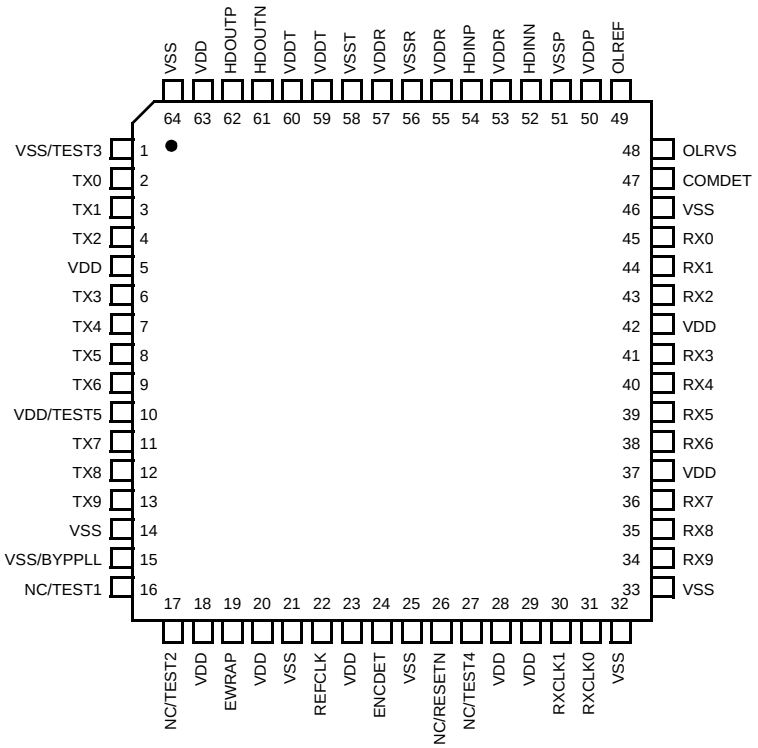

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Figure 2. 64-Pin MQFP Package (14 mm) Pinout

Input/Output Information (continued)

Table 3a. I/O Channel Signal Description

PIN	Name	I/O	Level	Description
2—4, 6—9, 11—13	TX[9:0]	Input	TTL/ CMOS	**Transmit Data.** One 10-bit, parallel 8b/10b encoded data byte clocked-in on the rising edge of REFCLK. TX0 is the leading LSB.
34—36, 38—41, 43—45	RX[9:0]	Output	TTL/ CMOS	**Receive Data.** One 10-bit parallel 8b/10b encoded data byte clocked-out on the alternate rising edges of RXCLK0, RXCLK1. RX0 is the leading LSB. Any receive code-group containing a comma character is clocked by the RXCLK1.
22	REFCLK	Input	TTL/ CMOS	**Reference Clock.** This 100 MHz—125 MHz clock is used to latch TX[9:0] data into the LU5X31F for transmission and is used by the transmitter PLL to generate the 1.0 Gbits/s—1.25 Gbits/s serial data. REFCLK has a ±100 ppm tolerance requirement.
31	RXCLK0	Output	TTL/ CMOS	**Receive Clock 0.** 62.5 MHz used to latch odd-numbered code-groups in the receive data stream. This clock may be stretched during code-group alignment but should not be truncated or slivered.
30	RXCLK1	Output	TTL/ CMOS	**Receive Clock 1.** 62.5 MHz used to latch even-numbered code-groups in the receive data stream. This clock may be stretched during code-group alignment but should not be truncated or slivered. RXCLK1 is 180 degrees out of phase with RXCLK0. Note that the comma pattern (contained in groups K28.1, K28.5, K28.7) is constrained to only appear in even-numbered code-group positions.
62	HDOUTP	Output	PECL	**Transmit Data.** Positive differential PECL serialized transmit data at 1.25 Gbits/s; requires external transmission line termination, as given in Figure 8.
61	HDOUTN	Output	PECL	**Transmit Data.** Negative differential PECL serialized transmit data at 1.25 Gbits/s; requires external transmission line termination, as given in Figure 8.
54	HDINP	Input	PECL	**Receive Data.** Positive differential PECL serialized receive data at 1.25 Gbits/s; requires external transmission line termination, as given in Figure 8.
52	HDINN	Input	PECL	**Receive Data.** Negative differential PECL serialized receive data at 1.25 Gbits/s; requires external transmission line termination, as given in Figure 8.
47	COMDET	Output	TTL/ CMOS	**Comma Detect.** Asserted high for a full RXCLK1 cycle to indicate that a comma code-word is present on RX[9:0].
24	ENCDET	Input	TTL/ CMOS	**Enable Comma Detect.** Enables COMDET and code-word synchronization when set high. When low, disables COMDET and maintains current code-word alignment.
19	EWRAP	Input	TTL/ CMOS	**Enable Wrap.** Enables the LU5X31F to internally loop serialized transmit data to the deserializer. HDOUTP and HDOUTN outputs remain active.

Input/Output Information (continued)

Table 3b. I/O Control/PLL Interface Descriptions

Pin	Name	I/O	Level	Description
49	OLREF	Input/Output	Analog	**Output Level Reference.** PECL level set resistor terminal 1.
48	OLRVS	Input/Output	Analog	**Output Level Ground.** PECL level set resistor terminal 2.
26	RESETN	Input	TTL/CMOS	**RESETN.** Active-low, internally pulled high.
10	TEST5	Input/Output	TTL/CMOS	**Global Test Control Input/Output.**
1, 16, 17, 27	TEST[4:1]	Input	TTL/CMOS	**Factory Test Pins.** Internally pulled low.
15	BYPPLL	Input	TTL/CMOS	**Test Control-PLL Bypass Mode.**

Table 3c. Power Connections

Pin	Name	Description
5, 10, 18, 20, 23, 28, 29, 37, 42, 63	V_{DD}	**Digital Power.**
53, 55, 57	$V_{DD}R$	**High-Speed Receive Analog Power.**
59, 60	$V_{DD}T$	**High-Speed Transmit Analog Power.**
50	$V_{DD}P$	**PLL Power.**
1, 14, 15, 21, 25, 32, 33, 46, 64	V_{SS}	**Digital Ground.**
56	$V_{SS}R$	**High-Speed Receive Analog Ground.**
58	$V_{SS}T$	**High-Speed Transmit Analog Ground.**
51	$V_{SS}P$	**PLL Ground.**

Electrical Specifications

Transmitter

Table 4. Reference Clock Specifications (REFCLK)

Parameter	Min	Max	Unit
Frequency Range	100	125	MHz
Frequency Tolerance	–100	100	ppm
Duty Cycle*	40	60	%
Rise Time (PECL)	—	0.8	ns
Fall Time (PECL)	—	0.8	ns
Rise Time (TTL/CMOS)	—	1.5	ns
Fall Time (TTL/CMOS)	—	1.5	ns
In-band Jitter 1 Gbit/s—1.25 Gbits/s	—	30	ps p-p
Out-of-Band Jitter	—	50	ps p-p

* Measured at 50% amplitude point.

Table 5. PLL Characteristics

Parameter	Min	Typ	Max	Unit
Bandwidth	—	1.5	—	MHz
Jitter Peaking	—	0.5	—	dB
Lock Time	—	—	230	µs

Table 6. Output Jitter at 1.0 Gbit/s—1.25 Gbits/s Data Rate

Parameter	Min	Max	Unit
Deterministic	—	0.08	UI p-p
Random	—	0.12	UI p-p
Total	—	0.2	UI p-p

Electrical Specifications (continued)

Receiver

Table 7. Input Data Rate

Parameter	Min	Max	Unit
Frequency Range	1.0	1.25	Gbits/s
Frequency Tolerance with REFCLK	–100	100	ppm

Table 8. Data Lock Characteristics

Parameter	Min	Typ	Max	Unit
Bandwidth	0.3 *	—	1†	MHz
Jitter Peaking†	—	0.5	—	dB
Lock Time*	—	—	2	µs

* Data pattern: 111110000 . . .
† Data pattern: 101010 . . .

Table 9. Power Dissipation*

Parameter	Min	Max	Unit
Power	—	750	mW

* Depending on application (PCB layout, etc.)

Table 10. dc Electrical Specifications*

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, $V_{DD}P$	—	3.135	3.3	3.465	V
Output Low	V_{OL}	—	0	—	0.6	V
Output High	V_{OH}	—	2.4	—	V_{DD}	V
Input Low	V_{IL}	—	0	—	0.8	V
Input High	V_{IH}	—	2.0	—	V_{DD}	V
Diff. PECL Output		Load, as in Figure 8.	800	—	—	mV
Diff. PECL Input		Source configuration, as in Figure 8.	400	—	1600	mV

* Depending on application (PCB layout, etc.)

Table 11. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	3.135	3.465	V
TTL High Input Voltage	3.0	3.6	V
PECL Output Current	—	16	mA
Junction Operating Temperature	0	125	°C
Storage Temperature	–65	150	°C

Timing Characteristics

Serial Timing

Table 12. Serial Output Timing Levels

Description	Min	Typ	Max	Unit
Rise Time 20%—80%	0.17	0.2	0.22	ns
Fall Time 80%—20%	0.17	0.2	0.22	ns
Common Mode	$V_{DD}/2 - 0.1$	$V_{DD}/2$	$V_{DD}/2 + 0.1$	V
Differential Swing	0.8	—	1.6	V p-p
Load (See Table 16.)	50	—	75	Ω

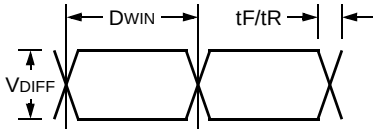

Figure 3. Serial Interface Timing

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Table 13. Serial Input Interface Timing

Description	Min	Max	Unit
Rise Time (tR)	150	225	ps
Fall Time (tF)	150	225	ps
Differential Swing (V_{DIFF})	0.4	1.6	V p-p
Source Impedance	50	75	Ω
Data Eye Opening (D_{WIN})	320	—	ps

Timing Characteristics (continued)

Receiver Section Timing

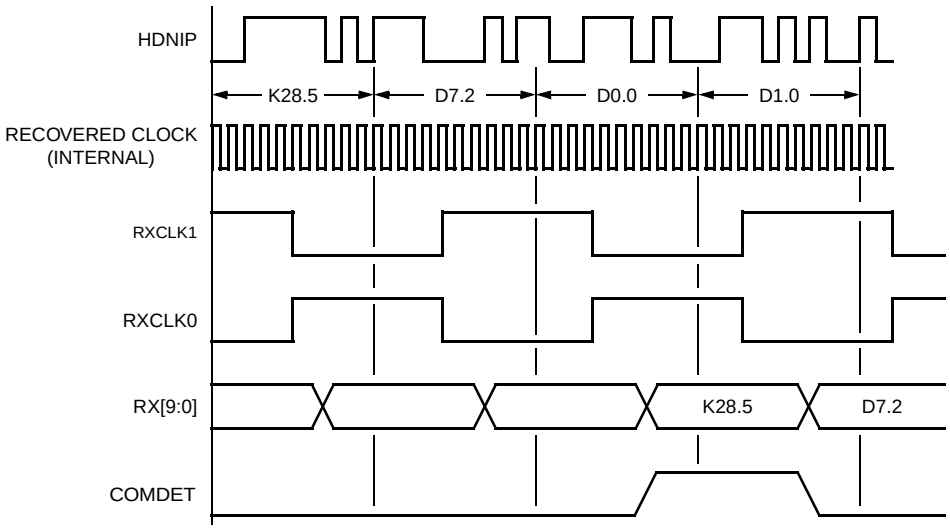

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Figure 4. Receiver Section Timing

Receiver Port Timing

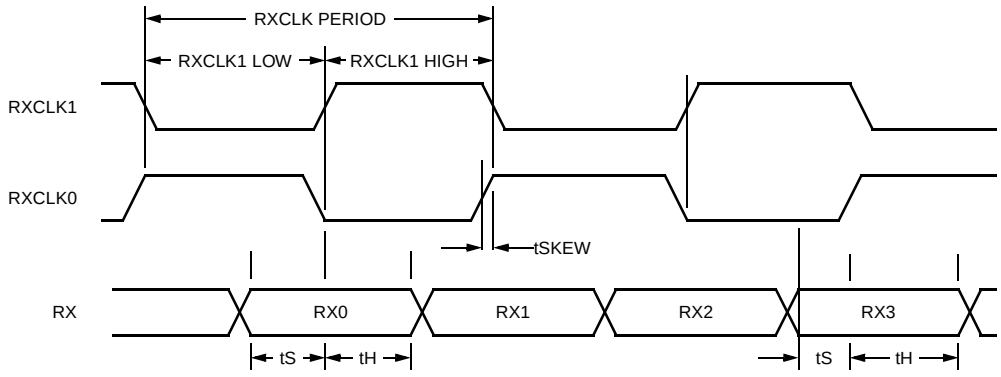

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Figure 5. Receiver Port Timing

Table 14. Receiver Parallel Port Timing

Symbol	Parameter	Min	Max	Unit
—	RXCLK[1:0] Frequency*	—	62.5	MHz
—	RXCLK[1:0] Low	7.0	9.0	ns
—	RXCLK[1:0] High	7.0	9.0	ns
tR/F	RXCLK[1:0] (0.4 V to 2.6 V)†	0.2	0.5	ns
tR/F	Data Output (0.4 V to 2.6 V)†	0.2	0.5	ns
tS	Setup Time	3.0	—	ns
tH	Hold Time	2.0	—	ns
tSKEW	Skew	—	1.0	ns

* 1.25 Gbits/s.
† 0.5 pF load.

Timing Characteristics (continued)

Transmitter Section Timing

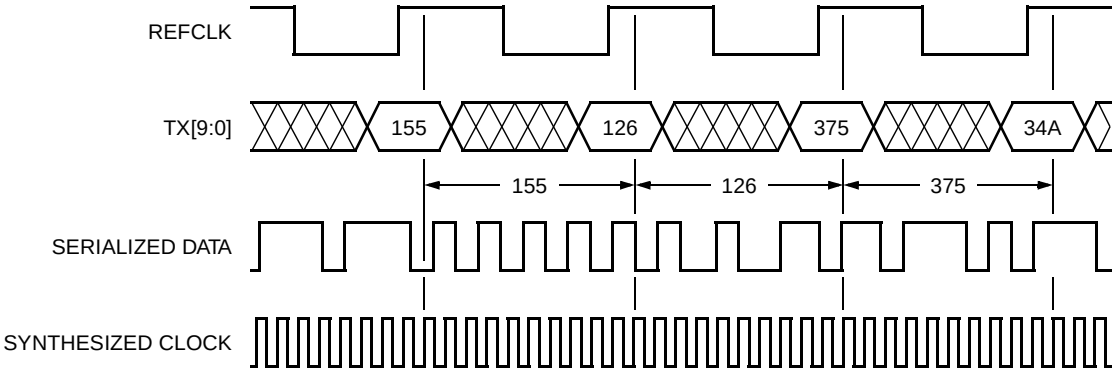

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Figure 6. Parallel Interface Transmit Timing

Table 15. Transmitter Timing at Parallel Interface

Description	Min	Max	Unit	Conditions
Data Setup	2	—	ns	With Positive Edge REFCLK
Data Hold	2	—	ns	With Positive Edge REFCLK
Rise Time	—	1	ns	—
Fall Time	—	1	ns	—

Application Section

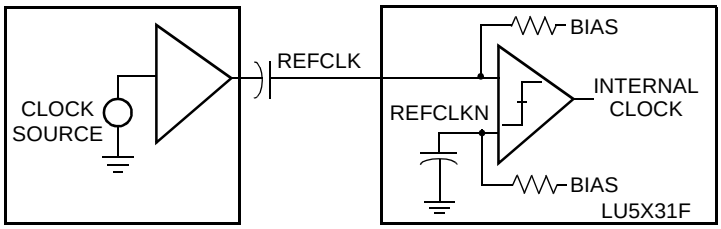

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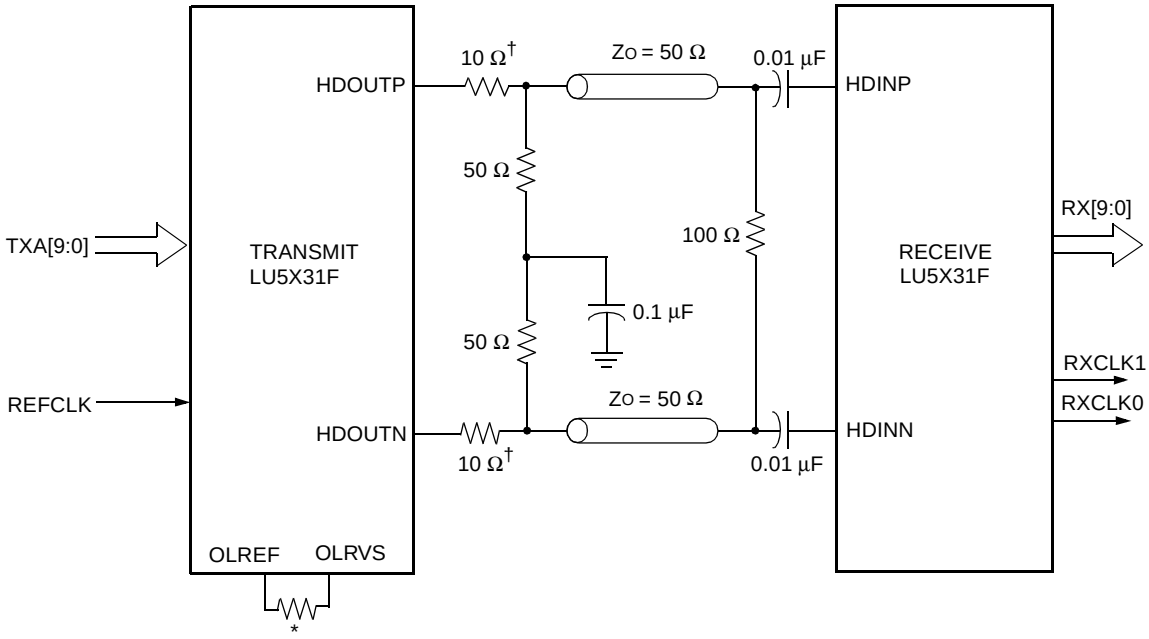
Figure 7. Reference Clock Connections with Single-Ended Source



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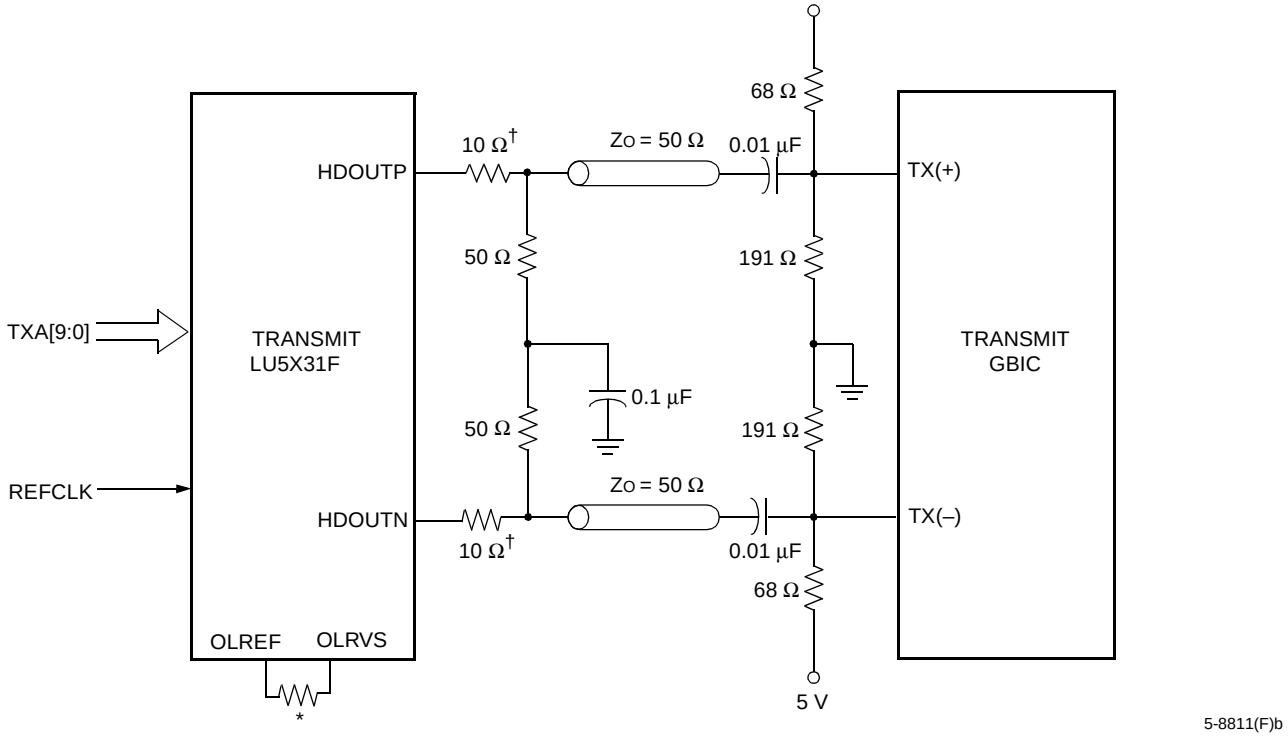
* External resistor connected between OLREF and OLRVS. See Table 16 for external resistor value required for differential output swing.
† Damping resistor, maximum = 10 Ω.

Figure 8. Typical Termination for a Single-Channel, High-Speed Serial Transmit-and-Receive Port in a 50 Ω Backplane Application

Application Section (continued)



* External resistor connected between OLREF and OLRVS. See Table 16 for resistor value vs. termination impedance and output swing.
† Damping resistor, maximum = 10 Ω.

Figure 9. Typical Termination for a Single-Channel, High-Speed Serial Transmit Port Interfacing a 5 V GBIC Transceiver

Table 16. External Resistor Value vs. Differential Output Level Viewing

Resistor Value (Ω)	Termination Impedance (Ω)	Differential Output Voltage (V)
7.5 K/11.25 K	50/75	0.8
5 K/7.5 K		1.2
4 K/6 K		1.6

Test Modes

Note: Test modes are intended for manufacture test only and are not guaranteed to be operational. They may be modified or eliminated without prior notice.

The device has per-channel test modes as well as global test modes. The bypass PLL, BYPPLL, is a global test input because it modifies the operation of the analog PLL. Test bits TEST[4:1] generally operate in the localized mode. The LDST[A:D] inputs are enable signals that permit the TEST[4:1] signals to be injected into a particular channel.

For example, if LDST = 1, the TEST[4:1] signals directly control the test modes in the A channel. Once LDST = 0, the previous values of TEST[4:1] are held for the A channel. The TEST[4:1] signals control the four channels (A, B, C, D) via level-sense latches that are gated with the LDST[A:D] inputs. TEST[5] is a global test pin used for both injection of signals as well as for monitoring points within the device.

Table 17. Test Modes

Global	Local Test Configuration				Global	Operation
BYPPLL	TEST1	TEST2	TEST3	TEST4	TEST5	
0	1	1	1	1	X	Normal operation.
0	1	1	1	0	Output	Analog PLL feedback signal viewed at TEST5 pin.
0	1	1	0	1	X	Transceiver operates normally except RX[9:0] output is from digital filter, not the serial data.
0	1	1	0	0	Output	Transceiver operates normally except RX[9:0] output is from digital filter and the analog PLL feedback signal is viewed at TEST5 pin.
0	1	0	1	P	P	Digital filter forced to count. Pulses applied at TEST4 increment accumulator; pulses at TEST5 decrement accumulator.
0	1	0	0	P	P	RX[9:0] output is from digital filter, not the serial data. Digital filter forced to count. Pulses applied at TEST4 increment accumulator; pulses at TEST5 decrement accumulator.
0	0	1	1	1	X	Parallel loopback. TX[9:0] = RX[9:0]. RX[9:0] remains active.
0	0	1	1	0	Output	Parallel loopback. TX[9:0] = RX[9:0] and analog PLL feedback signal viewed at TEST5 pin. RX[9:0] remains active.
0	0	1	0	1	X	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset.
0	0	1	0	0	Output	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5 pin.
0	0	0	1	1	X	Transmitter is held in reset. BYPPLL overrides this reset.

Test Modes (continued)

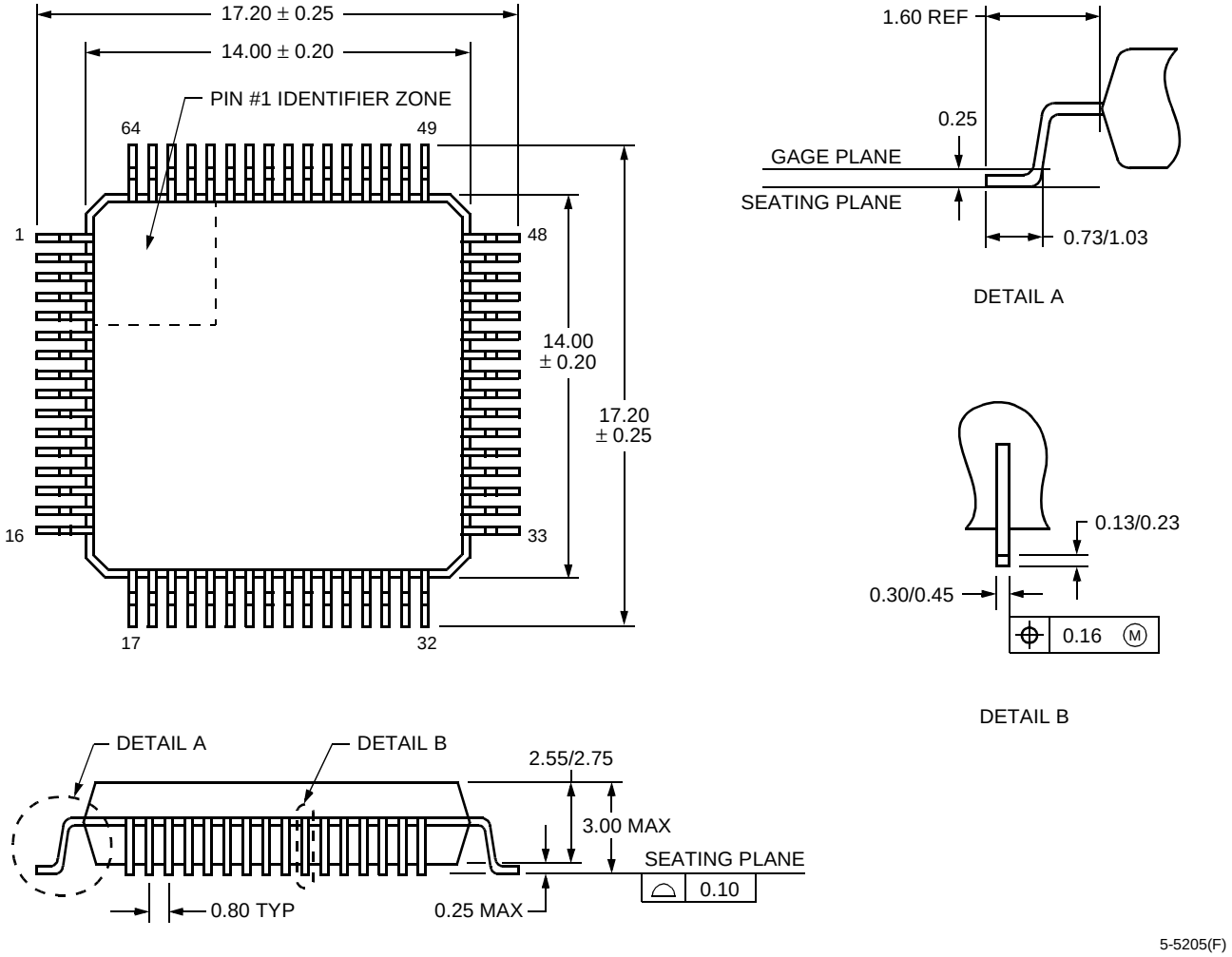
Table 17. Test Modes (continued)

Global	Local Test Configuration				Global	Operation
BYPPLL	TEST1	TEST2	TEST3	TEST4	TEST5	
0	0	0	1	0	Output	Transmitter is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5 pin.
0	0	0	0	1	X	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data.
0	0	0	0	0	Output	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data. Analog PLL feedback signal viewed at TEST5 pin.
1	X	X	1	C-0	C-90	Analog PLL is bypassed for low-speed functional test. A low-speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5X REFCLK, but here REFCLK is lowered to about 1 MHz.
1	X	X	0	C-0	C-90	Analog PLL is bypassed for low-speed functional test. A low-speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5X REFCLK, but here REFCLK is lowered to about 1 MHz. RX[9:0] output is from digital filter, not the serial data.

Outline Diagrams

64-Pin MQFP

Dimensions are in millimeters.



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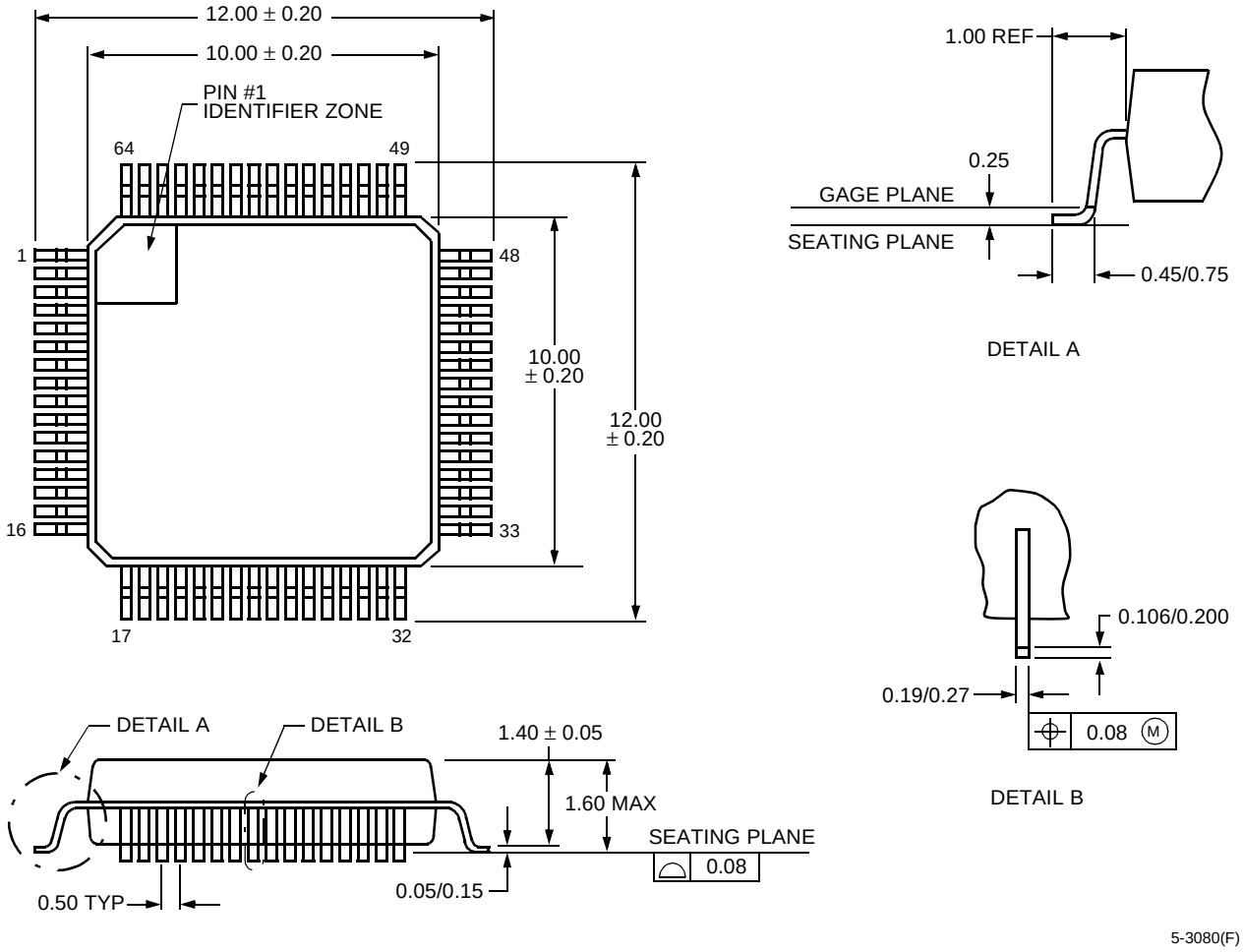
Outline Diagrams (continued)

64-Pin TQFP

Dimensions are in millimeters.



5-3080(F)

Ordering Information

Device Code	Comcode	Package	Temperature
LU5X31F	108497843	64-pin MQFP	0 °C—70 °C

For additional information, contact your Microelectronics Group Account Manager or the following:
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