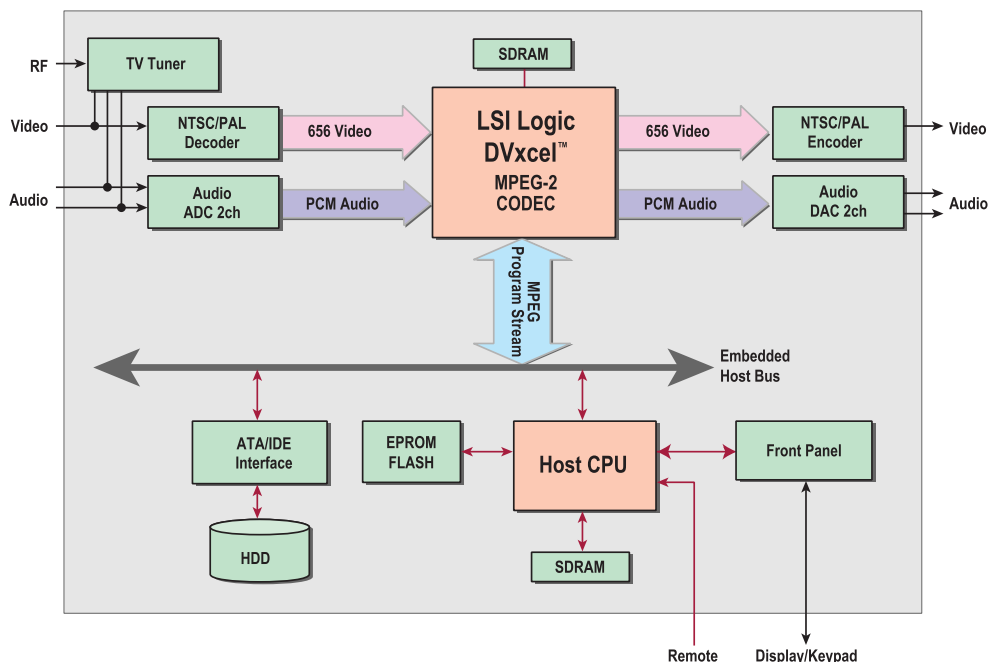


LSI Logic DVxcel™ Advanced MPEG-2 Video and System Codec for Consumer Applications

DVxcel

OVERVIEW

The LSI Logic DVxcel™ MPEG-2 video codec is a high-quality, single-chip digital video processing solution that is ideal for consumer digital recordable products, including DVD recorders. In addition to encoding and decoding, LSI Logic DVxcel has the capability to simultaneously encode and decode MPEG-2 video, enabling low-cost digital video recorder (DVR) applications. LSI Logic DVxcel, the latest in the DVx family of codecs, is based on LSI Logic's fourth-generation video processor architecture. LSI Logic DVxcel has been optimized, both in hardware design and functionality for high-quality, low-cost digital consumer recordable applications. Using LSI Logic's proven PerfectView® encoding algorithm, LSI Logic DVxcel delivers the highest-quality video encoding of any consumer-based solution.



LSI Logic DVxcel™ Digital Video Recorder (DVR) System Block Diagram



KEY FEATURES:

- Real-time MPEG-2 ML@MP video and system encoding
- Simultaneous encode and decode of MPEG-2 video streams with audio synchronization
- Single-pass, variable bit rate (VBR) and constant bit rate (CBR) encoding
- Multiple, programmable horizontal resolutions
- On-chip program stream multiplexing of compressed or uncompressed audio
- On-chip DVD-VR real-time read/write (RTRW) system level formatting
- MPEG-2 ML@MP video and system decoding



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DEVICE FEATURES:

Optimized for embedded designs, LSI Logic DVxcel features the following hardware interfaces:

- Flexible 16/32-bit host interface
- Host DMA target or primary 8-bit hardware I/O port for bitstream data transfers
- Secondary 8-bit hardware port for bitstream transfers
- Tertiary 8-bit hardware port for bitstream transfers
- 8- or 10-bit ITU-656 video input port
- 8-bit ITU-656 video output port
- Serial audio interfaces for audio capture and playback

LSI Logic DVxcel is based around a 110 MHz Micro-SPARC® RISC core and includes special hardware to implement:

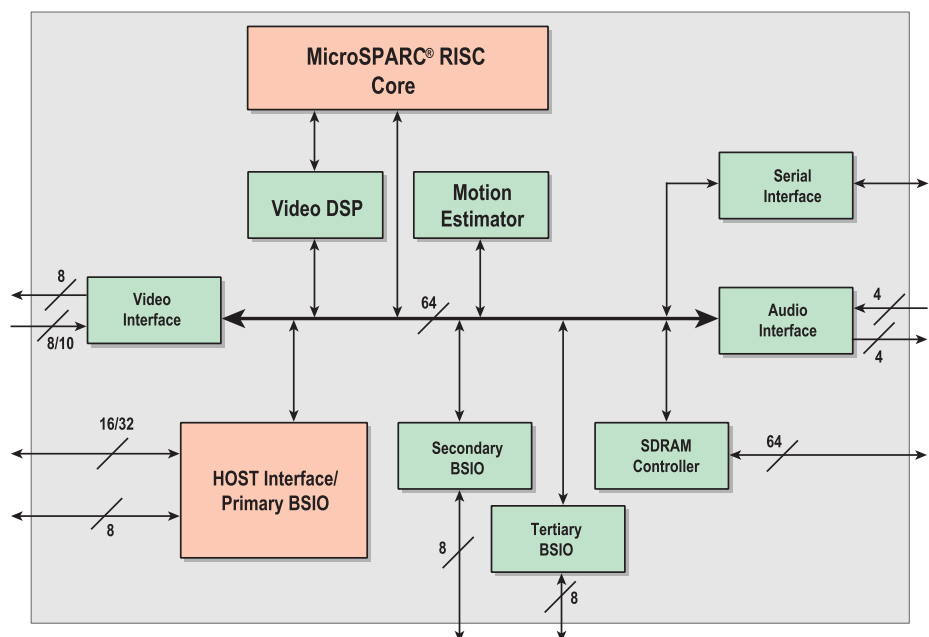
- Video compression pre-processing
- Motion estimation and compensation
- DCTs and IDCTs
- Variable-length encoding and decoding
- High-quality video scaling and compositing

TARGET APPLICATIONS

LSI Logic DVxcel offers significant design advantages for the following applications:

Digital Video Recorder (DVR)

LSI Logic DVxcel can be the core of a low-cost DVR application that has the ability to pause, fast-forward, rewind, and instant-replay live broadcast television. LSI Logic DVxcel simultaneously encodes and decodes video while also ensuring audio/video synchronization. Coupled with an embedded processor, LSI Logic DVxcel can enable a two-chip solution to provide a complete digital video time-shifting application.



LSI Logic DVxcel™ Internal Block Diagram




DVD/Optical Disc Recorder

Coupled with a DVD decoder (such as the LSI Logic ZiVA-4), LSI Logic DVxcel can provide the MPEG-2 video and system encoder portions of a DVD/optical disc recorder. LSI Logic DVxcel's on-chip MPEG-2 program stream multiplexing and DVD-VR RTRW format generation provides a clean and efficient system design for DVD/optical recorders, while the DVD decoder ensures compatibility with playback of existing content.

Personal TV Functions

LSI Logic DVxcel's programmable architecture can enable advanced personal TV features. While encoding video, vertical blanking interval (VBI) data can be captured and decoded by the codec to provide additional digital content information such as closed caption data and electronic programming guide data.



LSI Logic DVxcel™ MPEG-2 Video Codec

Video	Standards	NTSC, PAL, ITU-R BT.656
	Input Dithering	10-bit
	Output	Single-stream at 27 MHz
MPEG-2	Resolutions	Horizontal: 720, 704, 544, 480, 352 Vertical: 480 (NTSC), 576 (PAL)
	Encoding	ML@MP, VBR and CBR
	GOP Structure	I, IP, or IBP
	Bit Rate	1.8 to 10 Mbps
	System	Program Stream multiplexing of video Elementary Stream with audio Elementary Stream (DVD-VR compliant)
Audio	Ports	Four stereo input, four stereo output
	Interface	Serial interface to IDS devices
	Format	16-, 24-, or 32-bit at 32, 44.1, or 48 kHz
System	Host Interface	Flexible host interface with I-Mode, M-Mode, Wait, and DTACK
	Access Transfer	16-bit or 32-bit PIO 16-bit or 32-bit target DMA Three, 8-bit hardware-controlled bitstream ports
Memory	Configuration	8 Mbytes of external SDRAM
	Controller	On-chip, 64-bit-wide SDRAM interface
	Peak Bandwidth	880 Mbyte/s
Physical	Input Voltages	3.3 V I/O, 2.0 V Core
	System Clock	110 MHz
	Packaging	308-pin Ball Grid Array
	Operating Power	< 1.8 W @ VDDQ = 2.0 V typical
JTAG	Compliance	IEEE 1149.1 compliance for boundary scan testing

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