STANDARD
MICROSYSTEMS
CORPORATION

LPC47M120

PRELIMINARY

Legacy Reduced Super I/O with USB Hub

FEATURES

- 3.3 Volt Operation, 5 volt Tolerant
- LPC Interface
  - Multiplexed Command, Address and Data Bus
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
- PC98, PC99 Compliant
- General Purpose Input/Output
  - 16 Dedicated GPIO Pins
- System Management Interrupt
- Legacy Keyboard/Mouse Host Interface
  - Fast Gate A20 and KRESET Outputs (Port 92H)
  - Implements OHCI Legacy Support Registers
  - Generates SMI for External Keyboard/Mouse Controller Emulation
- Serial Port
  - High Speed NS16C550 Compatible UART with Send/Receive 16-Byte FIFO
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Two Floppy Drive Support
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to Eight IRQ and Seven DMA Options
  - Enhanced Digital Data Separator
- USB Hub
  - 1 Upstream, 4 Downstream Ports
  - Compliant with USB Spec. Version 1.1
  - Programmable USB Manufacturer ID, Product ID, Device Rev. Number
  - Number of active down stream Ports programmable via BIOS or selectable with external jumpers
  - Powered Separately for Downstream Port Wakeup
- Interrupt Generating Registers
  - Registers Generate IRQ1 – 15 on Serial IRQ Interface
- Mechanical Package
  - 100 Pin QFP

GENERAL DESCRIPTION

The LPC47M120 is a reduced function LPC I/O Controller for legacy free designs, with legacy support for the keyboard interface.

The LPC47M120 implements the LPC interface, a pin reduced ISA bus interface which provided the same or better performance as the ISA/X-bus with a substantial savings in pins used. The LPC47M120 provides an on chip UART compatible with the NS16C550A, 16 GPIO pins, a Legacy Keyboard Interface, a USB Hub and SMSC's true CMOS 765B Floppy Disk Controller.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use.

Legacy support for the keyboard/mouse interface is provided by implementation of OHCI Legacy Support Registers (as described in the Open Host Controller Interface Specification for USB, release 1.0a, Appendix B) along with legacy registers 60h and 64h. When enabled, I/O reads and writes to registers 60H and 64H are trapped, generating an SMI which enables external SMM code to emulate the keyboard and mouse services.

On board Interrupt Generating Registers enable external software to generate IRQ1 through IRQ15 on the Serial IRQ interface.

The USB Hub is a standalone block, implementing one upstream port and up to four downstream ports. An internal data path connection allows BIOS programming of the USB Vendor ID, Product ID, Device Revision Number. The number of active down stream ports is selectable with external jumpers or programmable via BIOS access to the hub control registers.

ORDERING INFORMATION

Order Number: LPC47M120-MC

100 Pin QFP Package

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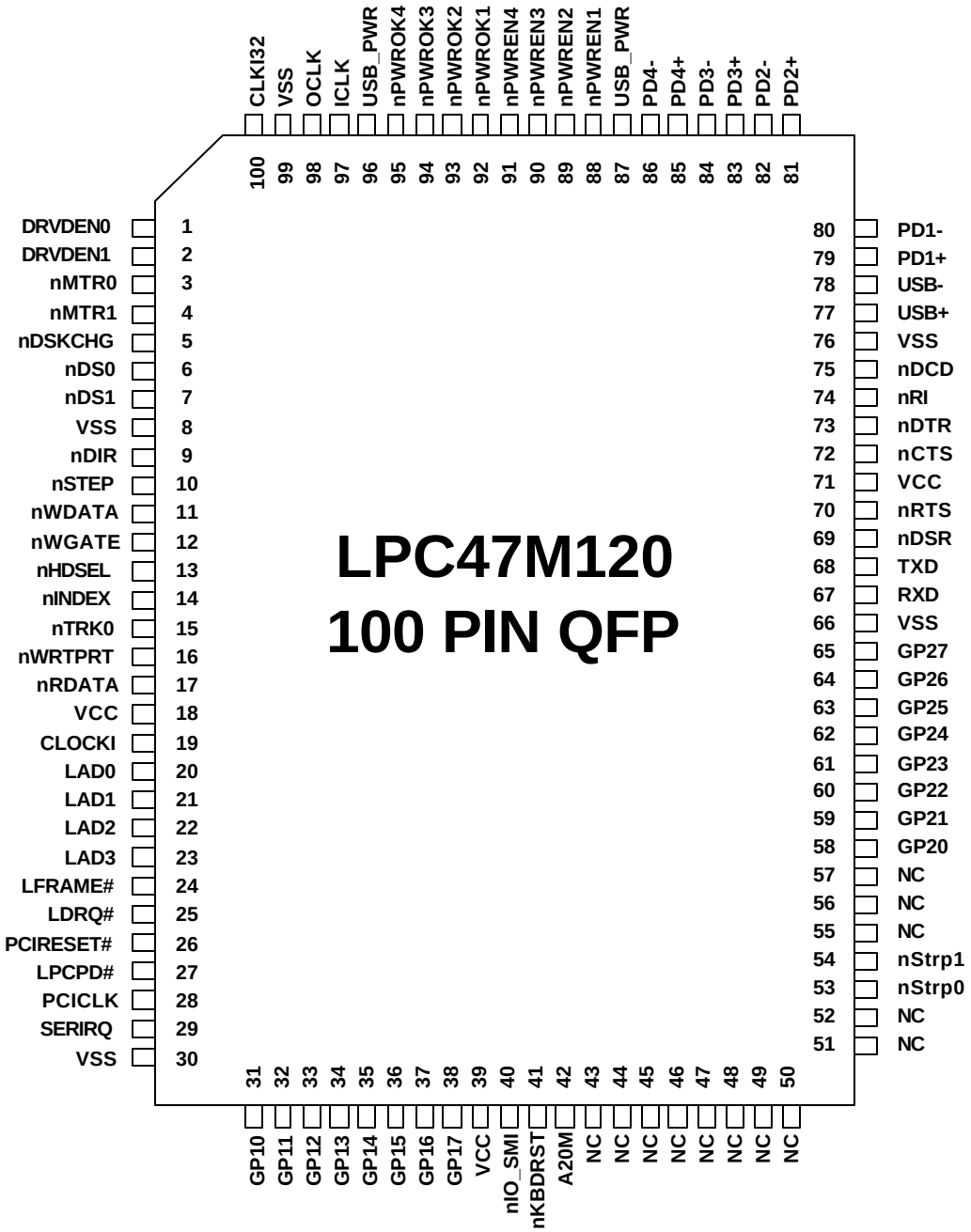
PIN LAYOUT

Pin Layout for Standard QFP Package



PIN CONFIGURATION

Table 1 - Pin Configuration for Standard QFP Package

PIN #	NAME	PIN #	NAME	PIN #	NAME	PIN #	NAME
1	DRVDEN0	**26**	PCIRESET#	**51**	NC	**76**	**VSS**
2	DRVDEN1	**27**	LPCPD#	**52**	NC	**77**	USB+
3	nMTR0	**28**	PCICLK	**53**	nStrp0	**78**	USB-
4	nMTR1	**29**	SERIRQ	**54**	nStrp1	**79**	PD1+
5	nDSKCHG	**30**	**VSS**	**55**	NC	**80**	PD1-
6	nDS0	**31**	GP10	**56**	NC	**81**	PD2+
7	nDS1	**32**	GP11	**57**	NC	**82**	PD2-
8	**VSS**	**33**	GP12	**58**	GP20	**83**	PD3+
9	nDIR	**34**	GP13	**59**	GP21	**84**	PD3-
10	nSTEP	**35**	GP14	**60**	GP22	**85**	PD4+
11	nWDATA	**36**	GP15	**61**	GP23	**86**	PD4-
12	nWGATE	**37**	GP16	**62**	GP24	**87**	**USB_PWR**
13	nHDSEL	**38**	GP17	**63**	GP25	**88**	nPWREN1
14	nINDEX	**39**	**VCC**	**64**	GP26	**89**	nPWREN2
15	nTRK0	**40**	nIO_SMI	**65**	GP27	**90**	nPWREN3
16	nWRTPRT	**41**	nKBDRST	**66**	**VSS**	**91**	nPWREN4
17	nRDATA	**42**	A20M	**67**	RXD	**92**	nPWROK1
18	**VCC**	**43**	NC	**68**	TXD	**93**	nPWROK2
19	CLOCKI	**44**	NC	**69**	nDSR	**94**	nPWROK3
20	LAD0	**45**	NC	**70**	nRTS	**95**	nPWROK4
21	LAD1	**46**	NC	**71**	**VCC**	**96**	**USB_PWR**
22	LAD2	**47**	NC	**72**	nCTS	**97**	ICLK
23	LAD3	**48**	NC	**73**	nDTR	**98**	OCLK
24	LFRAME#	**49**	NC	**74**	nRI	**99**	**VSS**
25	LDRQ#	**50**	NC	**75**	nDCD	**100**	CLKI32

Note: The number of active downstream ports is selectable via jumpers on strapping options nStrp0 and nStrp1 or programmable via BIOS. See section USB DOWNSTREAM PORT SELECTION located on page 73.

Note: No Connect (NC) pins 43 through 57 should be left unconnected, except pins 53 and 54 if USB downstream port selection is used.

DESCRIPTION OF PIN FUNCTIONS

PIN No./ QFP	SYMBOL	NAME	Power Plane	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)	NOTE
PROCESSOR/HOST LPC INTERFACE (11 pins)						
20,21, 22,23	LAD[3:0]	Multiplexed Command, Address, Data [3:0]	VCC	PCI_IO	PCI_IO	
24	LFRAME#	Frame	VCC	PCI_I	PCI_I	
25	LDRQ#	Encoded DMA Request	VCC	PCI_O	PCI_O	
26	PCI_RESET#	PCI Reset	VCC	PCI_I	PCI_I	
27	LPCPD#	Power Down	VCC	PCI_I	PCI_I	Note 3
28	PCI_CLK	PCI Clock	VCC	PCI_ICLK	PCI_ICLK	
29	SER_IRQ	Serial IRQ	VCC	PCI_IO	PCI_IO	
40	nIO_SMI	SMI Output	VCC	IO12	OD12	
CLOCKS (4 pins)						
19	CLOCKI	14.318MHz Clock Input	VCC	IS	IS	
97	ICLK	24 MHz Crystal/48 MHz Clock Input	VCC	IS	IS	Note 4
98	OCLK	24 MHz Crystal Input	VCC	IS	IS	
100	CLKI32	32.768 Trickle Clock Input	USB_PWR	IS	IS	Note 5
POWER PINS (10 pins)						
18,39, 71	VCC	Power				Note 6
87, 96	USB_PWR	USB Power				Note 6
8,30, 66,76, 99	VSS	Ground				
SERIAL PORT INTERFACE (8 pins)						
67	RXD	Receive Serial Data	VCC	IS	IS	
68	TXD	Transmit Serial Data	VCC	O12	O12	
69	nDSR	Data Set Ready	VCC	I	I	
70	nRTS	Request to Send	VCC	O8	O8	
72	nCTS	Clear to Send	VCC	I	I	
73	nDTR	Data Terminal Ready	VCC	O6	O6	
74	nRI	Ring Indicator	VCC	I	I	
75	nDCD	Data Carrier Detect	VCC	I	I	
KEYBOARD/MOUSE INTERFACE (2 pins)						
41	nKBDRST	Keyboard Reset	VCC	IO8	O8	
42	A20M	Gate A20	VCC	IO8	O8	
FDD INTERFACE (16 pins)						
1	DRVDEN0	Drive Density Select 0	VCC	IO12	(O12/OD12)	
2	DRVDEN1	Drive Density Select 1	VCC	IO12	(O12/OD12)	
3	nMTR0	Motor On 0	VCC	O12	(O12/OD12)	
4	nMTR1	Motor On 1	VCC	O12	(O12/OD12)	
5	nDSKCHG	Disk Change	VCC	IS	IS	
6	nDS0	Drive Select 0	VCC	O12	(O12/OD12)	

DESCRIPTION OF PIN FUNCTIONS

PIN No./ QFP	SYMBOL	NAME	Power Plane	BUFFER TYPE	BUFFER TYPE PER FUNCTION (NOTE 1)	NOTE
7	nDS1	Drive Select 1	VCC	O12	(O12/OD12)	
9	nDIR	Step Direction	VCC	O12	(O12/OD12)	
10	nSTEP	Step Pulse	VCC	O12	(O12/OD12)	
11	nWDATA	Write Disk Data	VCC	O12	(O12/OD12)	
12	nWGATE	Write Gate	VCC	O12	(O12/OD12)	
13	nHDSEL	Head Select	VCC	O12	(O12/OD12)	
14	nINDEX	Index Pulse Input	VCC	IS	IS	
15	nTRKO	Track 0	VCC	IS	IS	
16	nWRTPRT	Write Protected	VCC	IS	IS	
17	nRDATA	Read Disk Data	VCC	IS	IS	
USB HUB (18 pins)						
53, 54	nStrp0, nStrp1	nStrp0, nStrp1	Note 8	IPU	IPU	
77	USB+	Upstream Port Data +	USB_PWR	IOUSB	IOUSB	
78	USB-	Upstream Port Data -	USB_PWR	IOUSB	IOUSB	
85,83, 81,79	PD+[4:1]	Downstream Port Data +	USB_PWR	IOUSB	IOUSB	
86,84, 82,80	PD- [4:1]	Downstream Port Data -	USB_PWR	IOUSB	IOUSB	
91,90, 89,88	nPWREN[4:1]	Downstream Port Power Enable	USB_PWR	O24	O24	Note 7
95,94, 93,92	nPWROK[4:1]	Downstream Port Over Current Sense	USB_PWR	IPU	IPU	Note 7
GENERAL PURPOSE I/O (16 pins)						
31	GP10	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
32	GP11	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
33	GP12	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
34	GP13	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
35	GP14	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
36	GP15	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
37	GP16	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
38	GP17	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
58	GP20	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
59	GP21	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
60	GP22	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
61	GP23	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
62	GP24/ SYSOPT	General Purpose I/O/ System Option	VCC	IO8	(I/O8/OD8)	Note 2
63	GP25	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
64	GP26	General Purpose I/O	VCC	IO8	(I/O8/OD8)	
65	GP27	General Purpose I/O	VCC	IO8	(I/O8/OD8)	

Note 0: The "n" as the first letter of a signal name or the "#" as the suffix of a signal name indicates an "Active Low" signal.

Note 1: Buffer types per function on multiplexed pins are separated by a slash "/". Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 2: The GP24 / SYSOPT pin requires an external pulldown resistor to put the base IO address for configuration at 0x02E. An external pullup resistor is required to move the base IO address for configuration to 0x04E.

Note 3: The LPCPD# pin may be tied high. The LPC interface will function properly if the PCI_RESET# signal follows the protocol defined for the LRESET# signal in the "Low Pin Count Interface Specification."

Note 4: The 48MHz. clock input must not be driven high when USB_PWR = 0v.

Note 5: CLKI32 is used for timing port change events in the USB Hub. The CLKI32 input must not be driven high when USB_PWR = 0v.

Note 6: USB_PWR must be applied before, or at the same time as, VCC. When VCC is removed, USB_PWR must be at its full minimum potential at least 10 us before VCC begins a power-on cycle. When VCC and USB_PWR are fully powered, the potential difference between the two supplies must not exceed 500 mV.

Note 7: When the specified USB Down Stream Ports are disabled via the Strp0/Strp1 bit or nStrp1/nStrp0 Pins, the associated Power OK sense pins (nPWROK[x]) and Power Enable (nPWREN[4:1]) pins are also disabled. The USB Down Stream Port nPWROK[x] input pin can be a NC (No Connect) pin for existing designs or tied High (1). For EMI and reduced Noise sensitivity, it is recommended that the pin be tied High (1). The Power Enable (nPWREN[x]) pin will be forced low (0).

Note 8: nStrp1/nStrp0 Pins are latched on the de-asserting edge of USB_PWR power-on-reset.

Buffer Type Descriptions

Note: The buffer type values are specified at VCC=3.3V

IO12	Input/Output, 12mA sink, 6mA source.
IS/O12	Input with Schmitt Trigger/Output, 12mA sink, 6mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8 mA sink.
O24	Output, 24mA sink, 12mA source.
IO8	Input/Output, 8mA sink, 4mA source.
I	Input TTL Compatible.
IPU	Input TTL Compatible. With 30ua internal Pull Up
IS	Input with Schmitt Trigger.
IOUSB	USB Differential Data Lines (per USB specification; V1.1)
PCI_IO	Input/Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_O	Output. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_I	Input. These pins must meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_ICLK	Clock Input. These pins must meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2)

Note 1: See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.
Note 2: See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

Pins That Require External Pullup Resistors

The following pins require external pullup resistors:

- SERIRQ
- nWDATA if used as Open Collector Output.
- nWGATE if used as Open Collector Output.
- nHDSEL if used as Open Collector Output.
- nDIR if used as Open Collector Output.
- nSTEP if used as Open Collector Output.
- nDS0 if used as Open Collector Output.
- nDS1 if used as Open Collector Output.
- nMTRO if used as Open Collector Output.
- nMTR1 if used as Open Collector Output.
- DRVDEN0 if used as Open Collector Output.
- DRVDEN1 if used as Open Collector Output.
- GP10 if used as Open Collector Output.
- GP11 if used as Open Collector Output.
- GP12 if used as Open Collector Output.
- GP13 if used as Open Collector Output.
- GP14 if used as Open Collector Output.
- GP15 if used as Open Collector Output.
- GP16 if used as Open Collector Output.
- GP17 if used as Open Collector Output.
- GP20 if used as Open Collector Output.
- GP21 if used as Open Collector Output.
- GP22 if used as Open Collector Output.
- GP23 if used as Open Collector Output.
- GP24 if used as Open Collector Output.
- GP25 if used as Open Collector Output.
- GP26 if used as Open Collector Output.
- GP27 if used as Open Collector Output.

BLOCK DIAGRAM

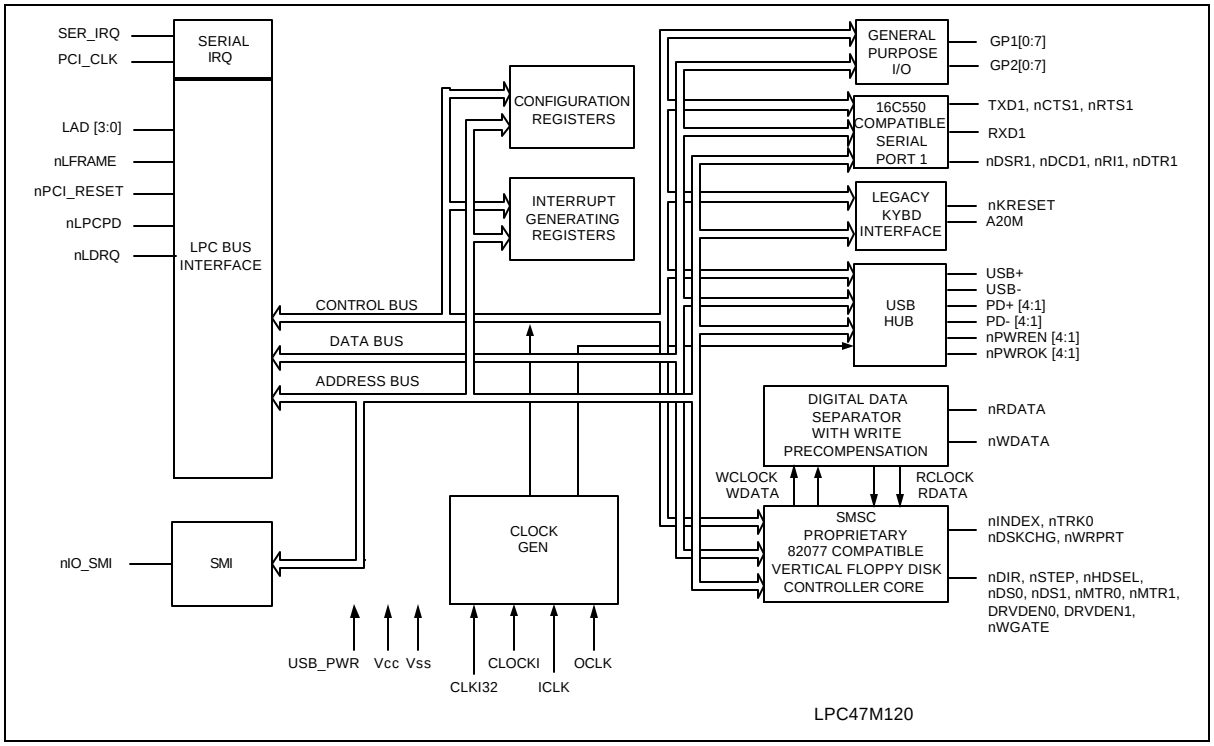


FIGURE 1 - LPC47M120 BLOCK DIAGRAM

3 VOLT OPERATION / 5 VOLT TOLERANCE

The LPC47M120 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- LFRAME#
- LDRQ#
- LPCPD#

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- PCI_RESET#
- PCI_CLK
- SER_IRQ

POWER FUNCTIONALITY

The LPC47M120 has two (2) power planes: VCC and USB_PWR.

VCC Power

The LPC47M120 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

USB Power

The LPC47M120 requires a supply (USB_PWR) to provide current for USB Hub wake-up events when V_{CC} is removed. The USB_PWR supply is 3.3 Volts (nominal). See the Operational Description Section for maximum USB_PWR current that is required. USB_PWR powers the USB Hub, 24MHz OSC/PLL, 32KHz clock input buffer, 48MHz CLK/OSC Mux and all Logical Device and Global Configuration Registers. The USB_PWR pin generates a USB_PWR Power-on-Reset signal to initialize these components. The 48MHz (ICLK) clock input and 32Khz (CLKI32) clock input must not be driven high when USB_PWR equals 0 volts.

Note: When V_{CC} is removed, USB_PWR must be at its full minimum potential at least 10 µs before Vcc begins a power-on cycle. When USB_PWR and Vcc are fully powered, the potential difference between the two supplies must not exceed 500mV.

Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as Vcc cycles on and off. When the internal PWRGOOD signal is “1” (active), Vcc > 2.3V (nominal), and the LPC47M120 host interface is active. When the internal PWRGOOD signal is “0” (inactive), Vcc ≤ 2.3V (nominal), and the LPC47M120 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

32.768 kHz Trickle Clock Input

The LPC47M10x utilizes a 32.768 kHz trickle input to supply a clock signal for the USB Hub logic. This clock is required for USB Hub wakeup events when Vcc and 48 MHz are removed.

Maximum Current Values

See the “Operational Description” section for the maximum current values.

The maximum USB_PWR current, I_{USB}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded) , and all inputs in a fixed state (i.e., 0V or 3.3V).

FUNCTIONAL DESCRIPTION

Super I/O Registers

The address map, shown below in Table 2 - Super I/O Block Addresses , shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial port and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

Host Processor Interface (LPC)

The host processor communicates with the LPC47M120 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 2 - Super I/O Block Addresses . Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Table 2 - Super I/O Block Addresses

ADDRESS	BLOCK NAME	LOGICAL DEVICE	NOTES
Base+(0-5) and +(7)	Floppy Disk	0	
Base+(0-7)	Serial Port Com 1	4	
60, 64	Legacy KYBD	7	
Base + (0-5F)	Runtime Registers	A	
Base + (0-1)	Configuration		

Note 1: Refer to the configuration register descriptions for setting the base address.

LPC Interface

The following sub-sections specify the implementation of the LPC bus.

LPC Interface Signal Definition

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset. Same functionality as RST_DRV but active low 3.3V.
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.
LPCPD#	Input	Powerdown Signal. Indicates that the LPC47M10x should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.

Note: The CLKRUN# signal is not implemented in this part.

LPC Cycles

The following cycle types are supported by the LPC protocol.

CYCLE TYPE	TRANSFER SIZE
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 byte
DMA Read	1 byte

Peripherals must ignore cycles that they do not support.

FIELD DEFINITIONS

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the LPC47M120. See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2 for definition of these fields.

LFRAME# USAGE

LFRAME# is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the LPC47M120 to know when to monitor the bus for a cycle. This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the LPC47M120 monitors the bus to determine whether the cycle is intended for it. The use of LFRAME# allows the LPC47M120 to enter a lower power state internally. There is no need for the LPC47M120 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the LPC47M120 samples LFRAME# active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The LFRAME# signal functions as described in the Low Pin Count (LPC) Interface Specification, Revision 1.0.

I/O READ AND WRITE CYCLES

The LPC47M120 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

DMA READ AND WRITE CYCLES

DMA read cycles involve the transfer of data from the host (main memory) to the LPC47M120. DMA write cycles involve the transfer of data from the LPC47M120 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the LPC47M120 are 1, 2 or 4 bytes.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

DMA PROTOCOL

DMA on the LPC bus is handled through the use of the LDRQ# lines from the LPC47M120 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Interface Specification, Revision 1.0.

Power Management

CLOCKRUN PROTOCOL

The CLKRUN# pin is not implemented in the LPC47M120.
See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.1.

LPCPD Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

SYNC Protocol
See the *Low Pin Count (LPC) Interface Specification* Reference Section 4.2.1.8 for a table of valid SYNC values.

TYPICAL USAGE

The SYNC pattern is used to add wait states. For read cycles, the LPC47M120 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47M120 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The LPC47M120 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.
The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The LPC47M120 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the LPC47M120 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

SYNC TIMEOUT

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The LPC47M120 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

SYNC PATTERNS AND MAXIMUM NUMBER OF SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47M120 has protection mechanisms to complete the cycle. This is used for EPP data transfers and should utilize the same timeout protection that is in EPP.

SYNC ERROR INDICATION

The LPC47M120 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the LPC47M120, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the LPC47M120. If the host was writing data to the LPC47M120, the data had already been transferred.

In the case of multiple byte cycles, such as memory and DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

I/O and DMA START Fields

I/O and DMA cycles use a START field of 0000.

Reset Policy

The following rules govern the reset policy:

1) When PCI_RESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2) When PCI_RESET# goes active (low):

a) the host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.
b) the LPC47M120 must ignore LFRAME#, tristate the LAD[3:0] pins and drive the LDRQ# signal inactive (high).

LPC TRANSFER SEQUENCE EXAMPLES

Wait State Requirements

I/O Transfers
The LPC47M120 inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY has been deasserted (i.e., EPP or IrCC transfers) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

DMA Transfers
The LPC47M120 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

See the example timing for the LPC cycles in the “Timing Diagrams” section.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

FDC Internal Registers

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 3 - Status, Data and Control Registers shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 3 - Status, Data and Control Registers

(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TSR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

STATUS REGISTER A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION

Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX

Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt.

STATUS REGISTER B (SRB)

Address 3F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins in PS/2 and Model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE
Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3
The DS3 disk interface is not supported.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input. Note: This function is not supported.

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode:
Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

DRIVE	DOR VALUE
0	1CH
1	2DH

BIT 6 MOTOR ENABLE 2
The MTR2 disk interface output is not supported in the LPC47M120.

BIT 7 MOTOR ENABLE 3
The MTR3 disk interface output is not supported in the LPC47M120.

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 4 - Tape Select Bits illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 4 - Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 2 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	1	0	nBIT 5	nBIT 4
X	X	1	X	0	1	0	1	nBIT 5	nBIT 4
X	1	X	X	1	0	1	1	nBIT 5	nBIT 4
1	X	X	X	1	1	1	1	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	nBIT 5	nBIT 4

Table 6 - Internal 2 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	nBIT 4	nBIT 5
X	X	1	X	0	1	1	0	nBIT 4	nBIT 5
X	1	X	X	1	0	1	1	nBIT 4	nBIT 5
1	X	X	X	1	1	1	1	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	nBIT 4	nBIT 5

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are '0'.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 7 - Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 - B1	L0-CRF2 - B0
0	1	L0-CRF2 - B3	L0-CRF2 - B2
1	0	L0-CRF2 - B5	L0-CRF2 - B4
1	1	L0-CRF2 - B7	L0-CRF2 - B6

Note: L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY
This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30.

Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 9 - Data Rates for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 8 - Precompensation Delays shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

Table 8 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default
	Default: See Table 11 - Default Precompensation Delays	

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located at the offset 0x1F in the runtime register block. Separator circuits will be turned off. The controller will come out of manual low power.

Table 9 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRVDEN pins.

Table 10 - DRVDEN Mapping

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 11 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

MAIN STATUS REGISTER

Address 3F4 READ ONLY
The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 - 1 DRV x BUSY
These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY
This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA
This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO
Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM
Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE
All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 12 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \# } x \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s\ \text{DELAY} =$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 12 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 are read as ‘0’.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 9 - Data Rates for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 9 - Data Rates for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC
This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (see Runtime Register at offset 0x1E).

CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY
PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 9 - Data Rates for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0"

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
						NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 9 - Data Rates for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0"

Table 10 - DRVDEN Mapping shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 13 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 14 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writeable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 15 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 16 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the PCI_RESET# pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a PCI_RESET#, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

PCI_RESET# Pin (Hardware Reset)

The PCI_RESET# pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION
The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits in LD0-CRF0[3,2].

PC/AT mode
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

PS/2 mode
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care". The DMA and interrupt functions are always enabled, and DENSEL is active low.

Model 30 mode
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

DMA TRANSFERS
DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: Single Transfer and Burst Transfer. Burst mode is enabled via Logical Device 0-CRF0-Bit[1] (LD0-CRF0[1]).

CONTROLLER PHASES
For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase
After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 17 - Description of Command Symbols for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase
All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host.

The interrupt and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The interrupt can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the interrupt and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The interrupt and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The interrupt and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode - Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller must respond by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 17 - Description of Command Symbols for explanations of the various symbols used. Table 18 - Instruction Set lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 17 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.

SYMBOL	NAME	DESCRIPTION
DS0, DS1	Disk Drive Select	DS1 DS0 DRIVE 0 0 Drive 0 0 1 Drive 1
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. N SECTOR SIZE 128 Bytes 256 Bytes 512 Bytes 1024 Bytes … … 07 16K Bytes

SYMBOL	NAME	DESCRIPTION
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

Instruction Set

Table 18 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Com mand execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Com mand execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Com mand execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Com mand execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution for Each Sector Repeat:	W	C								Input Sector Parameters
	W	H								
	W	R								
	W	N								
										FDC formats an entire cylinder
Result	R	ST0								Status information after Command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each seek operation.
	R	PCN								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	FIFOTHR				
Execution	W	PRETRK								

RELATIVE SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT						HUT		
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3		D2	D1	D0	GAP	WGATE
	R	0	EIS	EFIFO		POLL	FIFOTHR			
	R	PRETRK								

READ ID										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution.
	R	ST1								Disk status after the Command has completed
	R	ST2								
	R	C								
	R	H								
	R	R								
	R	N								

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	Invalid Codes								Invalid Command Codes (NoOp - FDC goes into Stand-by State)
Result	R	ST0								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 19 - Sector Size below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 19 - Sector Size

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 20 - Effects of MT and N Bits.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 21 - Skip Bits vs Read Data Command describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 21 - Skip Bits vs Read Data Command, the C or R value of the sector address is automatically incremented (see Table 23 - Result Phase Table).

Table 20 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 21 - Skip Bits vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field. Table 22 - Skip Bits vs. Read Deleted Data Command describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 22 - Skip Bits vs. Read Deleted Data Command, the C or R value of the sector address is automatically incremented (see Table 23 - Result Phase Table).

Table 22 - Skip Bits vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a “1” if there no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the INDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 23 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

Write Data
After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data
This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify
The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 23 - Result Phase Table and Table 24 - Verify Command Result Phase Table for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 24 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 25 - Typical Values for Formatting contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x	12x			50x	12x								22x	12x						
4E	00	3x C2	FC	4E	00	3x A1	FE						4E	00	3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM	DATA	CRC	GAP3	GAP 4b
40x	6x		26x	6x							11x	6x					
FF	00	FC	FF	00	FE						FF	00	FB or F8				

PERPENDICULAR FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x	12x			50x	12x								41x	12x						
4E	00	3x C2	FC	4E	00	3x A1	FE						4E	00	3x A1	FB F8				

Table 25 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested GPL value in Format A Track command.

*PC/AT values (typical)

**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

Note: All values except sector size are in hex.

CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTRK0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek
The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status
An interrupt signal is generated by the FDC for one of the following reasons:

1) Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command

2) End of Seek, Relative Seek, or Recalibrate command

3) FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 26 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status
Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify
The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 27 - Drive Control Delays (ms). The values are the same for MFM and FM.

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signaled by the DMA request cycles. Non-DMA mode uses the RQM bit and the interrupt to signal data transfers.

Configure
The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 27 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version
The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek
The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

Perpendicular Mode
The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 28 - Effects of WGATE and GAP Bits describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned

on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on Page 58 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1) The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2) The write pre-compensation given to a perpendicular mode drive will be 0ns.
3) For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1) "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2) "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 28 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK
In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the PCI_RESET# pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG
The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

COMPATIBILITY
The LPC47M120 was designed with software compatibility in mind. It is a fully backwards- compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

SERIAL PORT (UART)

The LPC47M120 incorporates one full function UART, compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UART. The interrupt from the UART is enabled by programming OUT2 to a logic "1". OUT2 being a logic "0" disables the interrupt.

Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial port is defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The LPC47M120 register set is described below.

Table 29 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*__Note:__ DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)
Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the LPC47M120. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART FCR is shadowed in the UART FIFO Control Shadow Register (runtime register at offset 0x20).

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3
Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

Bit 4,5
Reserved

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 6,7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

INTERRUPT IDENTIFICATION REGISTER (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1) Receiver Line Status (highest priority)
2) Received Data Ready
3) Transmitter Holding Register Empty
4) MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Table 30 - Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by Table 30 - Interrupt Control Table.

Bit 3
In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

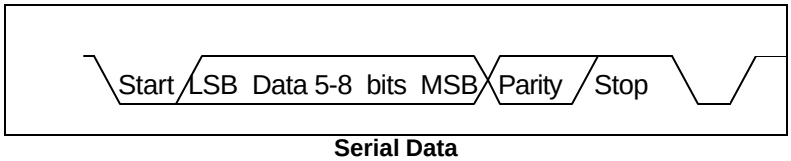
Bits 4 and 5
These bits of the IIR are always logic "0".

Bits 6 and 7
These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 30 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

LINE CONTROL REGISTER (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE



Serial Data

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as a 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0
This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1
This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable a UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1) The TXD is set to the Marking State(logic "1").
2) The receiver Serial Input (RXD) is disconnected.
3) The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4) All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5) The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6) The Modem Control output pins are forced inactive high.
7) Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier
Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)
Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)
The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a 2 is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 31 - Baud Rates , shows the baud rates possible.

Effect Of The Reset on Register File
Table 32 - Reset Function Table details the effect of the Reset input on each of the registers of the Serial Port.

FIFO INTERRUPT MODE OPERATION
When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.

D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
At least one character is in the FIFO.

The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay). The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION
With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.
Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
Bit 5 indicates when the XMIT FIFO is empty.
Bit 6 indicates that both the XMIT FIFO and shift register are empty.
Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 31 - Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note [2]: The High Speed bit is located in the Device Configuration Space.

Table 32 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 33 - Register Summary for UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 7)	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 34 - Register Summary for UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.
Note 7: The UART FCR's are shadowed in the UART FIFO Control Shadow Register (runtime register at offset 0x20).

NOTES ON SERIAL PORT OPERATION
FIFO MODE OPERATION:

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have the Tx FIFO empties after this condition, the Tx been loaded into the FIFO, concurrently. When interrupt will be activated without a one character delay.**

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

POWER MANAGEMENT

Power management capabilities are provided for the floppy disk and UART logical devices. For each logical device, two types of power management are provided: direct powerdown and auto powerdown.

FDC Power Management
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23-B0. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1) The motor enable pins of register 3F2H are inactive (zero).

2) The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).

3) The head unload timer must have expired.

4) The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

DSR From Powerdown
If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

Wake Up From Auto Powerdown
If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the PCI_RESET# pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1) Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2) A read from the MSR register.
3) A read or write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

Register Behavior
Table 35 - PC/AT and PS/2 Available Registers illustrates the AT and PS/2 (including Model 30) configuration registers available and the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 35 - PC/AT and PS/2 Available Registers shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

Pin Behavior
The LPC47M120 is specifically designed for systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the LPC47M120 can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

Table 35 - PC/AT and PS/2 Available Registers

BASE + ADDRESS	AVAILABLE REGISTERS		ACCESS PERMITTED
	PC-AT	PS/2 (MODEL 30)	
Access to these registers DOES NOT wake up the part			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (1)	DOR (1)	R/W
03H	---	---	---
04H	DSR (1)	DSR (1)	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the part			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part.

System Interface Pins
Table 36 - State of System Pins in Auto Powerdown gives the state of the interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged".

Table 36 - State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
LAD[3:0]	Unchanged
LDRQ#	Unchanged
LPCPD#	Unchanged
LFRAME#	Unchanged
PCI_RESET#	Unchanged
PCI_CLK	Unchanged
SER_IRQ	Unchanged

FDD Interface Pins
All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

Pins used for local logic control or part programming are unaffected. Table 37 - State of Floppy Disk Drive Interface Pins in Powerdown depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 37 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTPRT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Active
nSTEP	Active
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Active
DRVDEN[0:1]	Active

UART Power Management
Direct power management is controlled by CR22. Refer to CR22 for more information.

Auto Power Management is enabled by CR23 Bit 4. When set, these bits allow the following auto power management operations:

1) The transmitter enters auto powerdown when the transmit buffer and shift register are empty.

2) The receiver enters powerdown when the following conditions are all met:

   A. Receive FIFO is empty
   B. The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

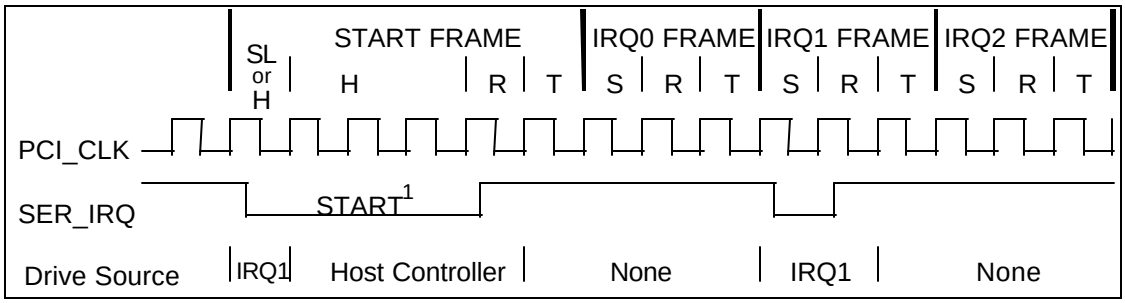
Exit Auto Powerdown
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

SERIAL IRQ

The LPC47M120 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0.

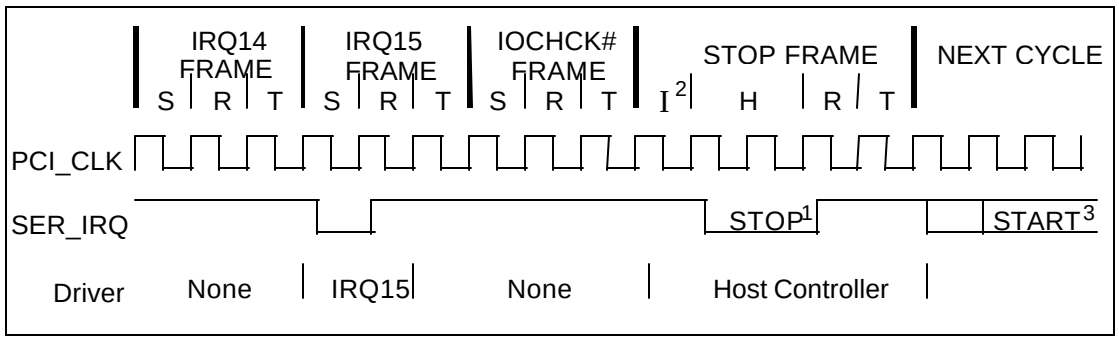
Timing Diagrams For SER_IRQ Cycle

A) Start Frame timing with source sampled a low pulse on IRQ1



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample
Note 1: Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

B) Stop Frame Timing with Host using 17 SER_IRQ sampling period



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle
Note 1: The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.
Note 2: There may be none, one or more Idle states during the Stop Frame.
Note 3: Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

SER_IRQ Cycle Control
There are two modes of operation for the SER_IRQ Start Frame.

1) **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The LPC47M120) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2) **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. **Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.**

SER_IRQ Data Frame

Once a Start Frame has been initiated, the LPC47M120 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the LPC47M120 must drive the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ must be left tri-stated. During the Recovery phase the LPC47M120 must drive the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the LPC47M120 must tri-state the SER_IRQ. The LPC47M120 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

SER_IRQ Sampling Periods

SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame will now support IRQ2 from a logical device, previously SER_IRQ Period 3 was reserved for use by the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices 0 (FDC), 4 (Ser Port 1), and 7 (KBD) shall have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the SMI pin via bit 7 of the SMI Enable Register 2.

Stop Cycle Control
Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

Latency
Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR Read Latency
Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

AC/DC Specification Issue
All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

Reset and Initialization
The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

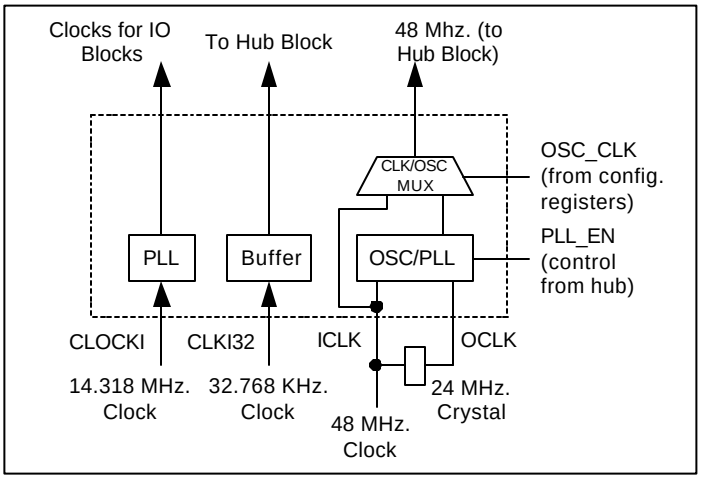
USB HUB FUNCTIONAL DESCRIPTION

The USB Hub Block implements one upstream port and up to four downstream ports. The internal address/data/ control connection is provided for programming by BIOS the USB Vendor ID, Product ID, Device Revision Number and number of down stream ports by accessing the Hub Control register. USB cable data is not transmitted or received via the internal connection.

The USB Hub Block implements the requirements defined in the USB Hub Device Class Specification Version 1.1 (USB Specification 1.1, Chapter 11), including Status Change Endpoint, Hub class specific descriptors and Hub class specific requests. The USB Hub Block supports Suspend and Resume both as a USB device and in terms of propagating Suspend and Resume signaling. It also supports remote wakeup by a device on downstream ports.

For efficient power management and wakeup requirements, the Hub Block is powered from separate power pins (USB_PWR). USB_PWR also powers the following: 24 Mhz. OSC/PLL, 32 KHz. Buffers, 48 Mhz. CLK/OSC Mux. and all Logical Device and Global Configuration Registers.

The Hub Block clock requirements are derived from separate CLK/OSC pins (ICLK, OCLK) and the CLKI32 pin. Clock pins ICLK and OCLK provide implementation flexibility for the system designer (see FIGURE 2 - LPC47M120 CLOCK GENERATOR). When a 48 Mhz. clock signal is available, it may be connected directly to the ICLK pin. To reduce overall system EMI, a local 24 Mhz. oscillator may alternately be connected between the ICLK and OCLK pins. Control bit OSC_CLK in the Logical Device A Configuration Registers at 0xF0, selects between clock sources. The 32 KHz. clock source is used to time certain port change events. This will ensure the USB Hub will respond to port change events while the hub is in Suspend.



For power conservation the USB Hub Block turns off internal hub clocks during Suspend, as follows:

The Hub Block responds to two types of Suspend. Selective (or Port) Suspend and Global Suspend. Segments of the bus can be selectively suspended by sending the command SetPortFeature (PORT_SUSPEND) to the hub port to which that segment is attached. The suspended port will block activity to the suspended bus segment. Because other ports on the hub remain active, internal clocks are not turned off.

Global Suspend is used when no communication is desired anywhere on the bus and the entire bus is placed in the Suspend state. The host signals the start of global suspend by ceasing all its transmissions (including the SOF token). As the hub block, and each device on the bus, recognizes that the bus is in the idle state for the appropriate length of time, it goes into the Suspend state. Because all bus segments attached to the hub are in the Suspend state, the hub will turn off the internal 24 Mhz. driven PLL. In addition, 48 Mhz. is stopped in the Hub Block. The 48 Mhz. clock signal at the ICLK pin, if enabled, is not stopped. Control logic external to the LPC47M120 should stop this clock, if desired.

The Hub Block will Resume from a Suspend state by receiving any non-idle signaling by a remote wakeup enabled device on its downstream ports or Resume signaling on its upstream port. If the Hub has been enabled as a remote wakeup source, it will also Resume from connects or disconnects on downstream ports. The internal 24 Mhz. driven PLL (and the 48 Mhz. in the Hub Block) will be started to complete the Resume.

USB DOWNSTREAM PORT SELECTION

The LPC47M120 USB Hub has the ability to program, via BIOS control register access or through external PIN strapping options, the number of Down Stream Ports that are available to the User. There is also a “Pin Strapping” option that will allow the board designer the ability to define the number of down stream ports that will be active via during USB_PWR POR.

The LPC47M120 USB Hub block will make the following changes to its external signals and device class response parameters:

1) All related input and output signals such as the associated Power OK sense pins (nPWROK[x]) and Power Enable (nPWREN[x]) pin are also disabled.
2) The USB Down Stream Port nPWROK[x] input pin can be a NC (No Connect) pin or tied High (1). For EMI and reduced Noise sensitivity, it is recommended that the pin be tied High (1).
3) The Power Enable (nPWREN[x]) pin will be forced low (0). For EMI and reduced Noise sensitivity, it is recommended that the pin be tied High (1).
4) The associated PDx+ and PDx- pins will not be active can be a NC (No Connect) pin. For EMI and reduced Noise sensitivity, it is recommended that the pin be tied High (1).
5) All Hub Device Class return descriptors must respond with the appropriate information relating to the number of ports that are currently selected by the Strap Pins or control bits in the register described in “Table 54 - Runtime Registers, Logical Device A

NAME	**REG INDEX**	**DEFINITION**	**NOTES**
OSC_CLK Default = 0x00 on USB_PWR POR	0xF0 R/W	Bit [0] Reserved Bit [1] OSC_CLK 0=48MHz clock is connected to the ICLK pin (default) 1=24MHz crystal is connected to the ICLK and OCLK pins Bits [7:2] Reserved	
IdVendor_Low Default=0x24 on USB_PWR POR	0xF1 R/W	Bit[7:0] USB Vendor ID (assigned by USB), low byte Default reset to SMSC ID	System Note1
IdVendor_High Default=0x04 on USB_PWR POR	0xF2 R/W	Bit[7:0] USB Vendor ID (assigned by USB), high byte Default reset to SMSC ID	System Note1
IdProduct_Low Default=0x20 on USB_PWR POR	0xF3 R/W	Bit[7:0] USB Product ID (assigned by manufacturer), low byte Default reset to SMSC silicon ID	System Note1
IdProduct_High Default=0x01 on USB_PWR POR	0xF4 R/W	Bit[7:0] USB Product ID (assigned by manufacturer), high byte Default reset to SMSC silicon ID	System Note1
BcdDevice_Low Default=0x00 on USB_PWR POR	0xF5 R/W	Bit[7:0] USB Device Release Number (in binary coded decimal), low byte Default set to SMSC silicon revision	System Note1
BcdDevice_High Default=0x00 on USB_PWR POR	0xF6 R/W	Bit[7:0] USB Device Release Number (in binary coded decimal), high byte Default set to SMSC silicon revision	System Note1
HubControl_1 Default=0x00 on USB_PWR POR	0xF7 R/W	Bit[0] GangedPWR Bit[1:6] Reserved Bit[7] NHubReset	
INT_G Default = 0x00 on VCC POR, USB_PWR POR, HARD RESET and SOFT RESET	0xF8 R/W	Bit[7:1] Reserved Bit[0] INT_G Enable 0=Disable Interrupt Generating Registers 1=Enable Interrupt Generating Registers When Bit 0 is set to “0” INT_GEN1 and INT_GEN2 registers (Runtime Registers at runtime block offset 59 and 5A) are prevented from outputting to the SER IRQ stream.	

NAME	REG INDEX	DEFINITION	NOTES
	0xFA- 0xFF	Reserved – read as '0'	

6) Table 55 - HubControl_1 Register Definition" on page 107, below. The information shown in "Table 38 - Hub Descriptor to be Modified" shown on page 74, below, describes what fields now need to be programmed bas on the number of enabled ports.

Table 38 - Hub Descriptor to be Modified

OFFSET	FIELD	PROGRAMMABLE	SIZE	DESCRIPTION
0	bDescLength		1	Number of bytes in this descriptor, including this byte.
1	bDescriptorType		1	Descriptor Type
2	bNbrPorts	X	1	Number of downstream ports that this hub supports. Selected by the "Strp0 and nStrp1" input pins or the HubControl_1 register defined in **Error! Not a valid result for table.**, shown on page 107, below.
3	Whub Characteristics		2	D1..D0: Power Switching Mode 00 – Ganged power switching (all ports' power at once) 01 – Individual port power switching 1X – No power switching (ports always powered on when hub is on and off when hub is off). D2: Identifies a Compound Device 0 – Hub is not part of a compound device 1 - Hub is part of a compound device D4..D3: Over-current Protection Mode 00 - Global Over-current Protection. The hub reports over-current as a summation of all ports' current draw, without a breakdown of individual port over-current status. 01 - Individual Port Over-current protection. The hub reports over-current on a per-port basis. Each port has an over-current indicator. 1X -No Over-Current Protection. This option is only allowed for bus-powered hubs that do not implement over-current protection. D15..D5: Reserved
5	BPwrOn2PwrGood		1	Time (in 2 ms intervals) from the time power on sequence begins on a port until power is good on that port. System software uses this value to determine how long to wait before accessing a powered-on port.
6	bHubContrCurrent		1	Maximum current requirements of the hub controller electronics in mA.
7	DeviceRemovable	X	Variable depend-ing on number of ports on hub	Indicates if a port has a removable device attached. If a non-removable device is attached to a port, that port will never receive an insertion change notification. This field is reported on byte-granularity. Within a byte, if no port exists for a given location, the field representing the port characteristics returns

OFFSET	FIELD	PROGRAMMABLE	SIZE	DESCRIPTION
				"0". Bit definition: 0 - Device is removable 1 - Device is not removable (permanently attached) This is a bitmap corresponding to the individual ports on the hub: Bit 0: Reserved for future use Bit 1: Port 1 Bit 2: Port 2 Etc. Bit n: Port n (implementation dependent, up to a maximum of 255 ports).
Variable	PortPwrCtrlMask	X	Variable depend-ing on number of ports on hub	Indicates if a port is not affected by a gang-mode power control request. Ports that have this field set always require a manual SetPortFeature(PORT_POWER) request to control the port's power state. Bit definition: 0 - Port does not mask the gang-mode power control capability. 1 - Port is not affected by gang-mode power commands. Manual commands must be sent to this port to turn power on and off. This is a bitmap corresponding to the individual ports on the hub: Bit 0: Reserved for future use. Bit 1: Port 1 Bit 2: Port 2 Etc. Bit n: Port n (implementation dependent, up to a maximum of 255 ports).

LEGACY KEYBOARD SUPPORT

To support applications and drivers in non-USB-aware environments (e.g., DOS), the Legacy Support Registers provide hardware support for software emulation (emulation code) of a PS/2 keyboard and/or mouse interface for USB implementations. These Legacy Support registers are implemented as described in the Open Host Controller Interface Specification for USB, release 1.0a, Appendix B.

A USB Host Controller accesses a USB keyboard and/or mouse using the standard OpenHCI descriptor-based accesses. The emulation code sets up the appropriate Endpoint Descriptors and Transfer Descriptors that cause data to be sent to or received from a USB keyboard/mouse using the normal USB protocols. When data is received from the keyboard/mouse, the emulation code is notified and becomes responsible for translating the USB keyboard/mouse data into a data sequence that is equivalent to what would be produced by a PS/2-compatible keyboard/mouse interface. The translated data is made available to the system through the legacy keyboard interface I/O addresses at 60h and 64h. Likewise, when data/control is to be sent to the keyboard (as indicated by the system writing to the legacy keyboard interface), the emulation code is notified and becomes responsible for translating the information into appropriate data to be sent to the USB keyboard/mouse through the transfer descriptor mechanism.

On the legacy keyboard/mouse interface, a read of I/O port 60h returns the current contents of the keyboard output buffer; a read of I/O port 64h returns the contents of the keyboard status register. An I/O write to port 60h or 64h puts data into the keyboard input buffer (data is being input into the keyboard subsystem). When emulation is enabled, reads and writes of registers 60h and 64h are captured in *HceInput*, *HceOutput*, and/or *HceStatus* operational registers. These operational registers are accessed by emulation code at offsets 1, 2 and 3, respectively, from the Keyboard Legacy Support Registers base I/O address for Logical Device 7. Additionally, operational register *HceControl* is accessed at offset 0.

The LPC47M120 emulation hardware described below does not directly support a mixed environment in which either the keyboard or mouse is located on USB and the other device is attached to a standard PS/2 interface. Support for a mixed environment would be solely supported by software emulation.

Keyboard/Mouse Input

Keyboard/Mouse input data is received by a USB Host Controller external to the LPC47M120. Emulation code is notified via a emulation interrupt (SMI) and presents this data to the Legacy Support Registers. For each byte of PS/2-compatible data that is to be presented to the applications software, the emulation code writes to the *HceOutput* register. The emulation code then sets the appropriate bits in the *HceStatus* register (normally, OutputFull is set for keyboard data and OutputFull plus AuxOutputFull for mouse data). If keyboard/mouse interrupts are enabled, setting the *HceStatus* register bits cause the generation of an IRQ1 for keyboard data and IRQ12 for mouse data. The emulation code then exits and waits for the next emulation interrupt.

When the host CPU exits from emulation code, it can service the pending IRQ1/IRQ12. This normally results in a read from I/O port 60h. When I/O port 60h is read, the LPC47M120 returns the current contents of HceOutput. The LPC47M120 then also clears the OutputFull bit in *HceStatus* and de-asserts IRQ1/IRQ12.

Keyboard Output

Keyboard output is indicated by application software writing data to either I/O address 60h or 64h. Upon a write to either address, the LPC47M120 captures the data in the *HceInput* register and, except in the case of a Gate A20 sequence, updates the *HceStatus* register's InputFull and CmdData bits. When the InputFull bit is set, an emulation interrupt is generated.

Upon receipt of the emulation interrupt, the emulation software reads *HceControl* and *HceStatus* to determine the cause of the emulation interrupt and performs the operation indicated by the data.

Legacy Keyboard Support Registers

The following operational registers are located at the offsets shown from the Keyboard Legacy Support Registers base I/O address for Logical Device 7.

Legacy Support Registers

OFFSET	REGISTER	DESCRIPTION
00h	*HceControl*	Used to enable and control the emulation hardware and report various status information.
01h	*HceInput*	Emulation side of the legacy Input Buffer register.
02h	*HceOutput*	Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.
03h	*HceStatus*	Emulation side of the legacy Status register.

Three of the operational registers (*HceStatus*, *HceInput*, *HceOutput*) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table below. When emulation is not enabled, reads of these registers return 0, writes are blocked and side effects are not active.

EMULATED REGISTERS

I/O ADDRESS	CYCLE TYPE	REGISTER CONTENTS ACCESSED/MODIFIED	SIDE EFFECTS
60h	IN	*HceOutput*	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	*HceInput*	OUT to port 60h will set InputFull to 1 and CmdData to 0 in *HceStatus.*
64h	IN	*HceStatus*	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	*HceInput*	OUT to port 64h will set InputFull to 1 and CmdData in *HceStatus to 1.*

HceInput **Register**

I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. When emulation is not enabled, writes are blocked. This register may be read or written directly by accessing it as shown in the Legacy Support Registers table, above. When accessed directly, reads and writes of this register have no side effects.

BIT	FIELD	R/W	DESCRIPTION
7-0	InputData	R/W	This register holds data that is written to I/O ports 60h and 64h.

HceOutput **Register**

The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in *HceStatus* is set to 0.

BIT	FIELD	R/W	DESCRIPTION
7-0	OutputData	R/W	This register hosts data that is returned when an I/O read of port 60h is performed by application software.

***HceStatus* Register**

The contents of the *HceStatus* Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register directly by accessing it as shown in the Legacy Support Registers able, above. Accessing this register directly produces no side effects.

BIT	FIELD	R/W	DESCRIPTION
0	OutputFull	R/W	The LPC47M120 sets this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in *HceControl* is set to 1, an emulation interrupt condition exists.
1	InputFull	R/W	Except for the case of a Gate A20 sequence, the LPC47M120 sets this bit to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
2	Flag	R/W	Nominally used as a system flag by software to indicate a warm or cold boot.
3	CmdData	R	The LPC47M120 sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h.
4	Inhibit Switch	R/W	This bit reflects the state of the keyboard inhibit switch and is set by software if the keyboard is NOT inhibited.
5	AuxOutputFull	R/W	IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set. This bit is set and reset by software.
6	Time-out	R/W	Used by software to indicate a time-out
7	Parity	R/W	This bit is set by software. Indicates parity error on keyboard/mouse data.

HceControl Register

BIT	FIELD	RESET	R/W	DESCRIPTION
0	EmulationEnable (Note 4)	0b	R/W	When set to 1, the LPC47M120 is enabled for legacy emulation. The LPC47M120 decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the LPC47M120 generates an emulation interrupt at appropriate times to invoke the emulation software. When set to 0, writes to 60h and 64h are blocked, reads of 60h and 64h return 0, side effects are not active and Emulation Interrupt, IRQ1 and IRQ12 outputs are blocked.
1	EmulationInterrupt (Note 1)	-	R	This bit is a static decode of the emulation interrupt condition.
2	CharacterPending	0b	R/W	When set, an emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
3	IRQEn	0b	R/W	When set, the LPC47M120 generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
4	General Purpose Bit	0b	R/W	General R/W bit. No side effects are produced when this bit is read or written.
5	GateA20Sequence (Note 2)	0b	R/W	Set by the LPC47M120 when a data value of D1h is written to I/O port 64h. Cleared by the LPC47M120 on write to I/O port 64h of any value other than D1h.
6	Reserved	0b	R/W	Reads return 0.
7	A20State (Note 3)	0b	R/W	Indicates current state of Gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.

Note 1: Producing an EmulationInterrupt from Keyboard Legacy Registers results in internal signal EmINT. EmINT is enabled on the group nSMI output by Runtime Register SMI_EN1, Bit [0].

Note 2: To reduce the number of SMIs caused by the Gate A20 sequence, an Emulation Interrupt is generated only if the A20 sequence would change the state of Gate A20.

Note 3: The A20State bit is indicated on the A20M pin.

Note 4: Logical Device 7 (Keyboard) Primary Interrupt and Secondary Interrupt Select Registers are used to select the interrupt for the Legacy Support Register signals IRQ1 and IRQ12, respectively. Typically Legacy Support Register signal IRQ1 is mapped to SER_IRQ IRQ1 and Legacy Support Register signal IRQ12 is mapped to SER_IRQ IRQ12.

Gate A20 Sequence

The Gate A20 sequence is used to enable A20M. To reduce the number of SMIs caused by the Gate A20 sequence, the LPC47M120 generates an SMI only if the A20 sequence would change the state of Gate A20.

The Gate A20 sequence is initiated with a write of D1h to port 64h. On detecting this write, the LPC47M120 sets the GateA20Sequence bit in *HceControl*. It captures the data byte in *HceInput* but does not set InputFull bit in *HceStatus*. When GateA20Sequence is set, a write of a value to I/O port 60h that has bit 1 set to a value different than A20State in *HceControl* causes InputFull to be set and causes an emulation interrupt. An SMI with both InputFull and GateA20Sequence set indicates that the application is trying to change the setting of Gate A20 on the keyboard controller. However, when GateA20Sequence is set and a write of a value to I/O port 60h that has bit 1 set to the same value as A20State in *HceControl* is detected, then no interrupt can occur.

Awrite to 64h of any value other than D1h causes GateA20Sequence to be cleared. If GateA20Sequence is active and a value of FFh is written to port 64h, GateA20Sequence is cleared but InputFull is not set. A write of any value other than D1h or FFh causes InputFull to be set which then causes an Emulation Interrupt. A write of FFh to port 64h when GateA20Sequence is not set causes InputFull to be set.

Port 92 Register

This port can only be read or written if Port 92 has been enabled via bit 2 of the KRST_GA20 Register (Logical Device 7, 0xF0) set to 1.
This register is used to support the alternate reset (nALT_RST) and alternate A20 (ALT_A20) functions. This register is reset to it's default value on Vcc POR, USB_PWR POR and Hard Reset.

PORT 92 REGISTER

Name	Port 92
Location	92h
Default Value	24h
Attribute	Read/Write
Size	8 bits

BIT	FUNCTION
7:6	Reserved. Returns 00 when read
5	Reserved. Returns a 1 when read
4	Reserved. Returns a 0 when read
3	Reserved. Returns a 0 when read
2	Reserved. Returns a 1 when read
1	ALT_A20 Signal control. Writing a 0 to this bit causes the ALT_A20 signal to be driven low. Writing a 1 to this bit causes the ALT_A20 signal to be driven high.
0	Alternate System Reset. This read/write bit provides an alternate system reset function. This function provides an alternate means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided by the Keyboard controller. This bit is set to a 0 by a system reset. Writing a 1 to this bit will cause the nALT_RST signal to pulse active (low) for 6 µs after a delay of 14 µs. Before another nALT_RST pulse can be generated, this bit must be written back to a 0.

Bit 0 of Port 92, which generates the nKBDRST signal, is used to reset the CPU under program control. If Port 92 is enabled, i.e., bit 2 of KRST_GA20 is set to 1, writing a 1 to bit 0 in the Port 92 Register causes nKBDRST to pulse low 6µs, after a delay of a 14 µs. Before another nKBDRST pulse can be generated, bit 0 must be set to 0 either by a system reset or a write to Port 92. Upon reset, this signal is driven inactive high (bit 0 in the Port 92 Register is set to 0).

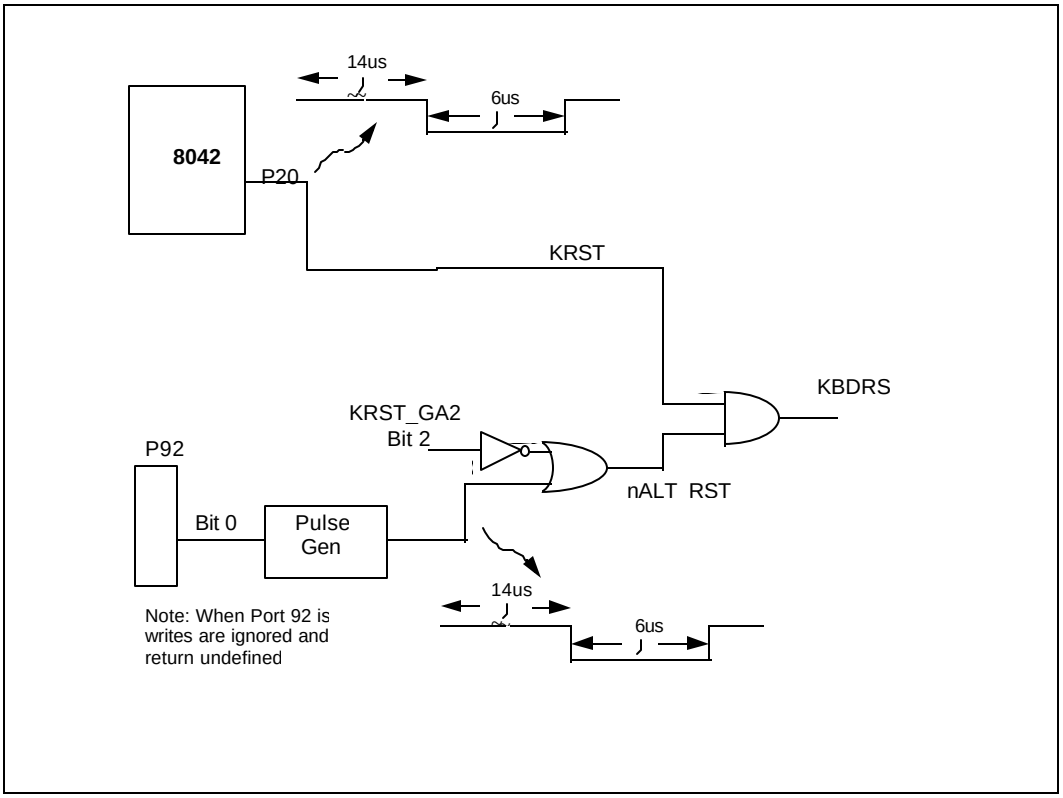


FIGURE 3 - Port 92 nKBDRST and A20M

Bit 1 of Port 92, the ALT_A20 signal, is used to force A20M to the CPU low for support of real mode compatible software. This signal is internally OR'ed with the A20State signal from the HceControl register to control the A20M output pin.

INTERRUPT GENERATING REGISTERS

The LPC47M120 contains on-chip Interrupt Generating Registers to enable external software to generate IRQ1 through IRQ15 on the Serial IRQ Interface. These registers, INT_GEN1 and INT_GEN2 as shown below, are located in the Logical Device A Runtime Block, at offsets 59h and 5Ah, respectively, from the Runtime Block base address setting (set at Index 0x60 and 0x61, Logical Device A Configuration Registers).

Registers INT_GEN1 and INT_GEN2 are enabled to output to the Serial IRQ stream by setting Logical Device A Configuration Register, at Index 0xF8, Bit 0 to '1'. When Bit 0 is set to '0', INT_GEN1 and INT_GEN2 are prevented from outputting to the Serial IRQ stream.

Writing Bits 0 through 8 to '0' in registers INT_GEN1 and INT_GEN2 enable the corresponding interrupt (INT1 through INT15) to be asserted (made active) in the Serial IRQ stream. Producing an interrupt in the Serial IRQ stream by writing these bits to '0' overrides other interrupt sources for the Serial IRQ stream. No other functional logic in the LPC47M120 sets bits in these registers. The asserted interrupt in the Serial IRQ stream from registers INT_GEN1 and INT_GEN2 is removed by writing the corresponding bit to '1'.

INT_GEN1 REGISTER

NAME	INT_GEN1
Location	Runtime Block Offset 59h
Default Value	0xFF
Attribute	Read/Write
Size	8 bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
nINT 7	nINT 6	nINT 5	nINT 4	nINT 3	nINT 2	nINT 1	Reserved

INT_GEN2 REGISTER

NAME	INT_GEN2
Location	Runtime Block Offset 5Ah
Default Value	0xFF
Attribute	Read/Write
Size	8 bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
nINT 15	nINT 14	nINT 13	nINT 12	nINT 11	nINT 10	nINT 9	nINT 8

GENERAL PURPOSE I/O

The LPC47M120 provides a set of flexible Input/Output control functions to the system designer through the 16 dedicated independently programmable General Purpose I/O pins (GPIO). These GPIO pins can be configured to perform basic I/O and all GPIO pins can generate an SMI.

GPIO Pins

The following pins include GPIO functionality. These pins are defined in the table below.

GPIO PINS	
PIN	**NAME**
31	**GP10**
32	**GP11**
33	**GP12**
34	**GP13**
35	**GP14**
36	**GP15**
37	**GP16**
38	**GP17**
58	**GP20**
59	**GP21**
60	**GP22**
61	**GP23**
62	**GP24/SYSOPT**
63	**GP25**
64	**GP26**
65	**GP27**

GPIO Description

Each GPIO port has a 1-bit data register and an 8-bit configuration control register. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 and GP2. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. All of the GPIO registers are located in the Runtime Regiister block, see Run Time Register section. The GPIO ports with their alternate functions and configuration state register addresses are listed in

Table 39 - General Purpose I/O Port Assignments .

Table 39 - General Purpose I/O Port Assignments

PIN NO. /QFP	DEFAULT FUNCTION	ALT. FUNCTION 1	DATA REGISTER	DATA REGISTER BIT NO.	REGISTER OFFSET (HEX)
31	GPIO 10		GP1	0	4B
32	GPIO 11			1	
33	GPIO 12			2	
34	GPIO 13			3	
35	GPIO 14			4	
36	GPIO 15			5	
37	GPIO 16			6	
38	GPIO 17			7	
58	GPIO 20		GP2	0	4C
59	GPIO 21			1	
60	GPIO 22			2	
61	GPIO 23			3	
62	GPIO 24	System Option		4	
63	GPIO 25			5	
64	GPIO 26			6	
65	GPIO 27			7	

Note 1: The GPIO Data and Configuration Registers are located in Runtime block at the offset shown from the Runtime block base address.

GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the “Runtime Registers” section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. Bit[0] of each GPIO Configuration Register determines the port direction, bit[1] determines the signal polarity, and bit[7] determines the output driver type select.

The basic GPIO configuration options are summarized in Table 40 - GPIO Configuration Summary.

Table 40 - GPIO Configuration Summary

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

GPIO Operation

The operation of the GPIO ports is illustrated in FIGURE 4 - GPIO FUNCTION ILLUSTRATION, below. Note: This figure is for illustration purposes only and is not intended to suggest specific implementation details. When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 41 - GPIO Read/Write Behavior).

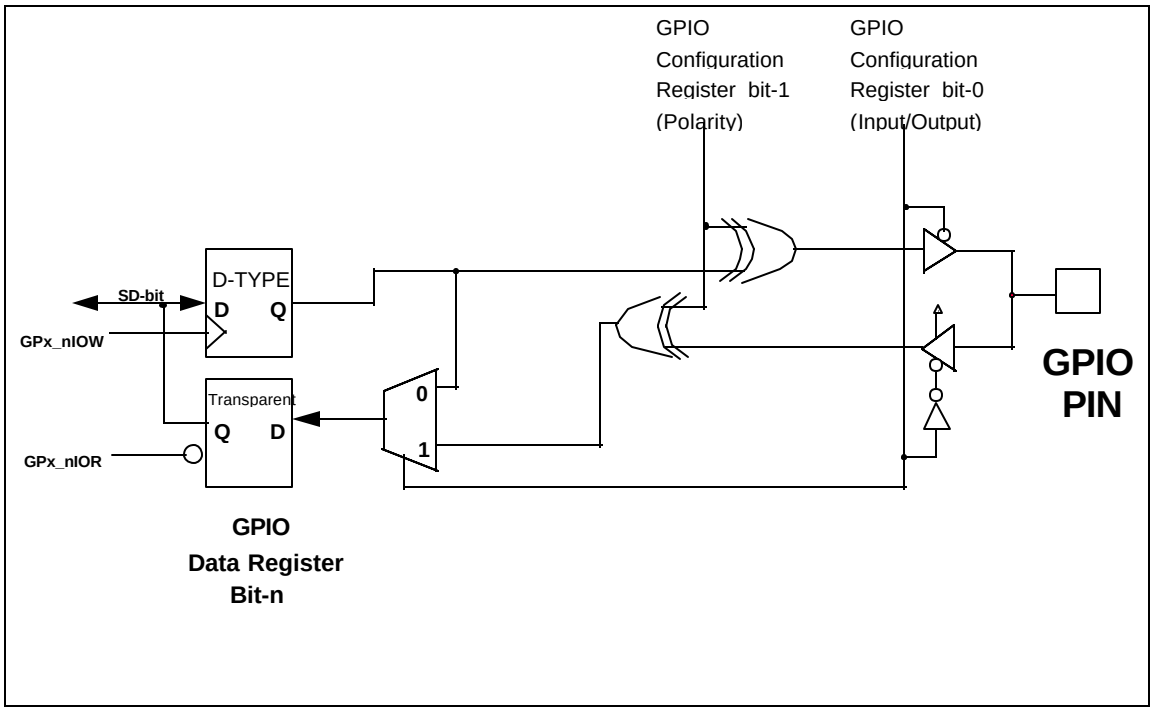


FIGURE 4 - GPIO FUNCTION ILLUSTRATION

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 41 - GPIO Read/Write Behavior). When the GPIO is programmed as an output, the pin is excluded from the SMI logic.

Table 41 - GPIO Read/Write Behavior

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

GPIO SMI Functionality

Each of the 16 LPC47M120 GPIOs can directly generate an SMI. The following SMI status and enable registers are for these GPIOs.

SMI_EN2 and SMI_ST2 for GP10 – GP17
SMI_EN3 and SMI_ST3 for GP20 – GP27

SYSTEM MANAGEMENT INTERRUPT (SMI)

The LPC47M10x implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from each of the functional blocks in the chip and each of the GPIOs. The output buffer of the nIO_SMI pin function is set to active low, open-drain output.

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1, 2 and 3. The nSMI output is then enabled onto the group nIO_SMI output pin via bit[7] in the SMI Enable Register 1. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 1.

An example logic equation for the nSMI output for SMI registers 1 and 2 is as follows:

nSMI = (EN_U1INT and IRQ_U1INT) or (EN_FINT and IRQ_FINT) or (EN_EMINT and IRQ_EMINT)

SMI Registers

The SMI event bits for the GPIOs and the Fan tachometer events are located in the SMI status and Enable registers 2 and 3. The polarity of the edge used to set the status bit and generate an SMI is controlled by the polarity bit of the control registers. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for these events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI registers are accessed at an offset from the Runtime Block Primary Base I/O Address (see Runtime register section for more information).

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1. All of these status bits are cleared at the source; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See the “Runtime Registers” section for the definition of these registers.

RUNTIME REGISTERS

The following registers are runtime registers in the LPC47M120. They are located at the address programmed in the Base I/O Address in Logical Device A at the offset shown.

Table 42 - Runtime Register Block Summary

REGISTER OFFSET (hex)	TYPE	HARD RESET	VCC POR	USB_PWRPOR	SOFT RESET	REGISTER
00	R	-	-	-	-	Reserved – reads return 0
01	R	-	-	-	-	Reserved – reads return 0
02	R	-	-	-	-	Reserved – reads return 0
03	R	-	-	-	-	Reserved – reads return 0
04	R	-	-	-	-	Reserved – reads return 0
05	R	-	-	-	-	Reserved – reads return 0
06	R	-	-	-	-	Reserved – reads return 0
07	R	-	-	-	-	Reserved – reads return 0
08	R	-	-	-	-	Reserved – reads return 0
09	R	-	-	-	-	Reserved – reads return 0
0A	R	-	-	-	-	Reserved – reads return 0
0B	R	-	-	-	-	Reserved – reads return 0
0C	R	-	-	-	-	Reserved – reads return 0
0D	R	-	-	-	-	Reserved – reads return 0
0E	R	-	-	-	-	Reserved – reads return 0
0F	R	-	-	-	-	Reserved – reads return 0
10	R/W	-	-	0x00	-	SMI_STS1
11	R/W	-	-	0x00	-	SMI_STS2
12	R/W	-	-	0x00	-	SMI_STS3
13	R	-	-	-	-	Reserved – reads return 0
14	R	-	-	-	-	Reserved – reads return 0
15	R	-	-	-	-	Reserved – reads return 0
16	R/W	-	-	0x00	-	SMI_EN1
17	R/W	-	-	0x00	-	SMI_EN2
18	R/W	-	-	0x00	-	SMI_EN3
19	R	-	-	-	-	Reserved – reads return 0
1A	R	-	-	-	-	Reserved – reads return 0
1B	R	-	-	-	-	Reserved – reads return 0
1C	R	-	-	-	-	Reserved – reads return 0
1D	R	-	-	-	-	Reserved – reads return 0
1E	R/W	-	0x01	-	-	Force Disk Change
1F	R	-	-	-	-	Floppy Data Rate Select Shadow
20	R	-	-	-	-	UART1 FIFO Control Shadow
21	R	-	-	-	-	Reserved – reads return 0
22	R	-	-	-	-	Reserved – reads return 0
23	R/W	0x01	0x01	-	-	GP10
24	R/W	0x01	0x01	-	-	GP11
25	R/W	0x01	0x01	-	-	GP12
26	R/W	0x01	0x01	-	-	GP13
27	R/W	0x01	0x01	-	-	GP14
28	R/W	0x01	0x01	-	-	GP15
29	R/W	0x01	0x01	-	-	GP16

REGISTER OFFSET (hex)	TYPE	HARD RESET	VCC POR	USB_PWRP OR	SOFT RESET	REGISTER
2A	R/W	0x01	0x01	-	-	GP17
2B	R/W	0x01	0x01	-	-	GP20
2C	R/W	0x01	0x01	-	-	GP21
2D	R/W	0x01	0x01	-	-	GP22
2E	R/W	0x01	0x01	-	-	GP23
2F	R/W	0x01	0x01	-	-	GP24
30	R/W	0x01	0x01	-	-	GP25
31	R/W	0x01	0x01	-	-	GP26
32	R/W	0x01	0x01	-	-	GP27
33	R	-	-	-	-	Reserved – reads return 0
34	R	-	-	-	-	Reserved – reads return 0
35	R	-	-	-	-	Reserved – reads return 0
36	R	-	-	-	-	Reserved – reads return 0
37	R	-	-	-	-	Reserved – reads return 0
38	R	-	-	-	-	Reserved – reads return 0
39	R	-	-	-	-	Reserved – reads return 0
3A	R	-	-	-	-	Reserved – reads return 0
3B	R	-	-	-	-	Reserved – reads return 0
3C	R	-	-	-	-	Reserved – reads return 0
3D	R	-	-	-	-	Reserved – reads return 0
3E	R	-	-	-	-	Reserved – reads return 0
3F	R	-	-	-	-	Reserved – reads return 0
40	R	-	-	-	-	Reserved – reads return 0
41	R	-	-	-	-	Reserved – reads return 0
42	R	-	-	-	-	Reserved – reads return 0
43	R	-	-	-	-	Reserved – reads return 0
44	R	-	-	-	-	Reserved – reads return 0
45	R	-	-	-	-	Reserved – reads return 0
46	R	-	-	-	-	Reserved – reads return 0
47	R	-	-	-	-	Reserved – reads return 0
48	R	-	-	-	-	Reserved – reads return 0
49	R	-	-	-	-	Reserved – reads return 0
4A	R	-	-	-	-	Reserved – reads return 0
4B	R/W	0x00	0x00	-	-	GP1
4C	R/W	0x00	0x00	-	-	GP2
4D	R	-	-	-	-	Reserved – reads return 0
4E	R	-	-	-	-	Reserved – reads return 0
4F	R	-	-	-	-	Reserved – reads return 0
50	R	-	-	-	-	Reserved – reads return 0
51	R	-	-	-	-	Reserved – reads return 0
52	R	-	-	-	-	Reserved – reads return 0
53	R	-	-	-	-	Reserved – reads return 0
54	R	-	-	-	-	Reserved – reads return 0
55	R	-	-	-	-	Reserved – reads return 0
56	R	-	-	-	-	Reserved – reads return 0
57	R	-	-	-	-	Reserved – reads return 0
58	R	-	-	-	-	Reserved – reads return 0
59	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 1

REGISTER OFFSET (hex)	TYPE	HARD RESET	VCC POR	USB_PWRP OR	SOFT RESET	REGISTER
5A	R/W	0xFF	0xFF	-	-	Interrupt Generating Register 2
5B	R	-	-	-	-	Reserved – reads return 0
5C	R	-	-	-	-	Reserved – reads return 0
5D	R	-	-	-	-	Reserved – reads return 0
5E	R	-	-	-	-	Reserved – reads return 0
5F	R	-	-	-	-	Reserved – reads return 0
60-7F	R	-	-	-	-	Reserved – reads return 0

The following registers are located at an offset from (PME_BLK) the address programmed into the base I/O address register for Logical Device A.

Table 43 - SMI, GPIO Register Description

NAME	REG OFFSET (hex)	DESCRIPTION
N/A	00 – 0F (R)	Reserved - Reads return 0
SMI_STS1 Default = 0x00 on USB_PWR POR	10 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits must be cleared at their source. Bit[0] EmINT (Legacy Keyboard Emulation) Bit[1] Reserved Bit[2] Reserved Bit[3] U1INT Bit[4] FINT Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved
SMI_STS2 Default = 0x00 on USB_PWR POR	11 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12. Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_STS3 Default = 0x00 on USB_PWR POR	12 (R/W)	SMI Status Register 3 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of ‘1’. Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27

NAME	REG OFFSET (hex)	DESCRIPTION
N/A	13 (R)	Reserved reads return 0
N/A	14 (R)	Reserved – reads return 0
N/A	15 (R)	Reserved – reads return 0
SMI_EN1 Default = 0x00 on USB_PWR POR	16 (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the group nSMI output, and the group nSMI output onto the nIO_SMI GPI/O pin, the serial IRQ stream or into the PME Logic. Unless otherwise noted, 1=Enable 0=Disable Bit[0] EN_EMINT Bit[1] Reserved Bit[2] Reserved Bit[3] EN_U1INT Bit[4] EN_FINT Bit[5] Reserved Bit[6] EN_SMI_S (Enable group SMI onto serial IRQ) Bit[7] EN_SMI (Enable group SMI onto nIO_SMI pin) (Note2)
SMI_EN2 Default = 0x00 on USB_PWR POR	17 (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_EN3 Default = 0x00 on USB_PWR POR	18 (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the group nSMI output. 1=Enable 0=Disable Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27
N/A	19 – 1D (R)	Reserved - Reads return 0

NAME	REG OFFSET (hex)	DESCRIPTION
Force Disk Change Default = 0x01 on VCC POR	1E (R/W)	Force Disk Change Bit[0] Force Disk Change for FDC0 0=Inactive 1=Active Bit[1] Force Disk Change for FDC1 0=Inactive 1=Active Force Change 0 and 1 can be written to 1 but are not clearable by software. Force Change 0 is cleared on nSTEP and nDS0 Force Change 1 is cleared on nSTEP and nDS1 DSKCHG (FDC DIR Register, Bit 7) = (nDS0 AND Force Change 0) OR (nDS1 AND Force Change 1) OR nDSKCHG Setting either of the Force Disk Change bits active '1' forces the FDD nDSKCHG input active when the appropriate drive has been selected. Bit[7:2] Reserved
Floppy Data Rate Select Shadow	1F (R)	Floppy Data Rate Select Shadow Bit[0] Data Rate Select 0 Bit[1] Data Rate Select 1 Bit[2] PRECOMP 0 Bit[3] PRECOMP 1 Bit[4] PRECOMP 2 Bit[5] Reserved Bit[6] Power Down Bit[7] Soft Reset
UART1 FIFO Control Shadow	20 (R)	UART FIFO Control Shadow 1 Bit[0] FIFO Enable Bit[1] RCVR FIFO Reset Bit[2] XMIT FIFO Reset Bit[3] DMA Mode Select Bit[5:4] Reserved Bit[6] RCVR Trigger (LSB) Bit[7] RCVR Trigger (MSB)
N/A	21 (R)	Reserved – reads return 0
N/A	22 (R)	Reserved – reads return 0
GP10 Default = 0x01 on VCC POR and HARD RESET	23 (R/W)	General Purpose I/0 bit 1.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP11 Default = 0x01 on VCC POR and HARD RESET	24 (R/W)	General Purpose I/0 bit 1.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP12 Default = 0x01 on VCC POR and HARD RESET	25 (R/W)	General Purpose I/0 bit 1.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity :=1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP13 Default = 0x01 on VCC POR and HARD RESET	26 (R/W)	General Purpose I/0 bit 1.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP14 Default = 0x01 on VCC POR and HARD RESET	27 (R/W)	General Purpose I/0 bit 1.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP15 Default = 0x01 on VCC POR and HARD RESET	28 (R/W)	General Purpose I/0 bit 1.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP16 Default = 0x01 on VCC POR and HARD RESET	29 (R/W)	General Purpose I/0 bit 1.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP17 Default = 0x01 on VCC POR and HARD RESET	2A (R/W)	General Purpose I/0 bit 1.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP20 Default = 0x01 on VCC POR and HARD RESET	2B (R/W)	General Purpose I/0 bit 2.0 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP21 Default =0x01 on VCC POR and HARD RESET	2C (R/W)	General Purpose I/0 bit 2.1 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP22 Default =0x01 on VCC POR and HARD RESET	2D (R/W)	General Purpose I/0 bit 2.2 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP23 Default = 0x01 on VCC POR and HARD RESET	2E (R/W)	General Purpose I/0 bit 2.3 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP24 Default = 0x01 on VCC POR and HARD RESET	2F (R/W)	General Purpose I/0 bit 2.4 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull

NAME	REG OFFSET (hex)	DESCRIPTION
GP25 Default = 0x01 on VCC POR and HARD RESET	30 (R/W)	General Purpose I/0 bit 2.5 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP26 Default = 0x01 on VCC POR and HARD RESET	31 (R/W)	General Purpose I/0 bit 2.6 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
GP27 Default = 0x01 on VCC POR and HARD RESET	32 (R/W)	General Purpose I/0 bit 2.7 Bit[0] In/Out : =1 Input, =0 Output Bit[1] Polarity : =1 Invert, =0 No Invert Bit[2] Reserved Bits[6:3] Reserved Bit[7] Output Type Select 1=Open Drain 0=Push Pull
N/A	33 – 4A (R)	Reserved – reads return 0
GP1 Default = 0x00 on VCC POR and HARD RESET	4B (R/W)	General Purpose I/0 Data Register 1 Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
GP2 Default = 0x00 on VCC POR and HARD RESET	4C (R/W)	General Purpose I/0 Data Register 2 Bit[0] GP20 Bit[1] GP21 Bit[2] GP22 Bit[3] GP23 Bit[4] GP24 Bit[5] GP25 Bit[6] GP26 Bit[7] GP27
N/A	4D - 58 (R)	Reserved – reads return 0

NAME	REG OFFSET (hex)	DESCRIPTION
INT_GEN1 Default = 0xFF on VCC POR and HARD RESET	59 (R/W)	Interrupt Generating Register 1 (Note 3) 0=Corresponding Interrupt cell driven low in the SER IRQ stream. Bit[0] Reserved Bit[1] nINT1 Bit[2] nINT2 Bit[3] nINT3 Bit[4] nINT4 Bit[5] nINT5 Bit[6] nINT6 Bit[7] nINT7
INT_GEN2 Default = 0xFF on VCC POR and HARD RESET	5A (R/W)	Interrupt Generating Register 2 (Note 3) 0=Corresponding Interrupt cell driven low in the SER IRQ stream. Bit[0] nINT8 Bit[1] nINT9 Bit[2] nINT10 Bit[3] nINT11 Bit[4] nINT12 Bit[5] nINT13 Bit[6] nINT14 Bit[7] nINT15
N/A	5B – 7F (R)	Reserved – reads return 0

Note 2: The nIO_SMI pin is inactive when the internal group SMI signal is inactive and when the SMI enable bit (EN_SMI, bit 7 of the SMI_EN2 register) is '0'. With an OD output buffer type, the nIO_SMI pin is floating when inactive.

Note 3: These bits when read indicate the current bit status. These bits are set to "0" by writing "0" to individual bit locations in this register. Producing an interrupt in the SER IRQ stream by setting these bits to "0", overrides other interrupt sources for the SER IRQ stream. No other functional logic in the LPC47M120 sets bits in this register.

CONFIGURATION

The Configuration of the LPC47M120 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components. The LPC47M120 is designed for motherboard applications in which the resources required by their components are known. With its flexible resource allocation architecture, the LPC47M120 allows the BIOS to assign resources at POST.

SYSTEM ELEMENTS

Primary Configuration Address Decoder
After a hard reset (PCI_RESET# pin asserted) or Vcc Power On Reset the LPC47M120 is in the Run Mode with all logical devices disabled. The logical devices may be configured through two standard Configuration I/O Ports (INDEX and DATA) by placing the LPC47M120 into Configuration Mode.

The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the LPC47M120 is in Configuration Mode.

The SYSOPT pin is latched on the falling edge of the PCI_RESET# or on Vcc Power On Reset to determine the configuration register's base address. The SYSOPT pin is used to select the CONFIG PORT's I/O address at power-up. Once powered up the configuration port base address can be changed through configuration registers CR26 and CR27. **The SYSOPT pin is a hardware configuration pin which is shared with the GP24 signal on pin 62.**

Note. An external pull-down resistor is required for the base IO address to be 0x02E for configuration. An external pull-up resistor is required to move the base IO address for configuration to 0x04E.

The INDEX and DATA ports are effective only when the chip is in the Configuration State.

PORT NAME	SYSOPT= 0 10k PULL-DOWN RESISTOR	SYSOPT= 1 10K PULL-UP RESISTOR	TYPE
CONFIG PORT (Note)	0x02E	0x04E	Write
INDEX PORT (Note)	0x02E	0x04E	Read/Write
DATA PORT	INDEX PORT + 1		Read/Write

Note: The configuration port base address can be relocated through CR26 and CR27.

Entering the Configuration State

The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = <0xAA>

CONFIGURATION SEQUENCE
To program the configuration registers, the following sequence must be followed:

1) Enter Configuration Mode
2) Configure the Configuration Registers
3) Exit Configuration Mode.

Enter Configuration Mode
To place the chip into the Configuration State the Config Key is sent to the chip's CONFIG PORT. The config key consists of 0x55 written to the CONFIG PORT. Once the configuration key is received correctly the chip enters into the Configuration State (The auto Config ports are enabled).

Configuration Mode
The system sets the logical device information and activates desired logical devices through the INDEX and DATA ports. In configuration mode, the INDEX PORT is located at the CONFIG PORT address and the DATA PORT is at INDEX PORT address + 1.

The desired configuration registers are accessed in two steps:

1) Write the index of the Logical Device Number Configuration Register (i.e., 0x07) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT
2) Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note: If accessing the Global Configuration Registers, step (a) is not required.

Exit Configuration Mode
To exit the Configuration State the system writes 0xAA to the CONFIG PORT. The chip returns to the RUN State.

Note: Only two states are defined (Run and Configuration). In the Run State the chip will always be ready to enter the Configuration State.

Programming Example
The following is an example of a configuration program in Intel 8086 assembly language.

```
;------------------------------.
; ENTER CONFIGURATION MODE   |
;------------------------------'
MOV     DX,02EH
MOV     AX,055H
OUT     DX,AL
;------------------------------.
; CONFIGURE REGISTER CRE0,   |
; LOGICAL DEVICE 8          |
;------------------------------'
MOV     DX,02EH
MOV     AL,07H
OUT     DX,AL ;Point to LD# Config Reg
MOV     DX,02FH
MOV     AL, 08H
OUT     DX,AL;Point to Logical Device 8
;
MOV     DX,02EH
MOV     AL,E0H
OUT     DX,AL    ; Point to CRE0
MOV     DX,02fH
MOV     AL,02H
OUT     DX,AL    ; Update CRE0
;------------------------------.
; EXIT CONFIGURATION MODE    |
;------------------------------'
MOV     DX,02EH
MOV     AX,0AAH
OUT     DX,AL
```

Notes: HARD RESET: PCI_RESET# pin asserted
SOFT RESET: Bit 0 of Configuration Control register set to one
All host accesses are blocked for 500µs after Vcc POR (see Power-up Timing Diagram)

Table 44 - LPC47M120 Configuration Registers Summary

INDEX	TYPE	HARD RESET	VCC POR	USB_PWR POR	SOFT RESET	CONFIGURATION REGISTER
GLOBAL CONFIGURATION REGISTERS						
0x02	W	0x00	0x00	0x00	-	Config Control
0x03	R	-	-	-	-	Reserved – reads return 0
0x07	R/W	0x00	0x00	0x00	0x00	Logical Device Number
0x20	R	0x5C	0x5C	0x5C	0x5C	Device ID - hard wired
0x21	R	0x00	0x00	0x00	0x00	Device Rev - hard wired
0x22	R/W	0x00	0x00	0x00	0x00	Power Control
0x23	R	0x00	0x00	0x00	-	Power Mgmt.
0x24	R/W	0x40	0x40	0x40	-	ADDR
0x26	R/W	Sysopt=0: 0x2E Sysopt=1: 0x4E	Sysopt=0: 0x2E Sysopt=1: 0x4E	Sysopt=0: 0x2E Sysopt=1: 0x4E	-	Configuration Port Address Byte 0 (Low Byte)
0x27	R/W	Sysopt=0: 0x00 Sysopt=1: 0x00	Sysopt=0: 0x00 Sysopt=1: 0x00	Sysopt=0: 0x00 Sysopt=1: 0x00	-	Configuration Port Address Byte 1 (High Byte)
0x28	R	-	-	-	-	Reserved
0x2A	R/W	-	0x00	-	-	TEST 6
0x2B	R/W	-	0x00	-	-	TEST 4
0x2C	R/W	-	0x00	-	-	TEST 5
0x2D	R/W	-	0x00	-	-	TEST 1
0x2E	R/W	-	0x00	-	-	TEST 2
0x2F	R/W	-	0x00	-	-	TEST 3
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDD)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x03, 0xF0	0x03, 0xF0	0x03, 0xF0	0x03, 0xF0	Primary Base I/O Address
0x70	R/W	0x06	0x06	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	0x02	0x02	DMA Channel Select
0xF0	R/W	0x0E	0x0E	0x0E	-	FDD Mode Register
0xF1	R/W	0x00	0x00	0x00	-	FDD Option Register
0xF2	R/W	0xFF	0xFF	0xFF	-	FDD Type Register
0xF4	R/W	0x00	0x00	0x00	-	FDD0
0xF5	R/W	0x00	0x00	0x00	-	FDD1
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (Serial Port 1)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	0x00	0x00	-	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 6 CONFIGURATION REGISTERS (Reserved)						

INDEX	TYPE	HARD RESET	VCC POR	USB_PWR POR	SOFT RESET	CONFIGURATION REGISTER
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (Keyboard)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate Note 2
0x60 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address, Keyboard Legacy Support Registers
0x70	R/W	0x00	0x00	0x00	0x00	Primary Interrupt Select Note 3
0x72	R/W	0x00	0x00	0x00	0x00	Second Interrupt Select Note 3
0xF0	R/W	0x00	0x00	0x00	-	KRESET and GateA20 Select
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (Reserved)						
LOGICAL DEVICE A CONFIGURATION REGISTERS (Runtime Block)						
0x30	R/W	0x00	0x00	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0xF0	R/W	-	-	0x00	-	OSC_CLK Note 1
0xF1	R/W	-	-	0x24	-	IdVendor_Low Note 1
0xF2	R/W	-	-	0x04	-	IdVendor_High Note 1
0xF3	R/W	-	-	0x20	-	IdProduct_Low Note 1
0xF4	R/W	-	-	0x01	-	IdProduct_High Note 1
0xF5	R/W	-	-	0x00	-	BcdDevice_Low Note 1
0xF6	R/W	-	-	0x00	-	BcdDevice_High Note 1
0xF7	R/W	-	-	0x00	-	HubControl_1 Note 1
0xF8	R/W	0x00	0x00	0x00	0x00	INT_G Register Note 1
LOGICAL DEVICE B CONFIGURATION REGISTERS (Reserved)						

Note: Reserved registers are read-only, reads return 0.

Note 1: These registers are powered by USB_PWR.

Note 2: Logical Device 7 (Keyboard) Activate Register activates registers at fixed locations 60h, 64h and 92h, and Keyboard Legacy Support Registers HceControl, HceInput, HceOutput and HceStatus.

Note 3: Logical Device 7 (Keyboard) Primary Interrupt and Secondary Interrupt Select Registers are used to select the interrupt for the Legacy Support Register signals IRQ1 and IRQ12, respectively. Typically Legacy Support Register signal IRQ1 is mapped to SER_IRQ IRQ1 and Legacy Support Register signal IRQ12 is mapped to SER_IRQ IRQ12.

Chip Level (Global) Control/Configuration Registers[0x00-0x2F]
The chip-level (global) registers lie in the address range [0x00-0x2F]. The design MUST use all 8 bits of the ADDRESS Port for register selection. All unimplemented registers and bits ignore writes and return zero when read.

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration Mode.

Table 45 - Chip Level Registers

REGISTER	ADDRESS	DESCRIPTION	NOTES
Chip (Global) Control Registers			
	0x00 - 0x01	Reserved - Writes are ignored, reads return 0.	
Config Control Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0x02 W	The hardware automatically clears this bit after the write, there is no need for software to clear the bits. Bit 0 = 1: Soft Reset. Refer to the "Configuration Registers" table for the soft reset value for each register.	
	0x03 - 0x06	Reserved - Writes are ignored, reads return 0.	
Logical Device # Default = 0x00 on VCC POR, USB_PWR POR SOFT RESET and HARD RESET	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.	
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.	
Chip Level, SMSC Defined			
Device ID - Hard wired Default = 0x5C	0x20 R	A read only register which provides device identification. Bits[7:0] = 0x5C when read.	
Device Rev Hard wired = Current Revision	0x21 R	A read only register which provides device revision information. Bits[7:0] = current revision when read.	
PowerControl Default = 0x00 on VCC POR, USB_PWR POR SOFT RESET and HARD RESET	0x22 R/W	Bit[0] FDC Power Bit[1] Reserved Bit[2] Reserved Bit[3] Reserved Bit[4] Serial Port 1 Power Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved	

REGISTER	ADDRESS	DESCRIPTION	NOTES
Power Mgmt Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0x23 R/W	Bit[0] FDC Bit[1] Reserved Bit[2] Reserved Bit[3] Reserved Bit[4] Serial Port 1 Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved For each bit above (except Reserved) 0 = Intelligent Pwr Mgmt off 1 = Intelligent Pwr Mgmt on	
ADDR Default = 0x40, on VCC POR, USB_PWR POR and HARD RESET	0x24 R/W	Bit[0] Reserved Bit[1] PLL Control 0 = PLL is On (backward compatible) 1 = PLL is off Bit [5:2] Reserved, set to zero Bit [6] 16-Bit Address Qualification 0 = 12-Bit Address Qualification 1 = 16-Bit Address Qualification Note: For normal operation, bit 6 should be set. Bit[7] Reserved	
Chip Level Vendor Defined	0x25	Reserved - Writes are ignored, reads return 0.	
Configuration Address Byte 0 Default =0x2E (Sysopt=0) =0x4E (Sysopt=1) on VCC POR, USB_PWR POR and HARD RESET	0x26	Bit[7:1] Configuration Address Bits [7:1] Bit[0] = 0 See Note 1	
Configuration Address Byte 1 Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0x27	Bit[7:0] Configuration Address Bits [15:8] See Note 1	
	0x28	Reserved - Writes are ignored, reads return 0.	
Chip Level Vendor Defined	0x29	Reserved - Writes are ignored, reads return 0.	
TEST 6 Default = 0x00, on VCC POR	0x2A R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 4 Default = 0x00, on VCC POR	0x2B R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 5 Default = 0x00, on VCC POR	0x2C R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	

REGISTER	ADDRESS	DESCRIPTION	NOTES
TEST 1 Default = 0x00, on VCC POR	0x2D R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 2 Default = 0x00, on VCC POR	0x2E R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 3 Default = 0x00, on VCC POR	0x2F R/W	Test Modes: Reserved for SMSC. Users should not write to this register, may produce undesired results.	

Note 1: To allow the selection of the configuration address to a user defined location, these Configuration Address Bytes are used. There is no restriction on the address chosen, except that A0 is 0, that is, the address must be on an even byte boundary. As soon as both bytes are changed, the configuration space is moved to the specified location with no delay (Note: Write byte 0, then byte 1; writing CR27 changes the base address).

The configuration address is only reset to its default address upon a Hard Reset, Vcc POR or USB_PWR POR.

Note: The default configuration address is either 02E or 04E, as specified by the SYSOPT pin.

Logical Device Configuration/Control Registers [0x30-0xFF]

Used to access the registers that are assigned to each logical unit. This chip supports three logical units and has three sets of logical device registers. The three logical devices are Floppy, Serial and Legacy Keyboard. A separate set (bank) of control and configuration registers exists for each logical device and is selected with the Logical Device # Register (0x07).

The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State. The logical register addresses are shown in the table below.

Table 46 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	NOTES
Activate (Note1) Default = 0x00 on VCC POR, USB_PWR POR , HARD RESET and SOFT RESET	(0x30)	Bits[7:1] Reserved, set to zero. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive	
Logical Device Control	(0x31-0x37)	Reserved – Writes are ignored, reads return 0.	
Logical Device Control	(0x38-0x3F)	Vendor Defined - Reserved - Writes are ignored, reads return 0.	
Memory Base Address	(0x40-0x5F)	Reserved – Writes are ignored, reads return 0.	
I/O Base Address Note 2 (see Device Base I/O Address Table) Default = 0x00 on VCC POR, USB_PWR POR , HARD RESET and SOFT RESET	(0x60-0x6F) 0x60,2,... = addr[15:8] 0x61,3,... = addr[7:0]	Registers 0x60 and 0x61 set the base address for the device. If more than one base address is required, the second base address is set by registers 0x62 and 0x63. Refer to Table 48 - I/O Base Address Configuration Register Description for the number of base address registers used by each device. Unused registers will ignore writes and return zero when read.	

Table 47 - Logical Device Registers

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	NOTES
Interrupt Select Defaults : 0x70 = 0x00 or 0x06 (Note3) on VCC POR, USB_PWR POR , HARD RESET and SOFT RESET 0x72 = 0x00, on VCC POR, USB_PWR POR , HARD RESET and SOFT RESET	(0x70,0x72)	Refer to Interrupt Configuration Register description. Unused register (0x72) will ignore writes and return zero when read. Interrupts default to edge high (ISA compatible).	
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
DMA Channel Select Default = 0x02 or 0x04 (Note 4) on VCC POR, USB_PWR POR , HARD RESET and SOFT RESET	(0x74,0x75)	0x74 is only implemented for FDC. 0x75 is not implemented and ignores writes and returns zero when read. Refer to DMA Channel Configuration.	
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return zero when read.	
Logical Device Configuration	(0xE0-0xFE)	Reserved – Vendor Defined (see SMSC defined Logical Device Configuration Registers).	
Reserved	0xFF	Reserved	

Note 1: A logical device will be active and powered up according to the following equation:

DEVICE ON (ACTIVE) = (Activate Bit SET or Pwr/Control Bit SET).
The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other.

Note 2: If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

Note 3: The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Note 4: The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02.

Table 48 - I/O Base Address Configuration Register Description

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Reserved	n/a	n/a	n/a
0x02	Reserved	n/a	n/a	n/a
0x03	Reserved	n/a	n/a	n/a
0x04	Serial Port 1	0x60,0x61	[0x0100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MSR +5 : LSR +6 : MSR +7 : SCR
0x05	Reserved	n/a	n/a	n/a
0x06	Reserved	n/a	n/a	n/a
0x07	KYBD	n/a	Not Relocatable Fixed Base Address: 60, 64, 92	60 : Data Register 64 : Command/Status Reg. 92 : PORT92
		0x60, 0x61	[0x0100:0x0FFC] ON 4 BYTE BOUNDARIES	+0 : HceControl +1 : HceInput +2 : HceOutput +3 : HceStatus
0x08	Reserved	n/a	n/a	n/a
0x09	Reserved	n/a	n/a	n/a
0x0A	Runtime Register Block	0x60, 0x61	[0x0000:0x0F7F] on 128 byte boundaries	+00: . . +5F :
0x0B	Reserved	n/a	n/a	n/a
Config. Port	Config. Port	0x26, 0x27 (Note 2)	0x0100:0x0FFE On 2 byte boundaries	See Configuration Registers in Table1. Accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 1: This chip uses address bits [A11:A0] to decode the base address of each of its logical devices. Lower address bits are used to decode individual logical device register locations. Register blocks are locatable on byte boundaries indicated in BASE I/O RANGE column. Bit 6 of the ADDR Global Configuration Register (CR24) must be set to '1' and Address Bits [A15:A12] must be '0' for 16 bit address qualification.

Note 2: The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be replaced via the global configuration registers at 0x26 and 0x27.

Table 49 - Interrupt Select Configuration Register Description

NAME	REG INDEX	DEFINITION	NOTES
Primary Interrupt Select Default=0x00 or 0x06 (Note 1) on VCC POR, USB_PWR POR, HARD RESET and SOFT RESET	0x70 (R/W)	Bits[3:0] selects which interrupt is used for the primary Interrupt. 0x00= no interrupt selected 0x01= IRQ1 0x02= IRQ2/nSMI 0x03= IRQ3 0x04= IRQ4 0x05= IRQ5 0x06= IRQ6 0x07= IRQ7 0x08= IRQ8 0x09= IRQ9 0x0A= IRQ10 0x0B= IRQ11 0x0C= IRQ12 0x0D= IRQ13 0x0E= IRQ14 0x0F= IRQ15 Note: All interrupts are edge high Note: nSMI is active low	

Note: An Interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND :
For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
For the Serial Port logical device by setting any combination of bits D0-D3 in the IER, and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
Note: IRQs are disabled if not used/selected by any Logical Device. Refer to Note A.
Note: nSMI must be disabled to use IRQ2.
Note: All IRQ's are available in Serial IRQ mode.
Note 1: The default value of the Primary Interrupt Select register for logical device 0 is 0x06.

Table 50 - DMA Channel Select Configuration Register Description

NAME	REG INDEX	DEFINITION	NOTES
DMA Channel Select Default=0x02 or 0x04 (Note 1) on VCC POR, USB_PWR POR, HARD RESET and SOFT RESET	0x74 (R/W)	Bits[2:0] select the DMA Channel. 0x00= Reserved 0x01= DMA1 0x02= DMA2 0x03= DMA3 0x04-0x07= No DMA active	

Note: A DMA channel is activated by setting the DMA Channel Select register to [0x01-0x03] AND :
For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
Note: The DMA channel must be disabled if not used/selected by any Logical Device. Refer to Note A.
Note 1: The default value of the DMA Channel Select register for logical device 0 (FDD) is 0x02.

Note A. Logical Device IRQ and DMA Operation

1) IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel must be disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

   a) FDC: For the following cases, the IRQ and DMA channel used by the FDC are disabled. Will not respond to the DMA request.
   Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".
   The FDC is in power down (disabled).

   b) Serial Ports: Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupt is disabled.

SMSC Defined Logical Device Configuration Registers

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by Vcc or USB_POR (as shown) or the PCI_RESET# signal. These registers are not affected by soft resets.

Table 51 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	NOTES
FDD Mode Register Default = 0x0E on VCC POR, USB_PWR POR and HARD RESET	0xF0 R/W	Bit[0] Floppy Mode = 0 Normal Floppy Mode (default) = 1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode = 0 Burst Mode is enabled = 1 Non-Burst Mode (default) Bit[3:2] Interface Mode = 11 AT Mode (default) = 10 (Reserved) = 01 PS/2 = 00 Model 30 Bit[4] Reserved Bit[5] Reserved, set to zero Bit[6] FDC Output Type Control = 0 FDC outputs are OD12 open drain (default) = 1 FDC outputs are O12 push-pull Bit[7] FDC Output Control = 0 FDC outputs active (default) = 1 FDC outputs tri-stated Note: Bits 6 & 7 do not affect the parallel port FDC pins.	

Table 51 - Floppy Disk Controller, Logical Device 0 [Logical Device Number = 0x00]

NAME	REG INDEX	DEFINITION	NOTES
FDD Option Register Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0xF1 R/W	Bit[0] Forced Write Protect = 0 Inactive (default) = 1 FDD nWRTPRT input is forced active when either of the drives has been selected. nWRTPRT (to the FDC Core) = WP (FDC SRA register, bit 1) = (nDS0 AND Forced Write Protect) OR (nDS1 AND Forced Write Protect) OR nWRTPRT (from the FDD Interface) OR Floppy Write Protect Note: The Floppy Write Protect bit is in the Device Disable register. Note: Boot floppy is always drive 0. Note: the Force Write Protect bit also applies to the Parallel Port FDC. Bit[1] Reserved Bits[3:2] Density Select = 00 Normal (default) = 01 Normal (reserved for users) = 10 1 (forced to logic "1") = 11 0 (forced to logic "0") Bit[7:4] Reserved.	
FDD Type Register Default = 0xFF on VCC POR, USB_PWR POR and HARD RESET	0xF2 R/W	Bits[1:0] Floppy Drive A Type Bits[3:2] Floppy Drive B Type Bits[5:4] Reserved (could be used to store Floppy Drive C type) Bits[7:6] Reserved (could be used to store Floppy Drive D type) Note: The LPC47M120 supports two floppy drives	
	0xF3 R	Reserved, Read as 0 (read only)	
FDD0 Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0xF4 R/W	Bits[1:0] Drive Type Select: DT1, DT0 Bits[2] Read as 0 (read only) Bits[4:3] Data Rate Table Select: DRT1, DRT0 Bits[5] Read as 0 (read only) Bits[6] Precompensation Disable PTS =0 Use Precompensation =1 No Precompensation Bits[7] Read as 0 (read only)	
FDD1	0xF5 R/W	Refer to definition and default for 0xF4	

Table 52 - Serial Port 1, Logical Device 4 [Logical Device Number = 0x04]

NAME	REG INDEX	DEFINITION	NOTES
Serial Port 1 Mode Register Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0xF0 R/W	Bit[0] Reserved Bit[1] High Speed = 0 High Speed Disabled(default) = 1 High Speed Enabled Bit[6:2] Reserved, set to zero Bit[7]: Reserved	

Table 53 - KYBD, Logical Device 7 [Logical Device Number = 0x07]

NAME	REG INDEX	DEFINITION	NOTES
KRST_GA20 Default = 0x00 on VCC POR, USB_PWR POR and HARD RESET	0xF0 R/W	KRESET and GateA20 Select Bit[0,1] Reserved Bit[2] Port 92 Select = 0 Port 92 Disabled = 1 Port 92 Enabled Bit[7:3] Reserved	
	0xF1 - 0xFF	Reserved - read as '0'	

Table 54 - Runtime Registers, Logical Device A

NAME	REG INDEX	DEFINITION	NOTES
OSC_CLK Default = 0x00 on USB_PWR POR	0xF0 R/W	Bit [0] Reserved Bit [1] OSC_CLK 0=48MHz clock is connected to the ICLK pin (default) 1=24MHz crystal is connected to the ICLK and OCLK pins Bits [7:2] Reserved	
IdVendor_Low Default=0x24 on USB_PWR POR	0xF1 R/W	Bit[7:0] USB Vendor ID (assigned by USB), low byte Default reset to SMSC ID	System Note1
IdVendor_High Default=0x04 on USB_PWR POR	0xF2 R/W	Bit[7:0] USB Vendor ID (assigned by USB), high byte Default reset to SMSC ID	System Note1
IdProduct_Low Default=0x20 on USB_PWR POR	0xF3 R/W	Bit[7:0] USB Product ID (assigned by manufacturer), low byte Default reset to SMSC silicon ID	System Note1
IdProduct_High Default=0x01 on USB_PWR POR	0xF4 R/W	Bit[7:0] USB Product ID (assigned by manufacturer), high byte Default reset to SMSC silicon ID	System Note1
BcdDevice_Low Default=0x00 on USB_PWR POR	0xF5 R/W	Bit[7:0] USB Device Release Number (in binary coded decimal), low byte Default set to SMSC silicon revision	System Note1
BcdDevice_High Default=0x00 on USB_PWR POR	0xF6 R/W	Bit[7:0] USB Device Release Number (in binary coded decimal), high byte Default set to SMSC silicon revision	System Note1
HubControl_1 Default=0x00 on USB_PWR POR	0xF7 R/W	Bit[0] GangedPWR Bit[1:6] Reserved Bit[7] NHubReset	
INT_G Default = 0x00 on VCC POR, USB_PWR POR, HARD RESET and SOFT RESET	0xF8 R/W	Bit[7:1] Reserved Bit[0] INT_G Enable 0=Disable Interrupt Generating Registers 1=Enable Interrupt Generating Registers When Bit 0 is set to "0" INT_GEN1 and INT_GEN2 registers (Runtime Registers at runtime block offset 59 and 5A) are prevented from outputting to the SER IRQ stream.	
	0xFA- 0xFF	Reserved – read as '0'	

Table 55 - HubControl_1 Register Definition

HubControl_1 RESET=0b0xx00000[1] INDEX=0xF7			HUB CONTROL REGISTER1
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	NhubReset	R/W	**NHubReset** – When this bit is asserted (0), the hub controller is in a reset state. The hub will not respond to any enumeration or device requests. When this bit is de-asserted (1), the hub controller is ready to receive packets from the Root Host Controller. Each Port will then be enabled via a control packet from the Host
6	Strp1	R/W	**Strap Select** – The two bits define the number of USB Down Stream Ports that will be enabled. The Default value, which is sampled during VT POR, is defined by the Input Pins nStrp1 and nStrp0. The state of the Strp1 and Strp0 bits are the logical invert of the associated input pins. The number of ports enabled is defined in the following table: Strp1 Strp0 Ports Enabled 1 1 Reserved – This selection is for future use 1 0 PD1+/-,PD2+/- 0 1 PD1+/-,PD2+/-,PD3+/- 0 0 PD1+/-,PD2+/-,PD3+/-,PD4+/- (Default) Note: For backward compatibility with existing older revision devices, the default for Strp1 and Strp0 is 00. This implies that the input pins nStrp1 and nStrp0, are required to not be connected. See Note 1:
5	Strp0	R/W	
4:1	Reserved	R	Reserved – Reads return 0
0	GangedPWR	R/W	**Ganged Power Sense enable** – When this bit is set (1), the Power Control block of the USB HUB device will internally OR the Power OK sense pins (nPWROK[4:1]) and Power Enable (nPWREN[4:1]) pins. This will allow the system designer the ability to reduce implementation costs by reducing the external current hardware. In this mode, since only one Sense and Enable pin is required, the unused input pins must be tied to VDD (1) and the unused output pins may be left unconnected. See Note 1:

Note 1: When the specified USB Down Stream Ports are disabled via the Strp0/Strp1 bit or nStrp1/nStrp0 Pins, the associated Power OK sense pins (nPWROK[x]) and Power Enable (nPWREN[x]) pins are also disabled. The USB Down Stream Port nPWROK[x] input pin can be a NC (No Connect) pin or tied High (1) and the Power Enable (nPWREN[x]) pin will be forced low (0).

[1] The "HubControl_1" register Reset value, is dependant on two Input Pins. The Default value of this register is a function nStrp1 and nStrp0 input pins, which are sampled during VTR POR. The state of the Strp1 and Strp0 bits are the logical invert of the associated input pins.

OPERATIONAL DESCRIPTION

Maximum Guaranteed Ratings

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-55° to +150°C
Lead Temperature Range .....Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground.....V_{cc}+0.3V
Negative Voltage on any pin, with respect to Ground.....-0.3V
Maximum V_{cc}.....+5.5V

Note: Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC Electrical Characteristics

(T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}			±10	µA	V_{IN} = 0
High Input Leakage	I_{IH}			±10	µA	V_{IN} = V_{CC}
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12mA
Backdrive Protect/ChiProtect (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#, USB+, USB-, PD+[1:4], PD-[1:4])	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#, USB+, USB-, PD+[1:4], PD-[1:4]) Inputs and Outputs in High Impedance State	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
LPC Bus Pins (LAD[3:0], LDRQ#, LPCPD#, LFRAME#)	I_{IL}			± 10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
IOUSB Input Levels: Differential Input Sensitivity (Notes 3 & 5)	VDI	0.2			V	|(PD+) - (PD-)|
Differential Common Mode Range (Note 3)	VCM	0.8		2.5	V	Includes VDI range
Single-Ended Receiver Threshold (Note 3)	VSE	0.8 (Note 4)		2.0 (Note 5)	V	
IOUSB Output Levels: Static Output Low (Note 3)	VOL	0.0		0.3	V	RL of 15 KΩ to GND
Static Output High (Note 3)	VOH	2.8		3.6	V	RL of 1.5 KΩ to 3.6V
Output Signal Crossover Voltage (Note 3)	VCRS	1.3		2.0	V	
V_{CC} Supply Current Active	I_{CCI}			15	mA	All outputs open, all inputs at a fixed state (i.e., 0V or 3.3V.
USB_PWR Supply Voltage	V_{TR}	V_{CC} min -.5V		V_{CC} max	V	V_{CC} must not be greater than .5V above USB_PWR
USB_PWR Supply Current Active	I_{TRI}	5		25	mA	All outputs , all inputs at a fixed state (i.e., 0V or 3.3V.

Note 1: All output leakage's are measured with the current pins in high impedance
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state.
Note 3: Voltages are measured from the local ground potential, unless otherwise specified.
Note 4: This minimum value is referred to as V_{IL} in the USB Spec 1.1
Note 5: This maximum value is referred to as V_{IH} in the USB Spec 1.1
Note 6: This input sensitivity is valid when both differential data inputs are in the differential common mode range.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V ±10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (pF)
SER_IRQ	50
nLAD[3:0]	50
LDRQ#	50
nDIR	240
nSTEP	240
nDS0-1	240
TXD1	50

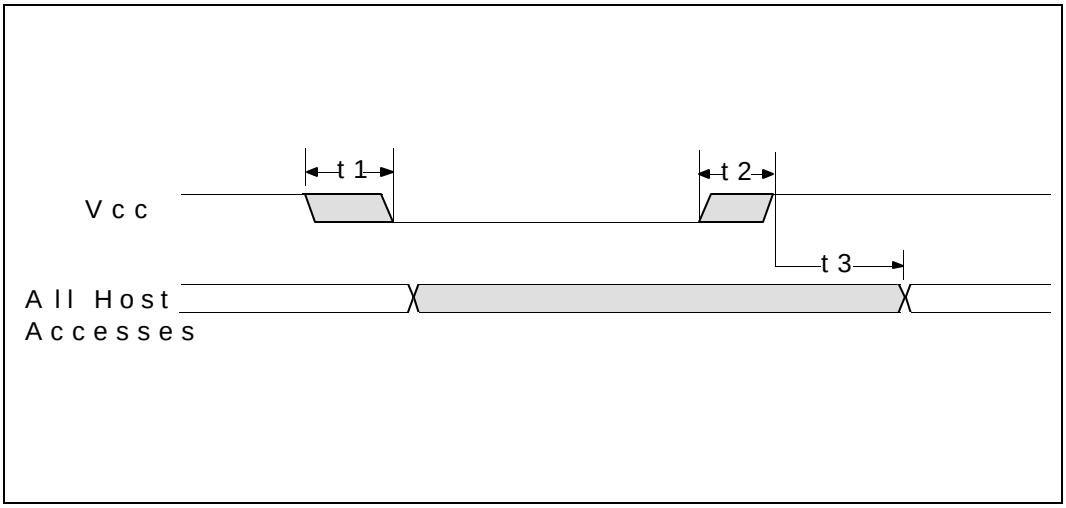


FIGURE 5 - POWER-UP TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Powerup (Note 1)	125		500	µs

Note 1: Internal write-protection period after Vcc passes 2.7 volts on power-up

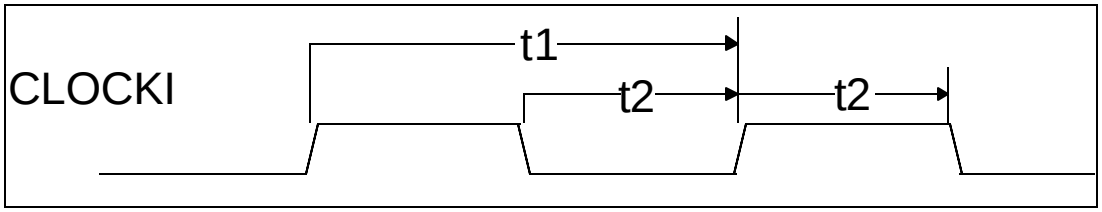


FIGURE 6 - INPUT CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
t1	Clock Cycle Time for 32KHZ		31.25		µs
t2	Clock High Time/Low Time for 32KHz		16.53		µs
	Clock Rise Time/Fall Time (not shown)			5	ns

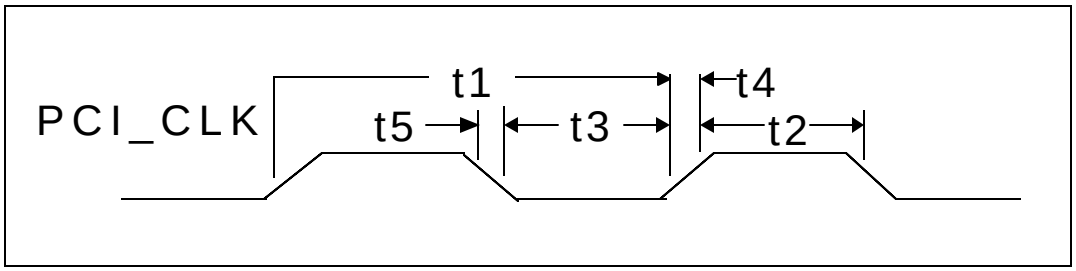


FIGURE 7 – PCI CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

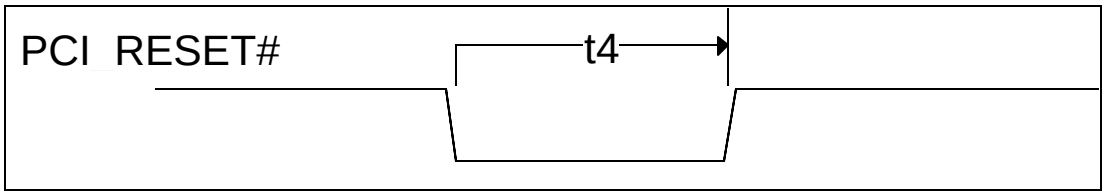


FIGURE 8 - RESET TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t4	PCI_RESET# width (Note 1)				µs

Note 1: The PCI_RESET# width is dependent upon the processor clock. The PCI_RESET# must be active while the clock is running and stable.

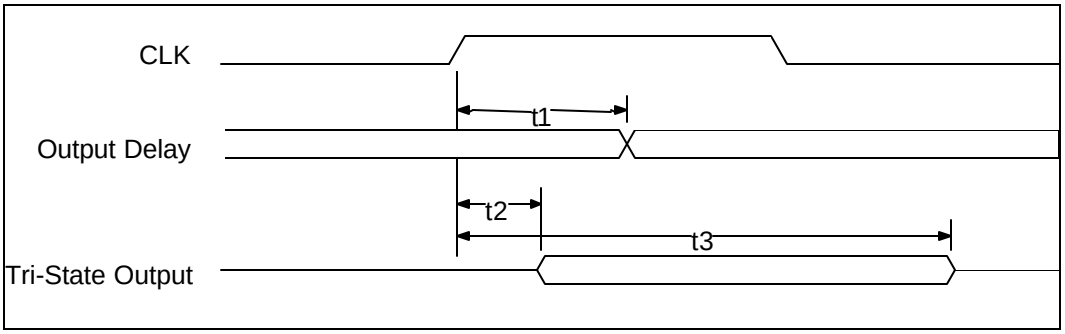


FIGURE 9 – OUPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

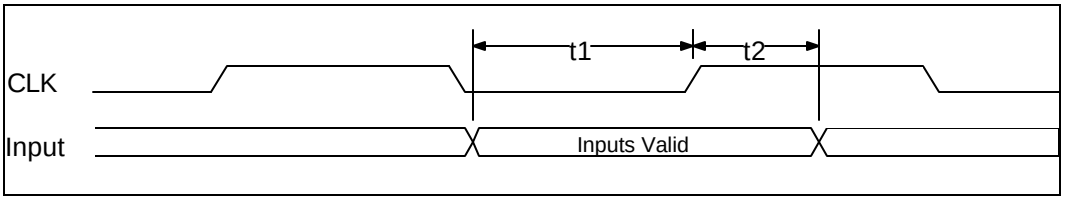


FIGURE 10 – INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns

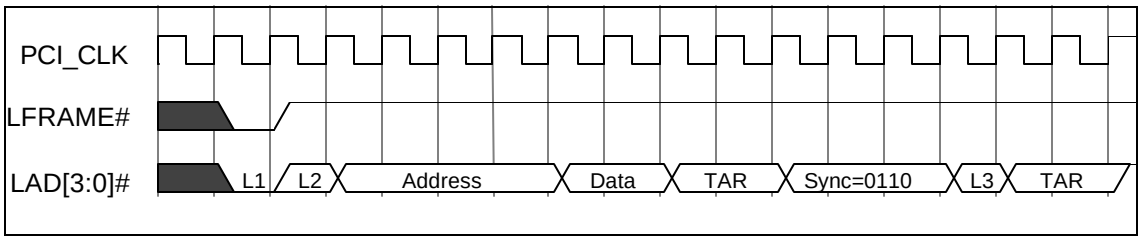


FIGURE 11 – I/O WRITE

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

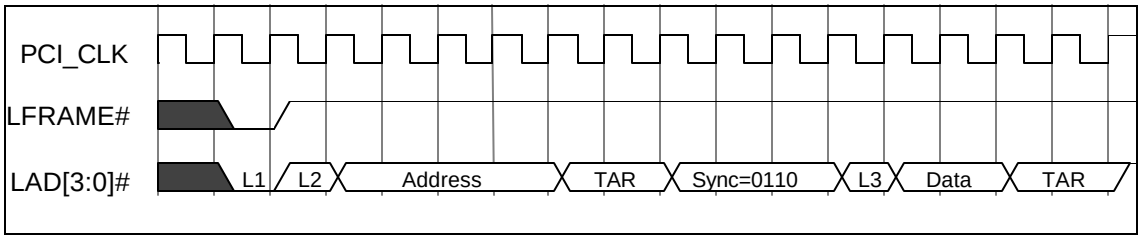


FIGURE 12 – I/O READ

Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

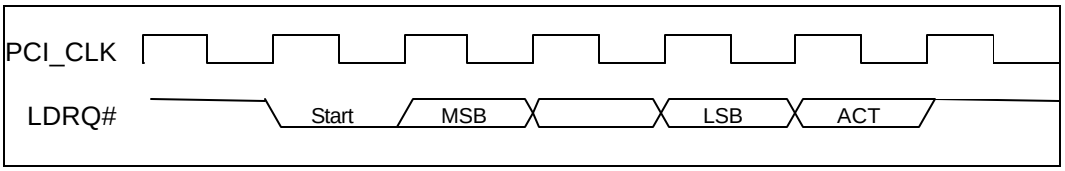


FIGURE 13 – DMA REQUEST ASSERTION THROUGH LDRQ#

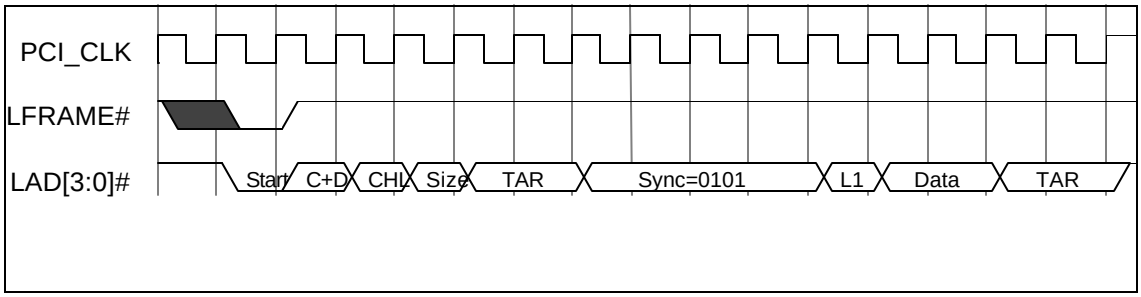


FIGURE 14 – DMA WRITE (FIRST BYTE)

Note: L1=Sync of 0000

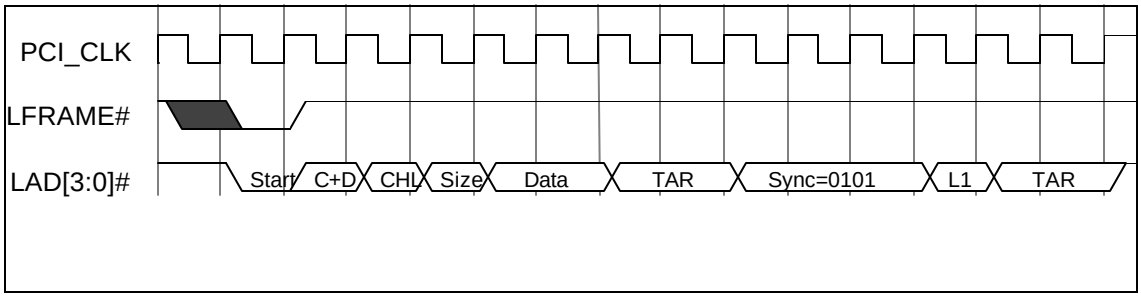


FIGURE 15 – DMA READ (FIRST BYTE)

Note: L1=Sync of 0000

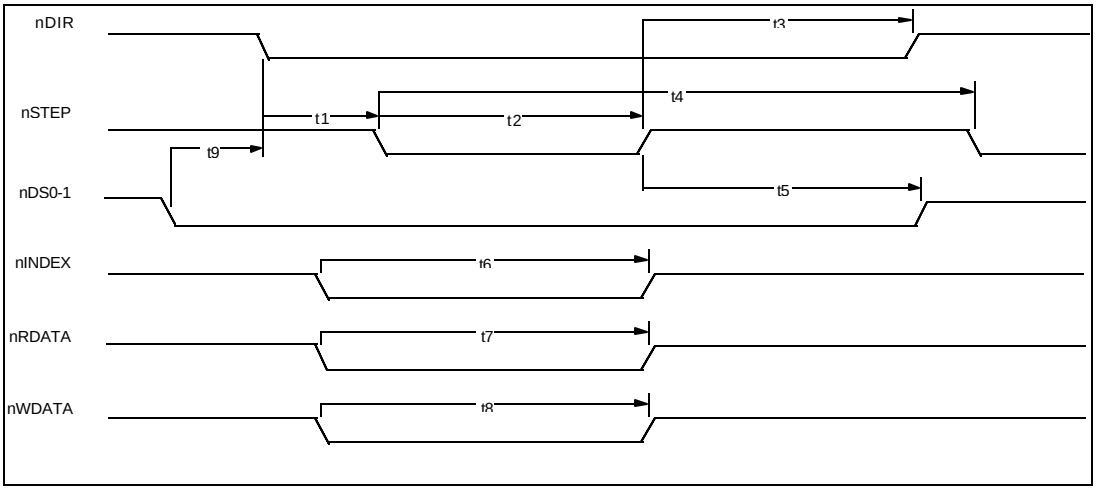


FIGURE 16 – FLOPPY DISK DRIVE TIMING (AT MODE ONLY)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low (Note)		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-1, Setup Time nDIR Low (Note)	0			ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz)
WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)
Note: The nDS0-1 setup and hold times must be met by software.

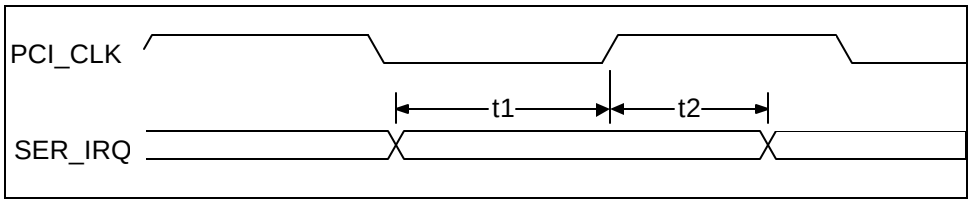


FIGURE 17 – SETUP AND HOLD TIME

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

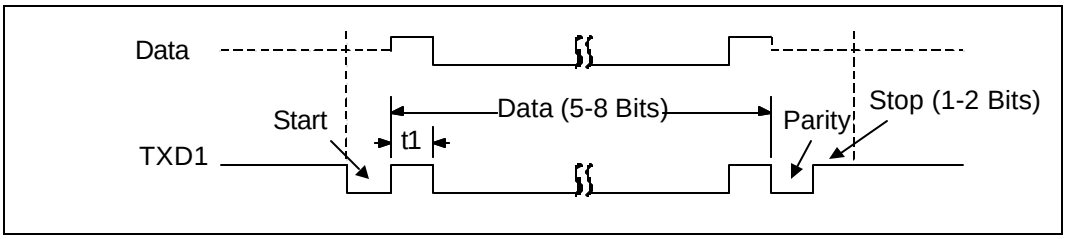


FIGURE 18 – SERIAL PORT DATA

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR} [1]		nsec

Note 1: t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the "Baud Rate" table in the "Serial Port" section.

USB Hub Interface Timing

The timing diagrams, for the USB Hub Interface, use a 50pF capacitive load on each of the differential outputs. Listed below are the driver characteristics and the data transfer timings. These values were taken from the USB Specification, Revision 1.1.

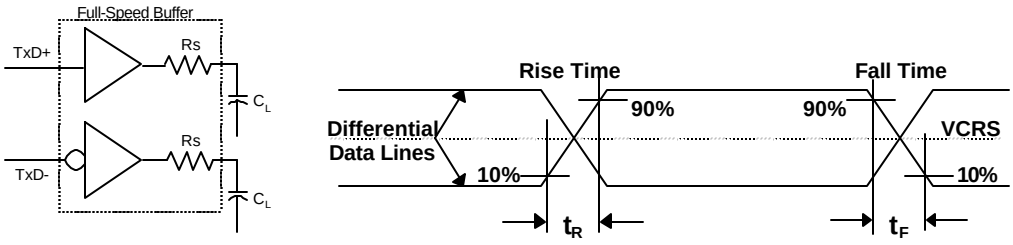
Table 56 - Electrical Source Characteristics

The values listed below satisfy speeds up to 12Mbps (Full Speed)

PARAMETER	SYM	CONDITIONS (NOTE 1,2,3)	MIN	MAX	UNIT
DRIVER CHARACTERISTICS:					
Transition Time:		Note 4,5 and FIGURE 19 CL = 50 pF			
Rise Time	TR		4	20	ns
Fall Time	TF	CL = 50 pF	4	20	ns
Differential Rise/Fall Time Matching	TRFM	(TR/TF) Note 9	90	111.11	%
Drive Output Impedance	ZDRV	Steady State Drive	28	44	Ω

PARAMETER	SYM	CONDITIONS (NOTE 1,2,3)	MIN	MAX	UNIT
DATA TRANSFER TIMINGS:					
Full Speed Data Rate	TDRATE	Notes 8, 10, & 12	11.9700	12.0300	Mbs
Frame Interval	TFRAME	Note 8	0.9995	1.0005	ms
Clock Period	TPERIOD	Note 10	80	86	ns
Source Jitter Total (including frequency tolerance): To next Transition For Paired Transitions	 TDJ1 TDJ2	Note 6, 7, & 9 FIGURE 21	 -3.5 -4.0	 3.5 4.0	 ns ns
Source Jitter for Differential Transition to SEO Transition	TDEOP	Note 7 and FIGURE 22	-2	5	ns
Receiver Jitter: To next Transition For Paired Transitions	 TJR1 TJR2	Note 7 and FIGURE 23	 -18.5 -9	 18.5 9.0	 ns ns
Source SEO interval of EOP	TEOPT	Note 7 and FIGURE 22	160	175	ns
Receiver SEO interval of EOP	TEOPR	Note 7 and FIGURE 22	82		ns
Width of SEO interval during differential transition	TFST	Note 11		14	ns

Note 1: All voltages are measured from the local ground potential, unless otherwise specified.
Note 2: All timing use a capacitive load (CL) to ground of 50pF, unless otherwise specified.
Note 3: Full speed timings have a 1.5KΩ pull-up to a voltage of 3.0V - 3.6V on the D+ data line.
Note 4: Measured from 10% to 90% of the data signals.
Note 5: The rising and falling edges should be smoothly transitioning (monotonic).
Note 6: Timing differences between the differential data signals.
Note 7: Measured at crossover point of differential data signals.
Note 8: For a more detailed description of the Data Signaling Rate and the Frame Interval see sections 7.1.11 and 7.1.12 in the USB Spec 1.1.
Note 9: Excluding the first transition from the idle state.
Note 10: The accuracy of the host controller's data rate must be known and controlled to better than ±0.05%
Note 11: During differential signal transitions both PD+ and PD- may temporarily be less that VIH(min). This period can be up to 14ns.
Note 12: The data-rate tolerance for host, hub, and full-speed functions is ±0.25%



Full Speed: 4 to 20ns at C_L = 50pF

Note: The output impedance of the buffer with a series resistance (Rs) is 28Ω to 44Ω.

FIGURE 19 - DATA SIGNAL RISE AND FALL TIME

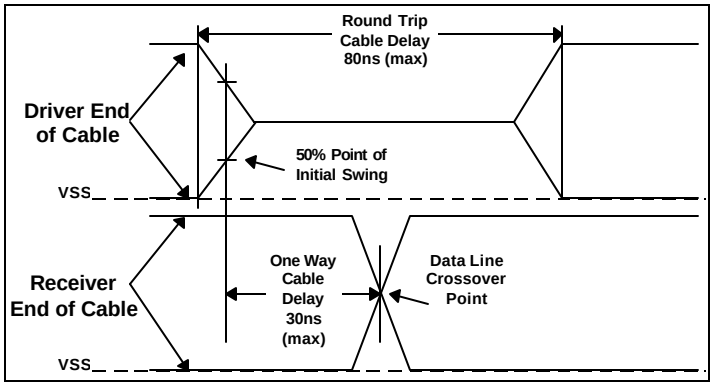


FIGURE 20 - CABLE DELAY

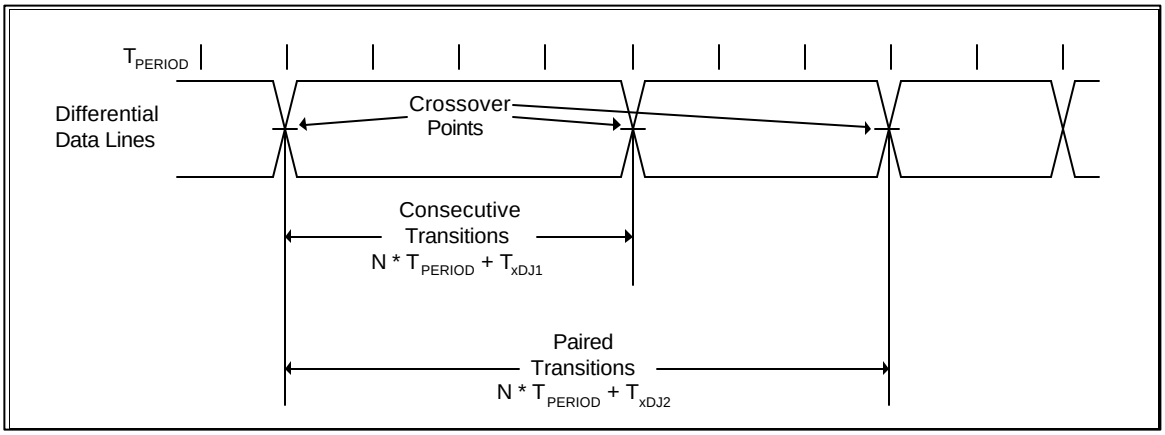


FIGURE 21 - DIFFERENTIAL DATA JITTER

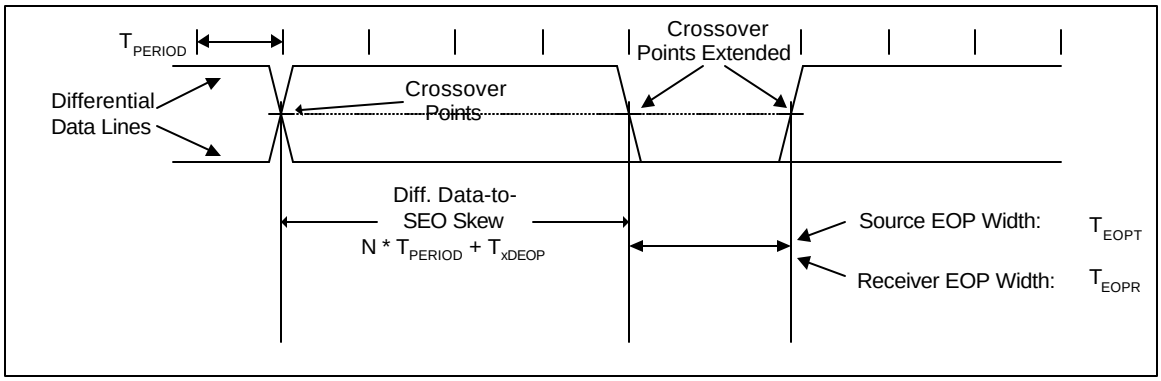


FIGURE 22 - DIFFERENTIAL TO EOP TRANSITION SKEW AND EOP WIDTH

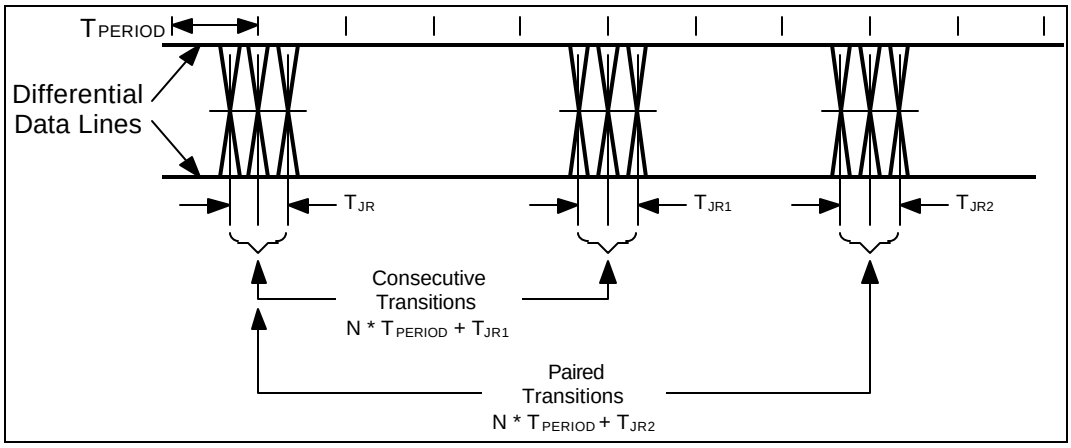


FIGURE 23 - RECEIVER JITTER TOLERANCE

MECHANICAL PACKAGE

100 Pin QFP Package Outline, 3.9 MM Footprint

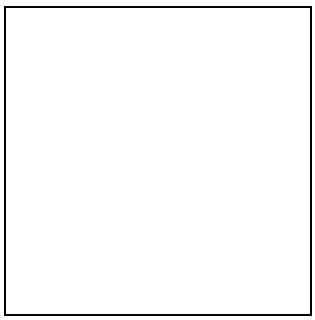


FIGURE 24 - 100 PIN QFP PACKAGE OUTLINE

	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.57	~	2.87	Body Thickness
D	23.65	~	24.15	X Span
D/2	11.825	11.95	12.075	$^1/_2$ X Span Measured from Centerline
D1	19.90	~	20.10	X body Size
E	17.65	~	18.15	Y Span
E/2	8.825	8.95	9.075	$^1/_2$ Y Span Measured from Centerline
E1	13.90	~	14.10	Y body Size
H	0.10	~	0.203	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e	0.65 Basic			Lead Pitch
q	0^o	~	7^o	Lead Foot Angle
W	0.20	~	0.40	Lead Width
R1	0.10	~	0.25	Lead Shoulder Radius
R2	0.15	~	0.40	Lead Foot Radius
ccc	~	~	0.09	Coplanarity *(Assemblers)*
ccc	~	~	0.10	Coplanarity *(Test House)*

Notes:

[1] Controlling Unit: millimeter
[2] Tolerance on the position of the leads is ± 0.065 mm maximum
[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.
[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated

APPENDIX - TEST MODE

Board Test Mode

Board test mode can be entered as follows:
On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.
Exit board test mode as follows:
On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.

See the “XNOR-Chain Test Mode” section below for a description of this board test mode.

XNOR-CHAIN TEST MODE

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See FIGURE 25 - XNOR-CHAIN TEST STRUCTURE, below.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the LPC47M120 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

The PCI_RESET# pin is not included in the XNOR-Chain. The XNOR-Chain output pin# is 49, No Connect. See the following subsections for more details.

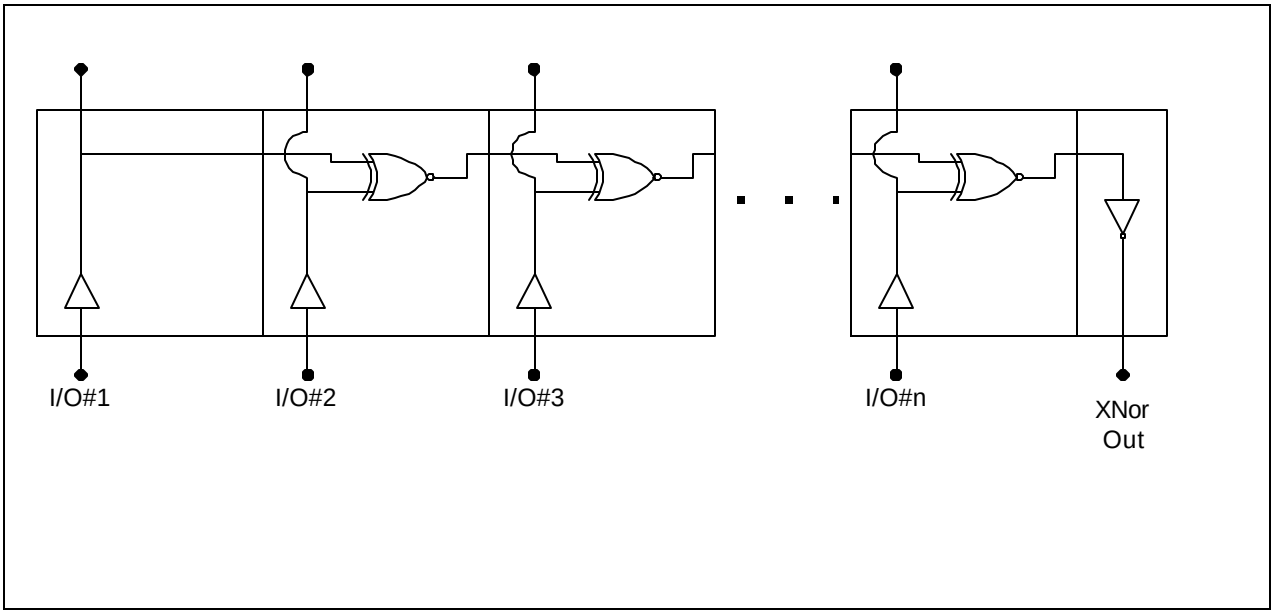


FIGURE 25 - XNOR-CHAIN TEST STRUCTURE

Introduction

The LPC47M120 provides board test capability through the XNOR chain. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

All pins on the chip are inputs to the XNOR chain, with the exception of the following:

- VCC (QFP pins 18, 39, 57 and 71, USB_PWR (QFP pins 87 and 96).
- VSS (QFP pins 8, 30, 43, 66, 76 and 99).
- PCI_RESET# (QFP pin 26), OCLK (QFP pin 98) and TSTOUT (XNOR output, QFP pin 49).
- NC pins (QFP pins 43 through 57).

To put the chip in the XNOR chain test mode, tie LAD0 (pin 20) and LFRAME# (QFP pin 24) low. Then toggle PCI_RESET# (QFP pin 26) from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 (QFP pin 20) and LFRAME# (QFP pin 24) become part of the chain.

To exit the XNOR chain test mode tie LAD0 (QFP pin 20) or LFRAME# (QFP pin 24) high. Then toggle PCI_RESET# (QFP pin 26) from a low to a high state. A VCC POR will also cause the XNOR chain test mode to be exited. To verify the test mode has been exited, observe the output at TSTOUT (QFP pin 49). Toggling any of the input pins should not cause its state to change.

Setup

Warning: Ensure power supply is off during setup.

1) Connect VSS (QFP pins 8, 30, 43, 66, 76 and 99) to ground.
2) Connect VCC (QFP pins 18, 39, 57 and 71), USB_PWR (QFP pins 87 and 96) to Power (3.3V).

3) Connect an oscilloscope or voltmeter to TSTOUT (QFP pin 49).
4) All other pins should be tied to ground.

Testing

1) Turn power on.
2) With LAD0 (QFP pin 20) and LFRAME# (QFP pin 24), low, bring PCI_RESET# (QFP pin 26) high. The chip is now in XNOR chain test mode. At this point, all inputs to the XNOR chain are low. The output, on TSTOUT (QFP pin 49), should also be low. Refer to INITIAL CONFIG on Truth Table 1.
3) Bring pin 100 high. The output on TSTOUT (QFP pin 49) should go high. Refer to STEP ONE on Truth Table 1.
4) In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on TSTOUT should now be low. Refer to END CONFIG on Truth Table 1.
5) The current state of the chip is now represented by INITIAL CONFIG in Truth Table 2.
6) Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The output on TSTOUT should now be low. Refer to Truth Table 2.
7) To exit test mode, tie LAD0 (QFP pin 20) OR LFRAME# (QFP pin 24) high, and toggle PCI_RESET# (QFP pin 26) from a low to a high state.

TRUTH TABLE 1 - Toggling Inputs in Descending Order

	PIN 100	PIN 99	PIN 98	PIN 97	PIN 96	PIN ...	PIN 1	OUTPUT QFP PIN 49
INITIAL CONFIG	L	L	L	L	L	L	L	L
STEP 1	H	L	L	L	L	L	L	H
STEP 2	H	H	L	L	L	L	L	L
STEP 3	H	H	H	L	L	L	L	H
STEP 4	H	H	H	H	L	L	L	L
STEP 5	H	H	H	H	H	L	L	H
…	…	…	…	…	…	…	…	…
STEP N	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

TRUTH TABLE 2 - Toggling Inputs in Ascending Order

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 100	OUTPUT QFP PIN 49
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L
STEP 5	L	L	L	L	L	H	H	H
	…	…	…	…	…	…	…	…
STEP N	L	L	L	L	L	L	H	L
END CONFIG	L	L	L	L	L	L	L	L

APPENDIX – REFERENCE DOCUMENTS

1) PCI Bus Power Management Interface Specification, Rev. 1.0, Draft, March 18, 1997.
2) Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document.
3) Universal Serial Bus (USB) Specification, Revision 1.1, September 23, 1998
4) Advanced Configuration and Power interface Specification, Revision 1.0

LPC47M120 REVISIONS

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
106, 107	Table 52 and Table 53	Merged tables have been corrected.	03/21/01