National Semiconductor

May 2003

LMS1485
5V Low Power RS-485 Differential Bus Transceiver

General Description

The LMS1485 is a low power differential bus/line transceiver designed for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation and V.11 and X.27.

The LMS1485 combines a TRI-STATE™ differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The LMS1485 is build with National's advanced BiCMOS process and is available in a 8-Pin SOIC package. It is a drop-in socket replacement to ADI's ADM1485 and LTC's LT1485.

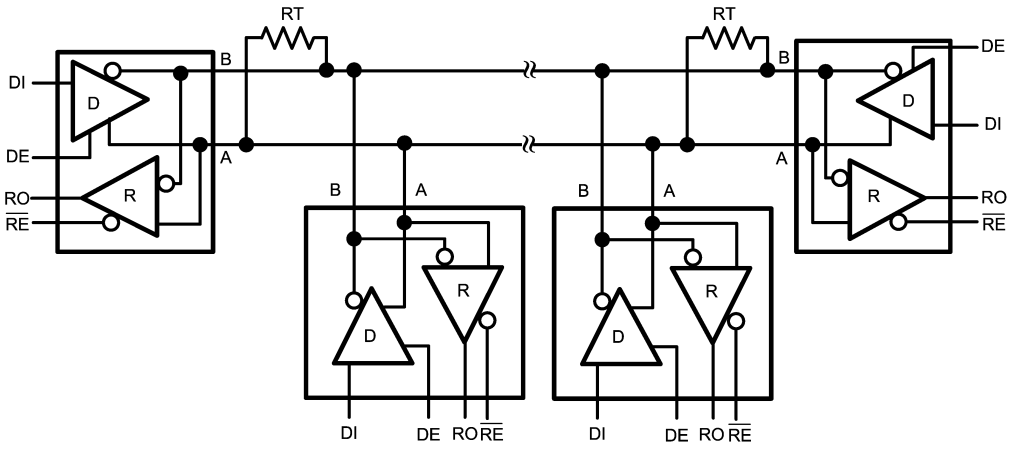
Features

- Meet ANSI standard RS-485-A and RS-422-B
- Data rate 30Mbps
- Single supply voltage operation, 5V
- Wide input and output voltage range
- Thermal shutdown protection
- Short circuit protection
- Driver propagation delay 10ns
- Receiver propagation delay 25ns
- High impedance outputs with power off
- Open circuit fail-safe for receiver
- Extended operating temperature range –40˚C to 85˚C
- ESD rating 8kV HBM
- Drop-in replacement to ADM1485 and LT1485
- Available in 8-pin SOIC
- Low supply current, I_{CC} = 1mA

Applications

- Low power RS-485 systems
- Network hubs, bridges, and routers
- Point of sales equipment (ATM, barcode scanners,…)
- Local area networks (LAN)
- Integrated service digital network (ISDN)
- Industrial programmable logic controllers
- High speed parallel and serial applications
- Multipoint applications with noisy environment

Typical Application



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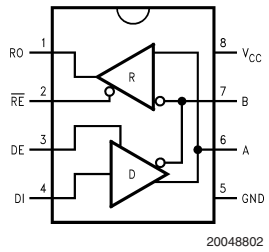
A typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in TRI-STATE, See National Application Note, AN-847 for further information.

Connection Diagram

8-Pin SOIC



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Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMS1485M	LMS1485M	95 Units/Rail	M08A
	LMS1485MX		2.5k Units Tape and Reel	
	LMS1485IM	LMS1485IM	95 Units/Rail	
	LMS1485IMX		2.5k Units Tape and Reel	

Pin Descriptions

Pin #	I/O	Name	Function
1	O	RO	Receiver Output: If A > B by 200 mV, RO will be high; If A < B by 200mV, RO will be low. RO will be high also if the inputs (A and B) are open (non-terminated)
2	I	$\overline{RE}$	Receiver Output Enable: RO is enabled when $\overline{RE}$ is low; RO is in TRI-STATE when $\overline{RE}$ is high
3	I	DE	Driver Output Enable: The driver outputs (A and B) are enabled when DE is high; they are in TRI-STATE when DE is low. Pins A and B also function as the receiver input pins (see below)
4	I	DI	Driver Input: A low on DI forces A low and B high while a high on DI forces A high and B low when the driver is enabled
5	N/A	GND	Ground
6	I/O	A	Non-inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
7	I/O	B	Inverting Driver Output and Receiver Input pin. Driver Output levels conform to RS-485 signaling levels
8	N/A	V_{CC}	Power Supply: $4.75V \leq V_{CC} \leq 5.25V$

Truth Table

DRIVER SECTION				
$\overline{RE}$	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
$\overline{RE}$	**DE**	**A-B**		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	X	X		Z
L	L	OPEN *		H

Note: * = Non Terminated, Open Input only

X = Irrelevant

Z = TRI-STATE

H = High level

L = Low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 2)	7V
Input Voltage, V_{IN} (DI, DE, or $\overline{RE}$)	−0.3V to V_{CC}+ 0.3V
Voltage Range at Any Bus Terminal (AB)	−7V to 12V
Receiver Outputs	−0.3V to V_{CC} + 0.3V
Package Thermal Impedance, θ_{JA}	
SOIC (Note 3)	125˚C/W
Junction Temperature (Note 3)	150˚C
Operating Free-Air Temperature Range, T_A	
Commercial	0˚C to 70˚C
Industrial	−40˚C to 85˚C
Storage Temperature Range	−65˚C to 150˚C
ESD Rating (Note 4) (Note 8)	8kV
ESD Rating (Note 4) (Note 9)	2kV
Soldering Information	
Infrared or Convection (20 sec.)	235˚C

Operating Ratings

	Min	Nom	Max	
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode) V_{IN} or V_{IC}	−7		12	V
High-Level Input Voltage, V_{IH} (Note 5)	2			V
Low-Level Input Voltage, V_{IL} (Note 5)			0.8	V
Differential Input Voltage, V_{ID} (Note 6)			±12	V

Electrical Characteristics

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver Section						
V_{OD}	Differential Output Voltage	R = ∞ (*Figure 1*)			5	V
V_{OD1}	Differential Output Voltage	R = 50Ω (*Figure 1*), RS-422	2		5	V
V_{OD2}	Differential Output Voltage	R = 27Ω (*Figure 1*), RS-485	1.5		5	V
V_{OD3}	Differential Output Voltage	V_{TEST} = −7V to + 12V (*Figure 2*)	1.5		5	V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R = 27Ω or 50Ω (*Figure 1*), (Note 7)	−0.2		0.2	V
V_{OC}	Common-Mode Output Voltage	R = 27Ω or 50Ω (*Figure 1*), (Note 7)			3	V
ΔV_{OC}	Change in Magnitude of Common-Mode Output Voltage	R = 27Ω or 50Ω (*Figure 1*), (Note 7)	−0.2		0.2	V
I_{OSD}	Short-Circuit Output Current	V_O = High, −7V≤V_{CM} ≤+12V	−250		250	mA
		V_O = Low, −7V ≤V_{CM} ≤+12V	−250		250	
V_{INL}	CMOS Input Logic Threshold Low	DE, DI, $\overline{RE}$			0.8	V
V_{INH}	CMOS Input Logic Threshold High	DE, DI, $\overline{RE}$	2			V
I_{IN}	Logic Input Current	DE, DI	−1		1	µA
Receiver Section						
V_{TH}	Differential Input Threshold Voltage	−7V ≤ V_{CM} ≤ + 12V	−0.2		+0.2	V
ΔV_{TH}	Input Hysteresis Voltage (V_{TH+} − V_{TH-})	V_{CM} = 0		70		mV
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ + 12V	12			kΩ
I_{IN}	Input Current (A, B)	V_{IN} = 12V			1	mA
		V_{IN} = −7V	−0.8			
I_{RE}	Logic Enable Input Current	$\overline{RE}$	−1		1	µA
V_{OL}	CMOS Low-Level Output Voltage	I_{OL} = 4mA			0.4	V

Electrical Characteristics (Continued)

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	CMOS High-Level Output Voltage	I_{OH} = −4mA	4			V
I_{OSR}	Short-Circuit Output Current	V_O = GND or V_{CC}	7		85	mA
I_{OZ}	Tristate Output Leakage Current	0.4V ≤V_O ≤+2.4V	−1		1	µA
Power Supply Current						
I_{CC}	Supply Current	Driver Enabled, Output = No Load, Digital Inputs = GND or V_{CC}		1.1	2.2	mA
		Driver Disabled, Output = No Load, Digital Inputs = GND or V_{CC}		1	2.2	mA
Switching Characteristics						
Driver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	R_L = 54Ω, C_L = 100pF (*Figure 3*, *Figure 7*)		11	20	ns
T_{SKEW}	Driver Output Skew	R_L = 54Ω, C_L = 100pF (*Figure 3*, *Figure 7*)		1		ns
T_R, T_F	Driver Rise and Fall Time	R_L = 100Ω, C_L = 100pF (*Figure 3*, *Figure 7*)		5	10	ns
T_{ENABLE}	Driver Enable to Ouput Valid Time	(*Figure 4*, *Figure 8*)		18	32	ns
$T_{DISABLE}$	Output Disable Time	(*Figure 4*, *Figure 8*)		20	40	ns
Receiver						
T_{PLH}, T_{PHL}	Propagation Delay Input to Output	C_L = 15pF (*Figure 5*, *Figure 7*)	18	33	55	ns
T_{SKEW}	Receiver Output Skew	(*Figure 5*, *Figure 7*)		2		ns
T_{ENABLE}	Receiver Enable Time	(*Figure 6*, *Figure 10*)		6	25	ns
$T_{DISABLE}$	Receiver Disable Time	(*Figure 6*, *Figure 10*)		15	25	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics

Note 2: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: ESD rating based upon human body model, 100pF discharged through 1.5kΩ.

Note 5: Voltage limits apply to DI, DE, $\overline{RE}$ pins.

Note 6: Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

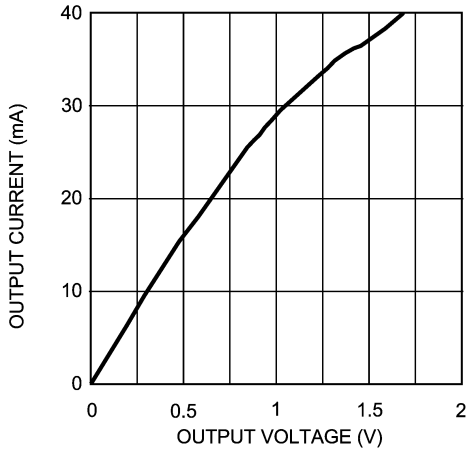
Note 7: $|\Delta V_{OD}|$ and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively when the input changes from high to low levels.

Note 8: ESD rating applies to pins 6 and 7

Note 9: ESD rating applies to pins 1, 2, 3, 4, 5 and 8

Typical Performance Characteristics

Receiver Output Low Voltage vs. Output Current



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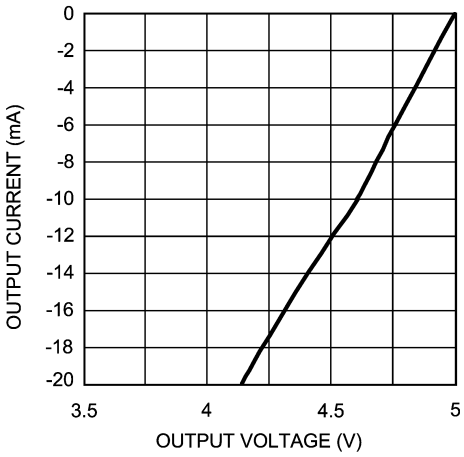
Receiver Output High Voltage vs. Output Current



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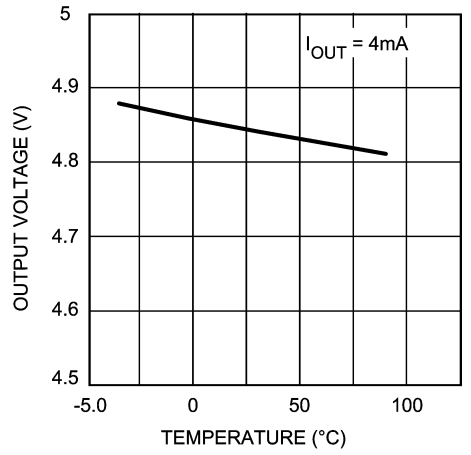
Receiver Output High Voltage vs. Temperature



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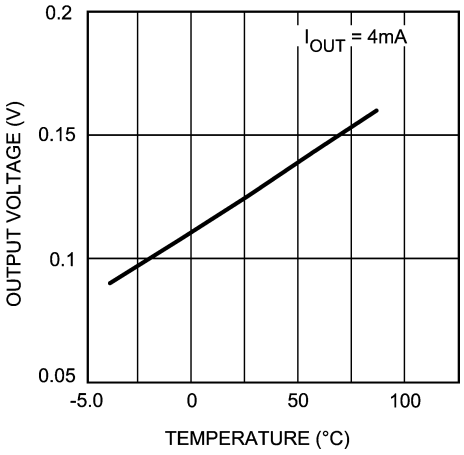
Receiver Output Low Voltage vs. Temperature



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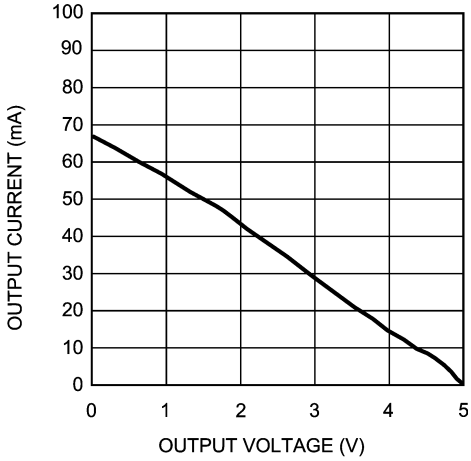
Driver Differential Output Voltage vs. Output Current



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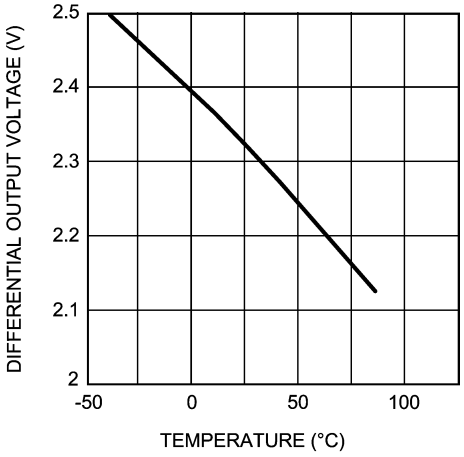
Driver Differential Output Voltage vs. Temperature
R_L = 54Ω



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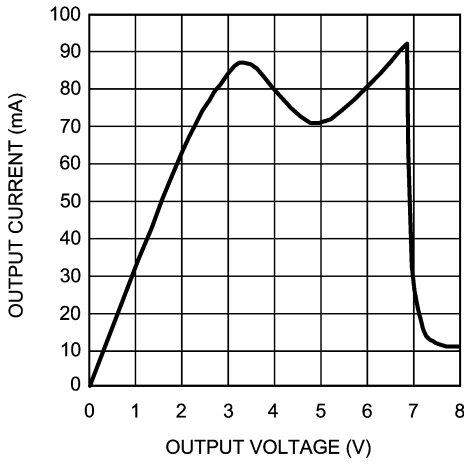
Typical Performance Characteristics (Continued)

Driver Output Low Voltage vs. Output Current



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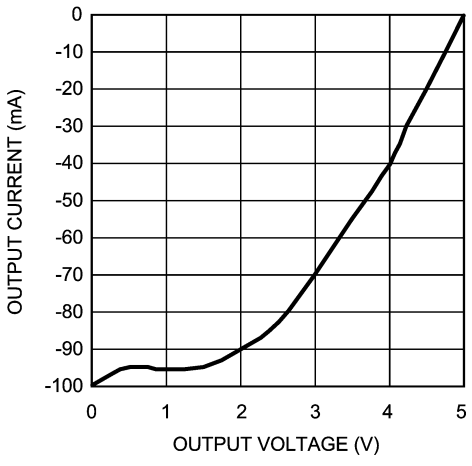
Driver Output High Voltage vs. Output Current



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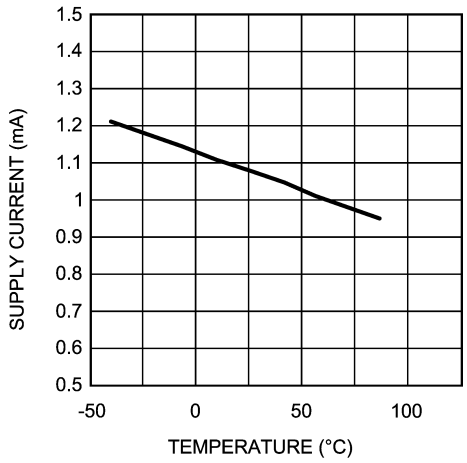
Supply Current vs. Temperature



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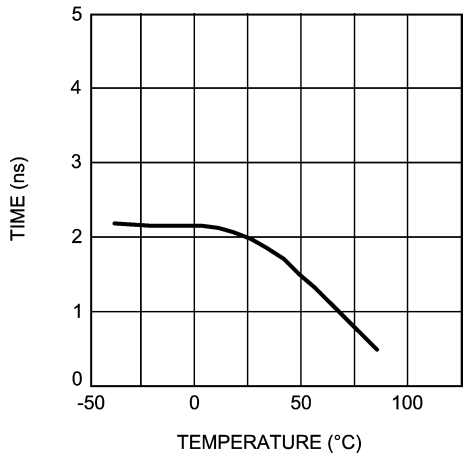
Receiver Skew vs. Temperature



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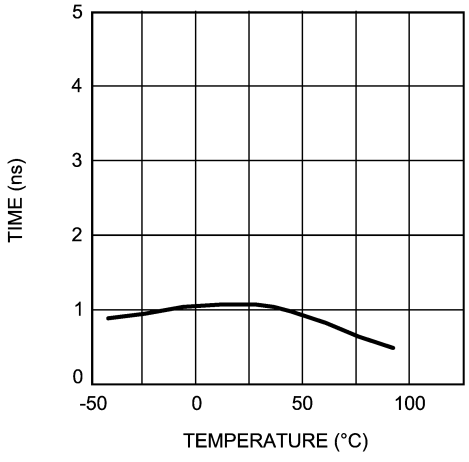
Driver Skew vs. Temperature



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Parameter Measuring Information

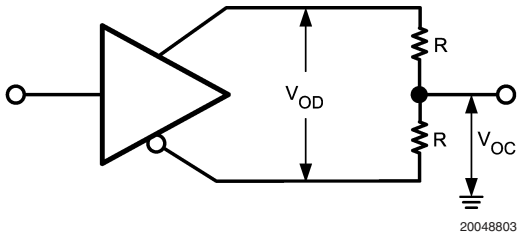


FIGURE 1. Test Circuit for V_{OD} and V_{OC}

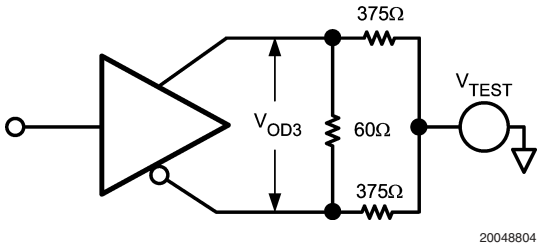


FIGURE 2. Test Circuit for V_{OD3}

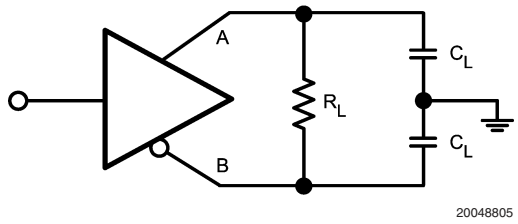


FIGURE 3. Test Circuit for Driver Propagation Delay

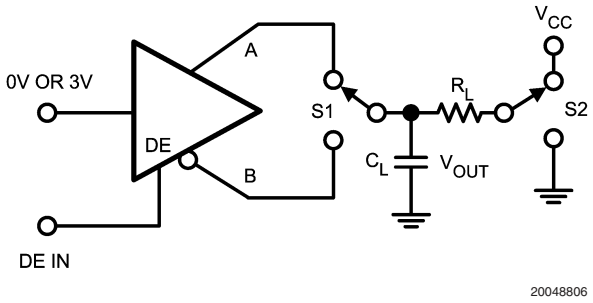


FIGURE 4. Test Circuit for Driver Enable / Disable

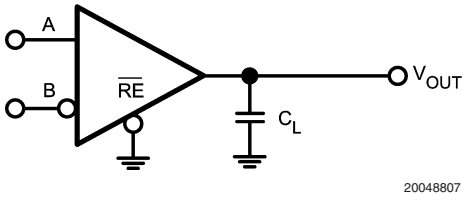


FIGURE 5. Test Circuit for Receiver Propagation Delay

Parameter Measuring Information (Continued)

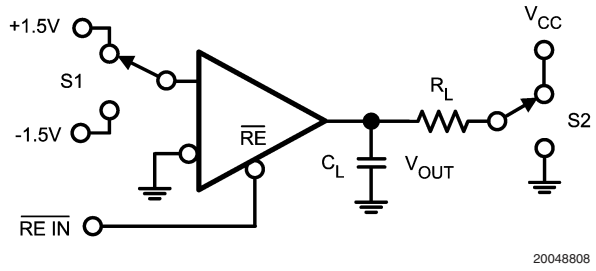


FIGURE 6. Test Circuit for Receiver Enable / Disable

Switching Characteristics

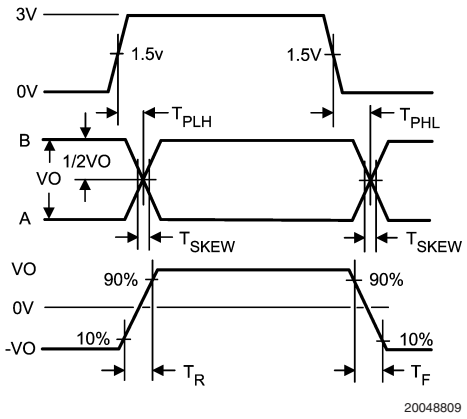


FIGURE 7. Driver Propagation Delay, Rise / Fall Time

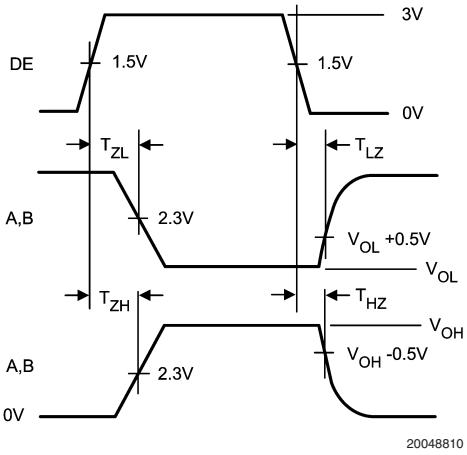


FIGURE 8. Driver Enable / Disable Time

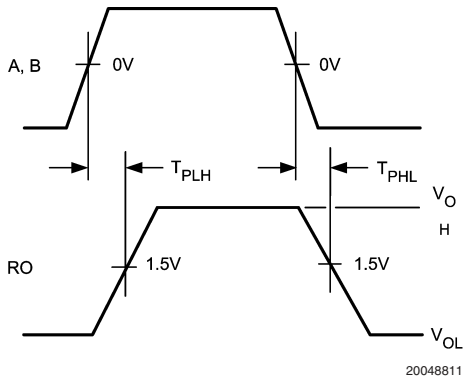


FIGURE 9. Receiver Propagation Delay

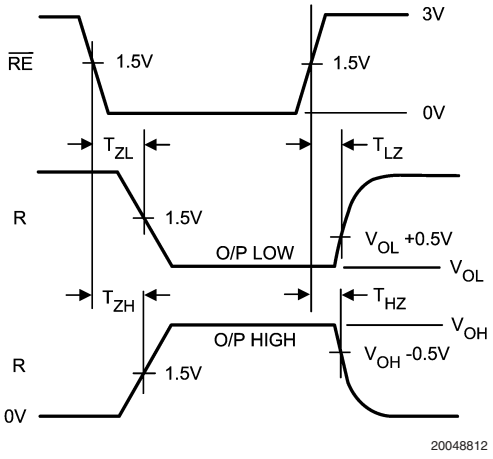


FIGURE 10. Receiver Enable / Disable Time

Application Information

POWER LINE NOISE FILTERING

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as 10µF, between the power supply pin and ground to filter out low frequencies and a 0.1µF to filter out high frequencies.

By pass-capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

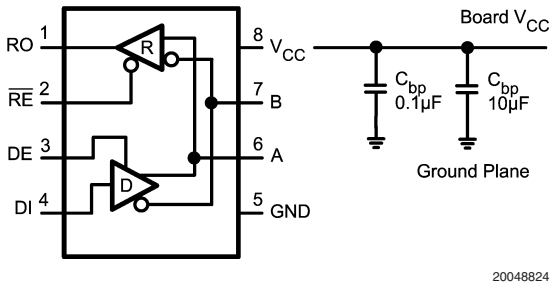
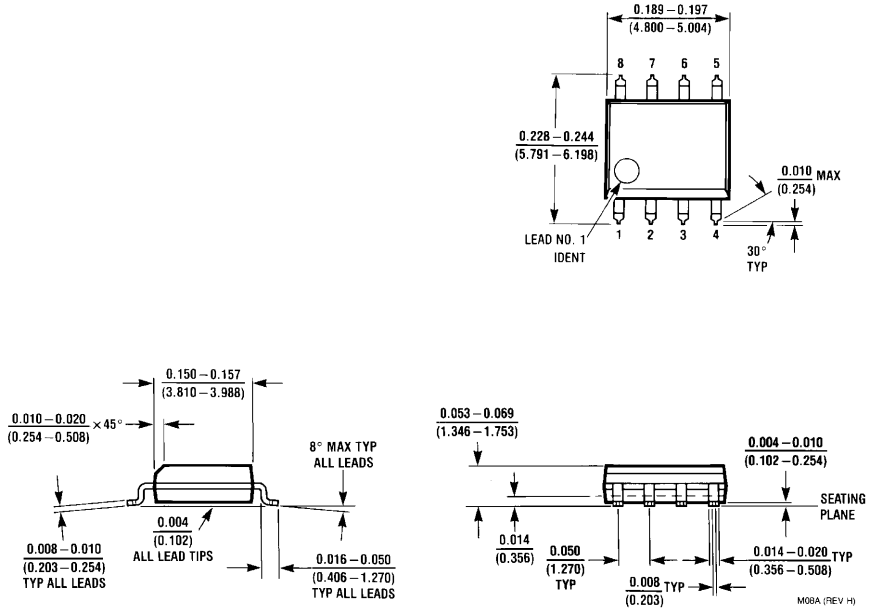


FIGURE 11. Placement of by-pass Capacitors, C_{bp}

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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