picoPACK™ LCD Display Controller Interface

Introduction

The LCD Display Controller Interface is a synthesizable intellectual property block that provides a port to typical LCD display controllers. In addition, the module can evaluate input signals switched by keys or buttons for display control purposes. The module is part of the picoPACK IP series from picoTurbo, Inc.

Features

- 32 bit APB bus
- LCD Display Controller Interface
    - support of HD44780 compatible LCD display controllers
    - 4 and 8 bit interface
    - automatic busy state polling
    - configurable timing
- Input Key Interface
    - 4 input key lines
    - key long press mode
    - auto repeat mode
    - configurable timings
- Configuration options
- Targeted at gate array and standard cell technologies
- Equivalent NAND2 gate count ≈ 7.8K

Applications

- Mobile applications
- High performance multi CPU controllers
- Low cost single chip controllers

Architecture
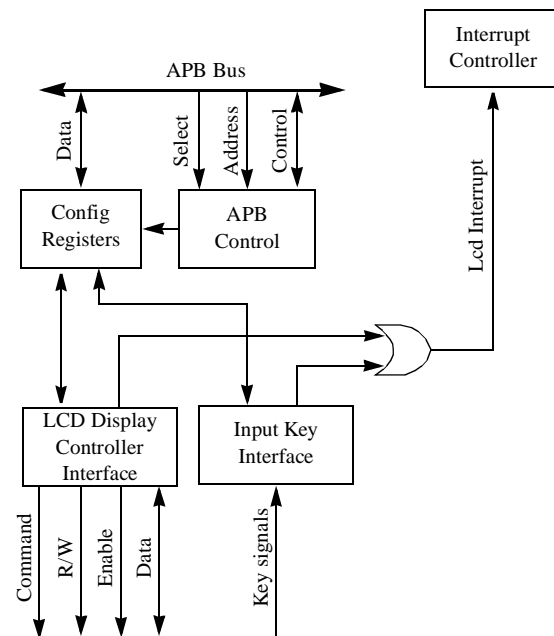
Interface Ports

- 32 bit APB bus interface
- HD44780 compatible LCD Display Controllers

Bus Support

- AMBA™ 2.0

Functional Description

The LCD device consists of a LCD display controller interface for HD44780 compatible devices and a input key interface.

LCD display controller interface

The actual LCD Display Controller Interface polls the display controller until it is no longer in a busy state and writes commands/data to or reads commands/data from the display controller.

Input Key Interface

The Input Key Interface generates interrupts when key press activity is detected. Hereby the key press signal is debounced. The generated interrupt sequence depends on which mode (normal, longpress, autorepeat) is activated.

The LCD is a little endian device. Please refer to the AMBA2.0 specification for further details.
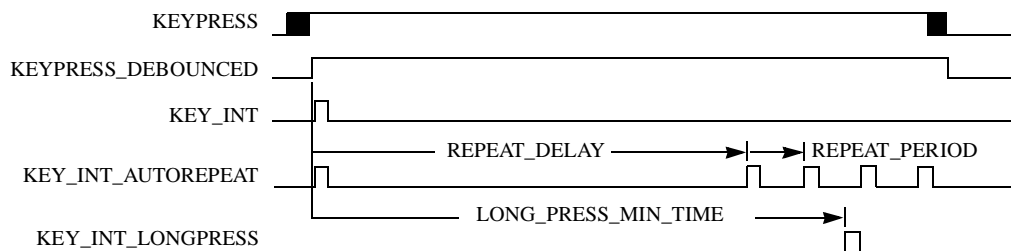
Deliverables

- Fully synthesizable VHDL-RTL source code
- Fully synthesizable VERILOG-RTL source code
- Synopsys synthesis scripts
- Testbench with functional test vectors
- User documentation

Operating Conditions

For the minimum clock speed there is no limitation due to fully static design. The maximum clock speed depends on target technology and constraining. Therefore any clock frequency from 0 MHz to the actual maximum frequency may be chosen for safe operation.

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