Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU3X312FTR
12-Port Transceiver for 10Base-T/100Base-TX/FX

Overview

The LU3X312FTR is an twelve-channel, single-chip complete transceiver designed specifically for dual-speed 10Base-T, 100Base-TX, and 100Base-FX switches and repeaters. It supports simultaneous operation in three separate *IEEE** standard modes: 10Base-T, 100Base-TX, and 100Base-FX. The LU3X312FTR uses 0.25 µm low-power CMOS to achieve extremely low power dissipation and operates from a single 3.3 V power supply.

Each channel implements the following:

- 10Base-T transceiver function of *IEEE* 802.3.
- 100Base-TX transceiver function of *IEEE* 802.3u.
- 100Base-FX transceiver function of *IEEE* 802.3u.
- Autonegotiation of *IEEE* 802.3u.
- MII management of *IEEE* 802.3u.

The LU3X312FTR supports operations over two pairs of unshielded twisted-pair (UTP) cable (10Base-T and 100Base-TX) and over fiber-optic cable (100Base-FX).

It has been designed with a flexible system interface that allows configuration for optimum performance and effortless design. The individual per-port system interface can be configured as 10 Mbits/s or 100 Mbits/s reduced MII (RMII) or 10 Mbits/s or 100 Mbits/s serial MII (SMII).

Features

10 Mbits/s Transceiver

- Compatible with *IEEE* 802.3 10Base-T standard for category 3 unshielded twisted-pair (UTP) cable.
- Compatible with the reduced MII (RMII) specification of the RMII consortium version 1.2.
- Selectable 6-pin RMII or 2-pin serial MII (SMII).
- Autopolarity detection and correction.
- Adjustable squelch level for extended line length capability (two levels).
- On-chip filtering eliminates the need for external filters.
- Half- and full-duplex operations.

100 Mbits/s TX Transceiver

- Compatible with *IEEE* 802.3u PCS (clause 23), PMA (clause 24), autonegotiation (clause 28), and PMD (clause 25) specifications.
- Compatible with the reduced MII (RMII) specification of the RMII consortium version 1.2.
- Selectable 6-pin RMII, 2-pin MII (serial MII).
- Scrambler/descrambler bypass.
- Selectable carrier sense signal generation (CRS) asserted during either transmission or reception in half duplex (CRS asserted during reception only in full duplex).
- Full- or half-duplex operations.
- On-chip filtering and adaptive equalization that eliminates the need for external filters.

100 Mbits/s FX Transceiver

- Pseudo-ECL compatible input/output for 100Base-FX support (with fiber-optic signal detect).
- Compatible with *IEEE* 802.3u 100Base-FX standard.
- Uses existing twisted-pair I/O pins for compatible fiber-optic transceiver pseudo-ECL (PECL) data:
  - — No additional data pins required.
  - — Uses existing LU3X312FTR pins for fiber-optic signal detect (FOSD) inputs.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Features (continued)

- Fiber mode automatically configures port:
  — Disables autonegotiation.
  — Disables 10Base-T.
  — Enables 100Base-FX far-end fault signaling.
  — Disables MLT-3 encoder/decoder.
  — Disables scrambler/descrambler.
- FX mode enable is pin- or register-selectable on an individual per-port basis.

General

- Low power dissipation (<0.4 W per port).
- Autonegotiation (*IEEE* 802.3u, clause 28):
  — Fast link pulse (FLP) burst generator.
  — Arbitration function.
- Supports the station management protocol and frame format (clause 22):
  — Basic and extended registers.
  — Support next page mode.
  — Accepts preamble suppression.
  — Maskable status interrupts.
  — Up to 12.5 MHz MDC clock rate.
- Supports the following management functions via pins if MII station management is unavailable:
  — Speed select.
  — Scrambler/descrambler bypass.
  — Full duplex.
  — No link pulse mode.
  — Carrier sense select.
  — Autonegotiation.
  — FX mode select.
- 50 MHz/125 MHz clock input in RMII and SMII modes, respectively.
- Supports half- and full-duplex operations.
- Provides four LED status signals:
  — Activity (transmit or receive). Optional LED blink mode (500 ms on, 500 ms off or 2.5 s on, 2.5 s off) or pulse stretch mode (40 ms—80 ms).
  — Full duplex.
  — Link integrity.
  — Speed indication.
- Serial LED output stream for additional status monitoring.
- Bicolor LED mode.
- LED drivers on-chip (8 mA—10 mA). Drivers can be turned off when LED is not used (power saving).
- Per-channel powerdown mode for 10 Mbits/s and 100 Mbits/s operation.
- Loopback for 10 Mbits/s and 100 Mbits/s operation.
- Internal pull-up or pull-down resistors to set default configuration during powerup.
- 0.25 μm low-power CMOS technology.
- 352-pin PBGA package.
- JTAG boundary scan.
- Single 3.3 V power supply.

Description

RMII Mode

The reduced media independent interface (RMII) is a low pin count interface specification promulgated by the RMII consortium. This specification reduces the total number of pins from 16 for the *IEEE* 802.3u MII interface to six for the RMII. Architecturally, the RMII specification provides for an additional reconciliation sublayer on either side of the MII but, in the LU3X312FTR, has been implemented in the absence of the MII.

The management interface (MDIO/MDC) remains identical to that defined in *IEEE* 802.3u.

The RMII specification has the following characteristics:

- It supports 10 Mbits/s and 100 Mbits/s data rates.
- 50 MHz clock references are sourced from MAC to PHY or from an external shared source.
- It provides independent 2-bit wide transmit and receive data paths.

SMII Mode

The serial media independent interface (SMII) is a low pin count interface specification promulgated by *Cisco**. This specification reduces the total number of pins from 16 for the *IEEE* 802.3u MII interface to two for the SMII. Architecturally, the SMII specification provides for an additional reconciliation sublayer on either side of the MII but, in the LU3X312FTR, has been implemented in the absence of the MII.

The management interface (MDIO/MDC) remains identical to that defined in *IEEE* 802.3u.

The SMII specification has the following characteristics:

- It supports 10 Mbits/s and 100 Mbits/s data rates.
- 125 MHz clock references are sourced from MAC to PHY or from an external shared source.
- It provides independent serial transmit and receive data paths.

LED Control

LEDs can be accessed in one of the following modes:

- Serial mode. In this mode, all of the LEDs are time-division multiplexed onto one pin, with a second pin acting as the clock and a third as a strobe. All LEDs and all channels share the same pins.
- Parallel mode. In this mode, each LED and each channel has its own pin. There is a total of four LED pins per channel for a total of 32 pins.
- Bicolor mode. In this mode, each channel has two outputs to control a bicolor LED. One LED can be used for each port, indicating link and activity.

In all modes, the LEDs can be operated as follows:

- LED stretch
- LED blink
- No stretch or blink

Clocking

The LU3X312FTR operates with a 50 MHz clock input when in the RMII mode, and with a 125 MHz clock input when in the SMII mode.

FX Mode

Each individual port of the LU3X312FTR can be operated in 100Base-FX mode by selecting it through the pin program option (FX_MODE_EN[11:0]), or through the register bit (register 29, bit 0).

When operating in FX mode, the twisted-pair I/O pins are reused as the fiber-optic transceiver I/O data pins, and the fiber-optic signal detect (FOSD) inputs are enabled.

When a port is placed in FX mode, it will automatically configure the port for 100Base-FX operation (and the register bit control will be ignored) such that:

- The far-end fault signaling option will be enabled.
- The MLT-3 encoding/decoding will be disabled.
- Scrambler/descrambler will be disabled.
- Autonegotiation will be disabled.
- The signal detect inputs will be activated.
- 10Base-T will be disabled.

* *Cisco* is a registered trademark of Cisco Systems.

Functional Description

Block Diagrams

Single-Channel Twisted-Pair Interface

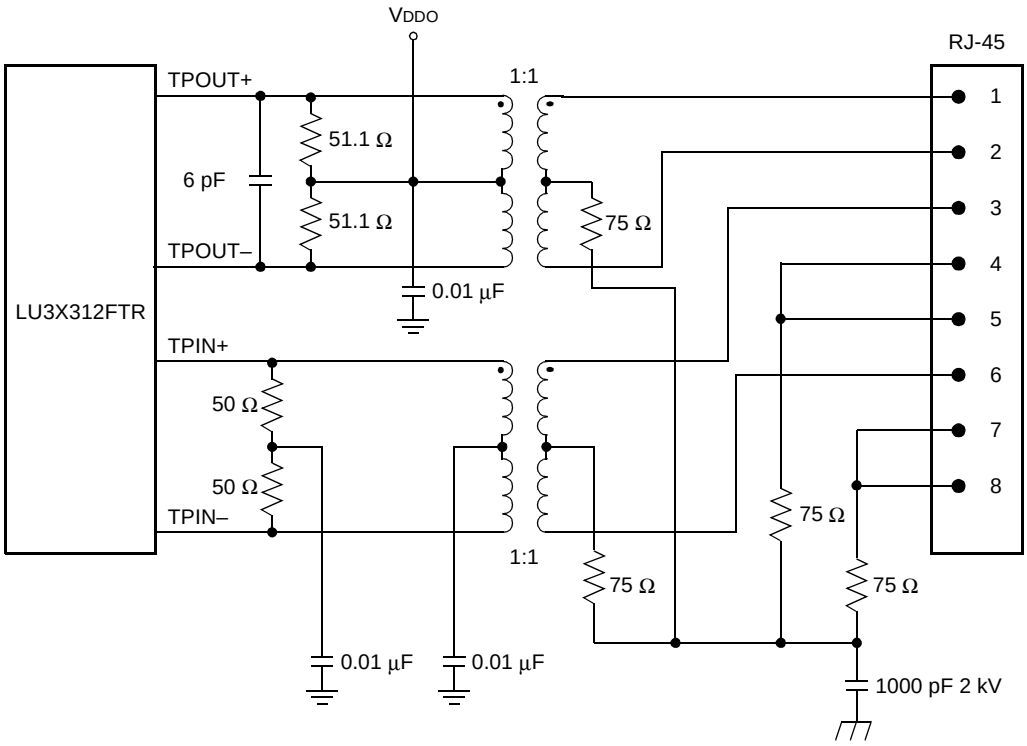


Figure 1. Typical Single-Channel Twisted-Pair (TP) Interface

Functional Description (continued)

Single-Channel Detail Functions

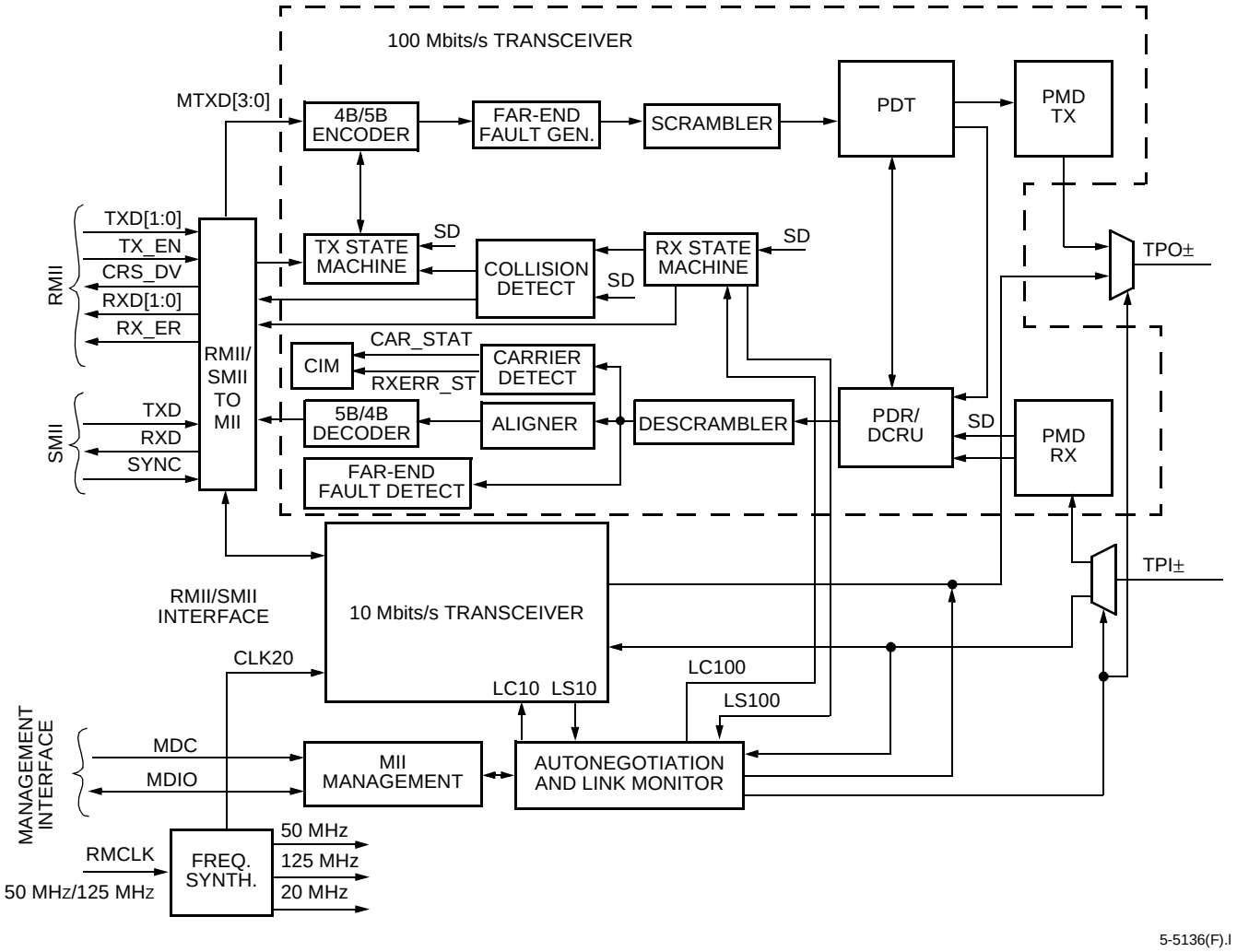


Figure 2. LU3X312FTR Single-Channel Detail Functions

Functional Description (continued)

Device Overview

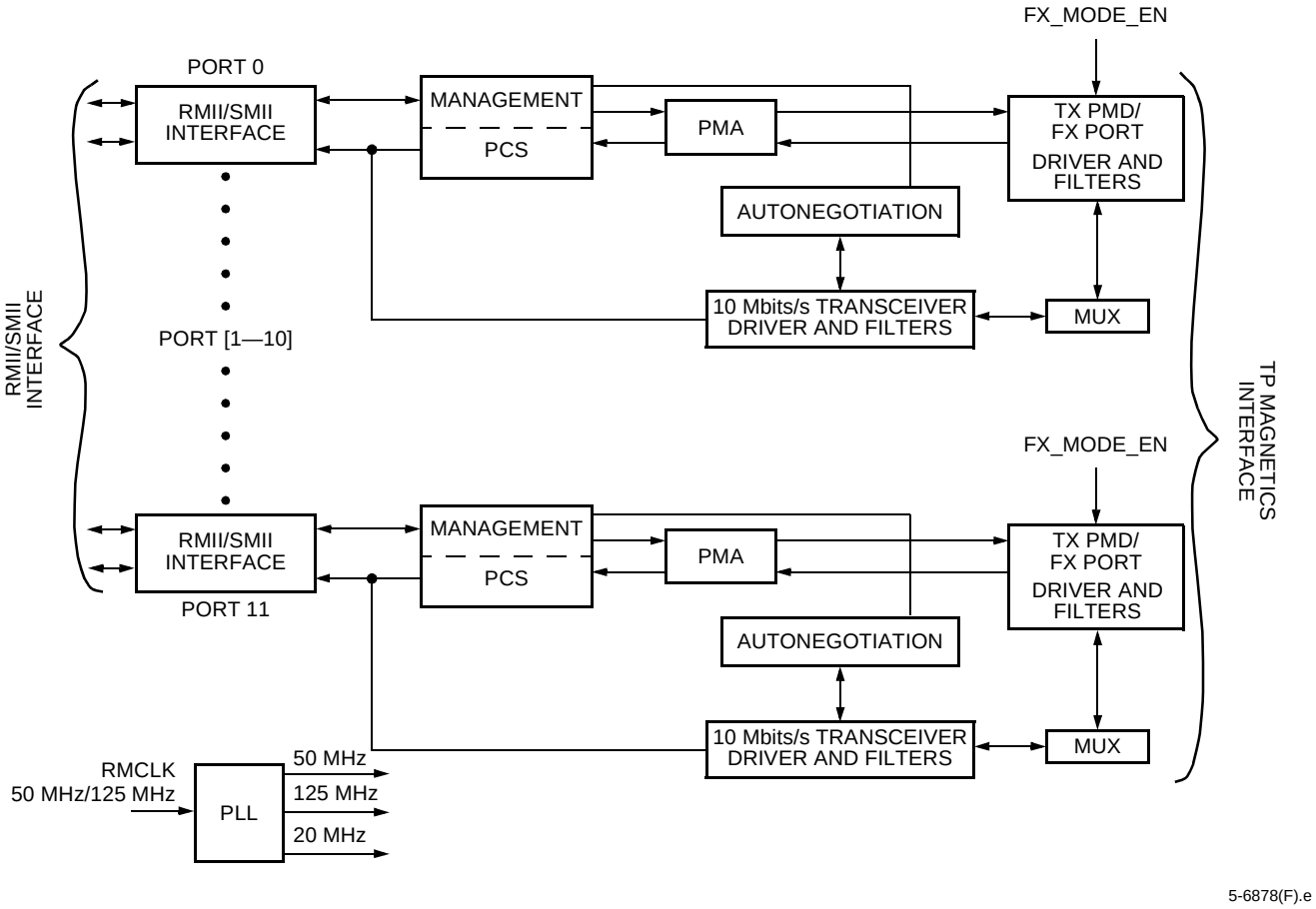
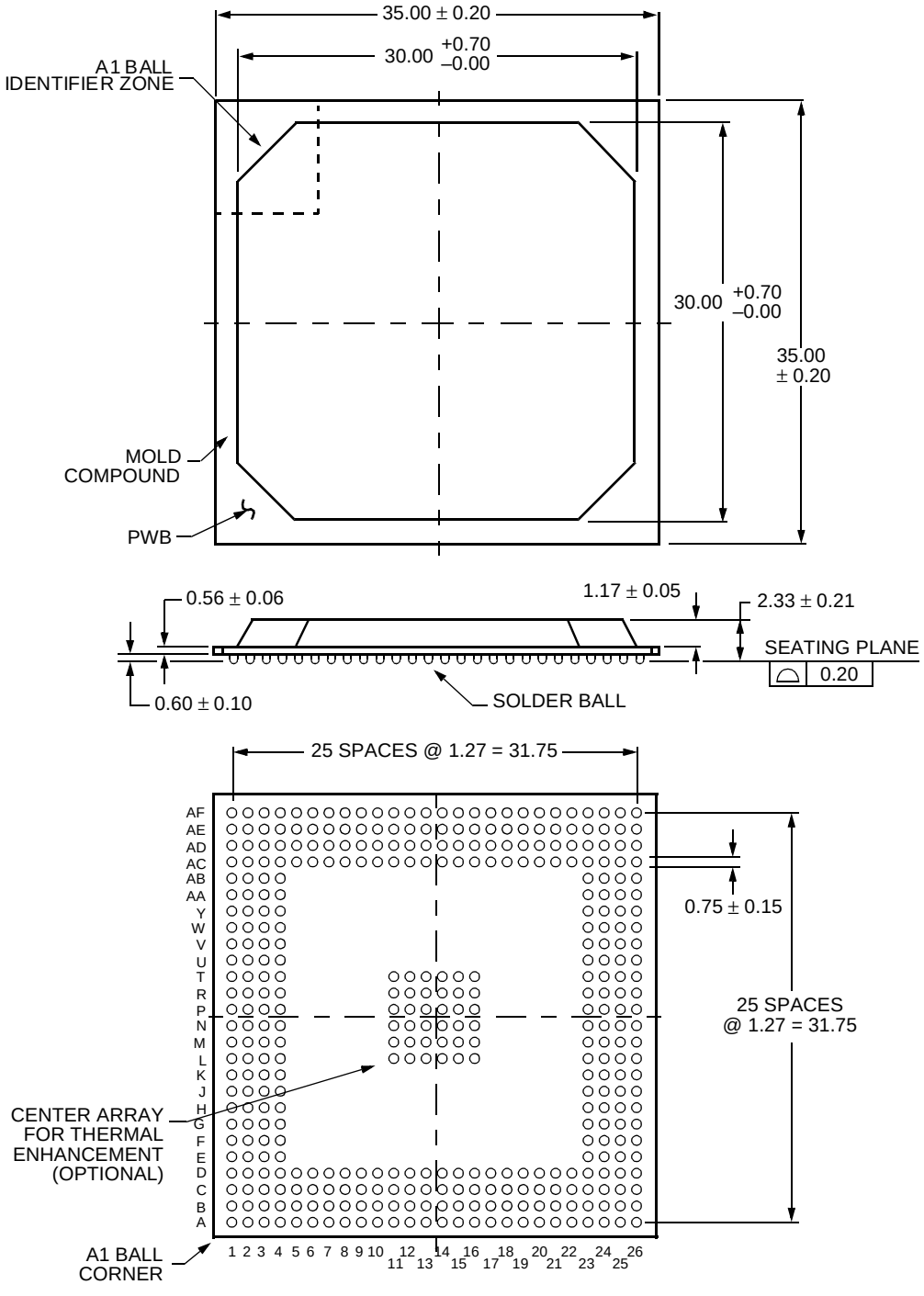


Figure 3. LU3X312FTR Device Overview

Outline Diagram

352-Pin PBGA

Dimensions are in millimeters.



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Note: Although the 36 thermal enhancement balls are stated as an option, they are standard on the 352 PBGA package.

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