Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU3X36FTR
HEX-FET (Fast Ethernet Transceiver) for 10Base-T/100Base-TX/FX

Overview

The LU3X36FTR is a six-channel, single-chip complete transceiver designed specifically for dual-speed 10Base-T, 100Base-TX, and 100Base-FX switches and repeaters. It supports simultaneous operation in three separate *IEEE** standard modes: 10Base-T, 100Base-TX, and 100Base-FX. The LU3X36FTR uses 0.25 µm low-power CMOS to achieve extremely low power dissipation and operates from a single 3.3 V power supply.

Each channel implements the following:

- 10Base-T transceiver function of *IEEE* 802.3.
- 100Base-TX transceiver function of *IEEE* 802.3u.
- 100Base-FX transceiver function of *IEEE* 802.3u.
- Autonegotiation of *IEEE* 802.3u.
- MII management of *IEEE* 802.3u.

The LU3X36FTR supports operations over two pairs of unshielded twisted-pair (UTP) cable (10Base-T and 100Base-TX) and over fiber-optic cable (100Base-FX).

It has been designed with a flexible system interface that allows configuration for optimum performance and effortless design. The individual per-port system interface can be configured as 10 Mbits/s or 100 Mbits/s reduced MII (RMII) or 10 Mbits/s or 100 Mbits/s serial MII (SMII).

Features

10 Mbits/s Transceiver

- Compatible with *IEEE* 802.3 10Base-T standard for category 3 unshielded twisted-pair (UTP) cable.
- Compatible with the reduced MII (RMII) specification of the RMII consortium version 1.2.
- Selectable 6-pin RMII or 2-pin Serial MII (SMII).
- Autopolarity detection and correction.
- Adjustable squelch level for extended line length capability (two levels).
- On-chip filtering eliminates the need for external filters.
- Half- and full-duplex operations.

100 Mbits/s TX Transceiver

- Compatible with *IEEE* 802.3u PCS (clause 23), PMA (clause 24), autonegotiation (clause 28), and PMD (clause 25) specifications.
- Compatible with the reduced MII (RMII) specification of the RMII consortium version 1.2.
- Selectable 6-pin RMII, 2-pin MII (serial MII).
- Scrambler/descrambler bypass.
- Selectable carrier sense signal generation (CRS) asserted during either transmission or reception in half duplex (CRS asserted during reception only in full duplex).
- Full- or half-duplex operations.
- On-chip filtering and adaptive equalization that eliminates the need for external filters.

100 Mbits/s FX Transceiver

- Pseudo-ECL compatible input/output for 100Base-FX support (with fiber-optic signal detect).
- Compatible with *IEEE* 802.3U 100Base-FX standard.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

Features (continued)

- Reuses existing twisted-pair I/O pins for compatible fiber-optic transceiver pseudo-ECL (PECL) data:
  — No additional data pins required.
  — Reuses existing LU3X36FTR pins for fiber-optic signal detect (FOSD) inputs.
- Fiber mode automatically configures port:
  — Disables autonegotiation.
  — Disables 10Base-T.
  — Enables 100Base-FX remote fault signaling.
  — Disables MLT-3 encoder/decoder.
  — Disables scrambler/descrambler.
- FX mode enable is pin- or register-selectable on an individual per-port basis.

General

- Low power dissipation (<0.4 W per port).
- Autonegotiation (*IEEE* 802.3u, clause 28):
  — Fast link pulse (FLP) burst generator.
  — Arbitration function.
- Supports the station management protocol and frame format (clause 22):
  — Basic and extended registers.
  — Support next page mode.
  — Accepts preamble suppression.
  — Maskable status interrupts.
  — 12.5 MHz MDC clock rate.
- Supports the following management functions via pins if MII station management is unavailable:
  — Speed select.
  — Scrambler/descrambler bypass.
  — Full duplex.
  — No link pulse mode.
  — Carrier sense select.
  — Autonegotiation.
  — FX mode select.
- Single 50 MHz/125 MHz clock input in RMII and SMII modes, respectively.
- Supports half- and full-duplex operations.
- Provides four LED status signals:
  — Activity (transmit or receive). Optional LED blink mode (500 ms on, 500 ms off or 2.5 s on, 2.5 s off) or pulse stretch mode (40 ms—80 ms).
  — Full duplex.
  — Link integrity.
  — Speed indication.
- Serial LED output stream for additional status monitoring.
- Bicolor LED mode.
- LED drivers on-chip (8 mA—10 mA). Drivers can be turned off when LED is not used (power saving).
- Per-channel powerdown mode for 10 Mbits/s and 100 Mbits/s operation.
- Loopback for 10 Mbits/s and 100 Mbits/s operation.
- Internal pull-up or pull-down resistors to set default configuration during powerup.
- 0.25 µm low-power CMOS technology.
- 272-pin PBGA.
- JTAG boundary scan.
- Single 3.3 V power supply.

Functional Description

Functional Block Diagrams

Single-Channel Twisted-Pair Interface

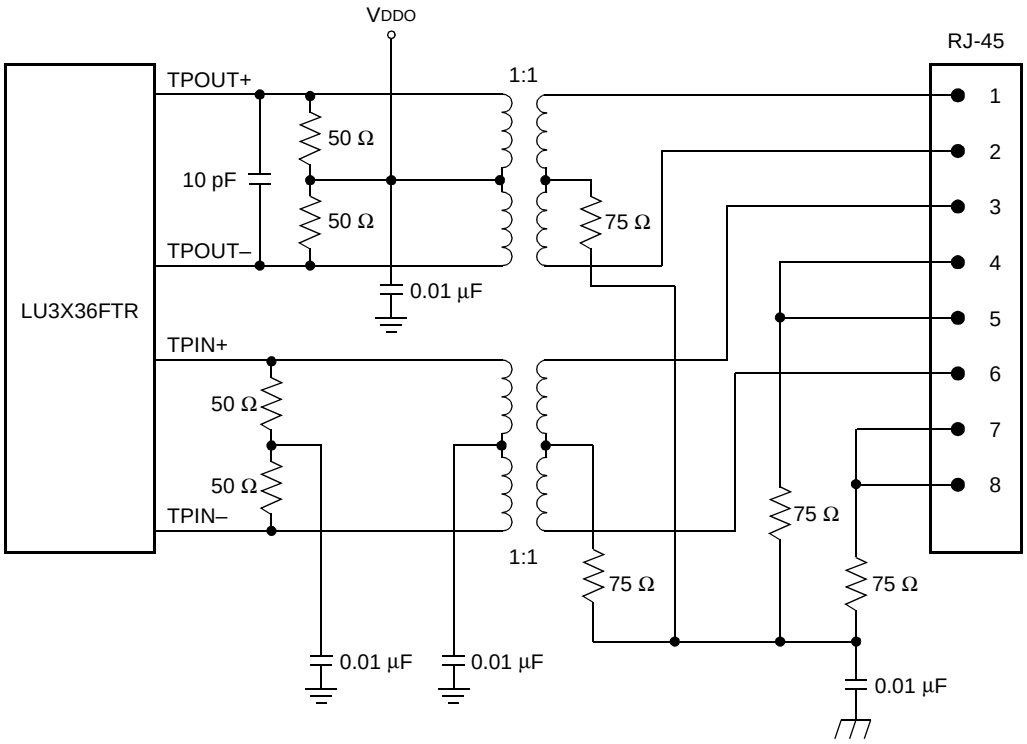

Figure 1. Typical Single-Channel Twisted-Pair (TP) Interface

Functional Description (continued)

Single-Channel Detail Functions

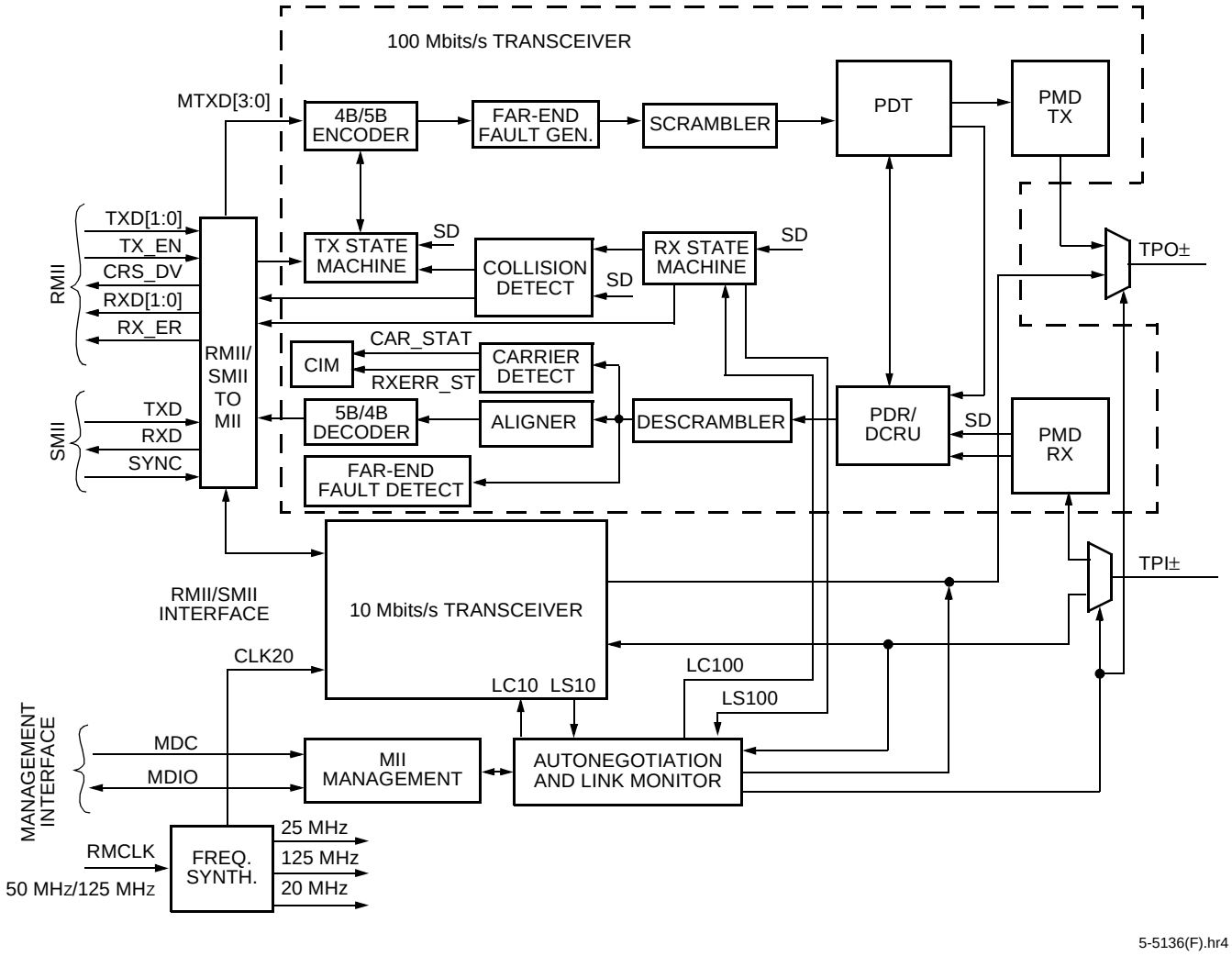

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Figure 2. LU3X36FTR Single-Channel Detail Functions

Functional Description (continued)

Device Overview

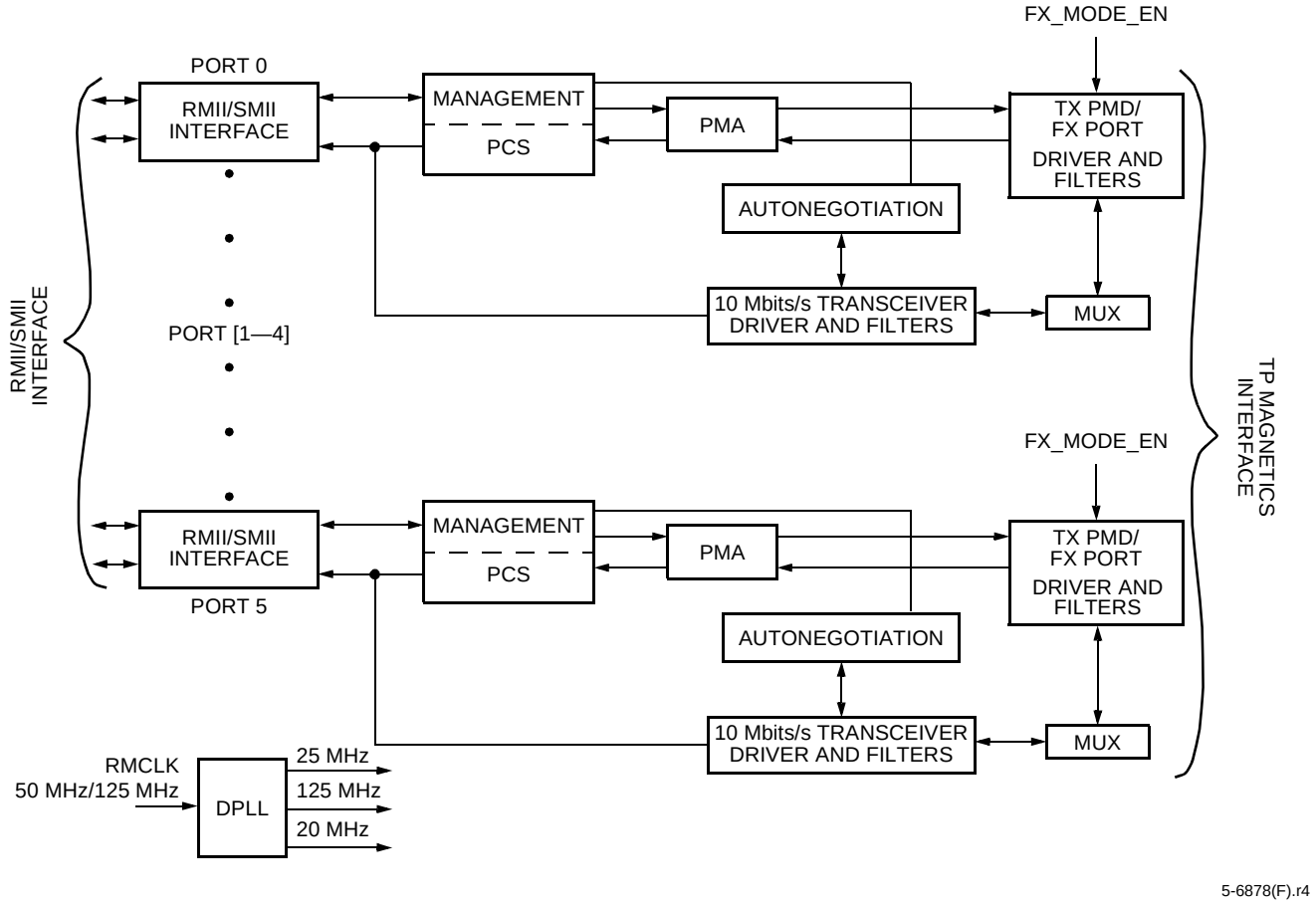

Figure 3. LU3X36FTR Device Overview

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