LXT973 Twisted-Pair-to-Fiber Media Converter Board

Application Note

November 2001

For technical assistance on this product, please call 1-800-628-8686
or send an e-mail to support@mailbox.intel.com.

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Contents

Figures

Tables

1.0 General Description

LXT973 is an ideal building block for systems that require two Ethernet ports, such as Internet Protocol (IP) Telephones, Twisted-Pair (TX)-to-Fiber (FX) converter modules, and telecommunications applications, such as Telecom Central Office (TCO) and Customer Premise Equipment (CPE) devices.

LXT973 is an IEEE-compliant, 2-port, Fast Ethernet PHY transceiver that directly supports both 100BASE-TX and 10BASE-T applications. The device also provides a pseudo-ECL (PECL) interface per port for use with 100BASE-FX fiber networks. The device's fiber ports are designed to connect to common industry-standard, fiber modules, incorporating ECL receivers and drivers and allowing for seamless integration.

LXT973 also incorporates auto MDIX, allowing the device to automatically switch the twisted-pair inputs and outputs. This feature eliminates the concern of common networking connection problems where straight-through and cross cable are used.

1.1 Board Features

- Two IEEE 802.3 compliant ports
  - 100BASE-TX
  - 100BASE-FX
- Minimum configuration required
- Single 3.3V power supply
- Auto MDIX on the 100BASE-TX port
- Three configurable LEDs for status display

2.0 Introduction

The LXT973 twisted pair-to-fiber media converter board block diagram (shown in Figure 1) demonstrates the ease of implementing the LXT973 dual-port PHY in a media converter design. Each port provides a Media Independent Interface (MII) normally connected to a Media Access Controller (MAC). This design uses an Altera FPGA between two MII ports to account for the different clock frequencies that may exist in bi-directional data. Please refer to Section 3.2, "About the Board" on page 8 for information on the FPGA.

Figure 1. LXT973 Twisted-Pair-to-Fiber Media Converter Board

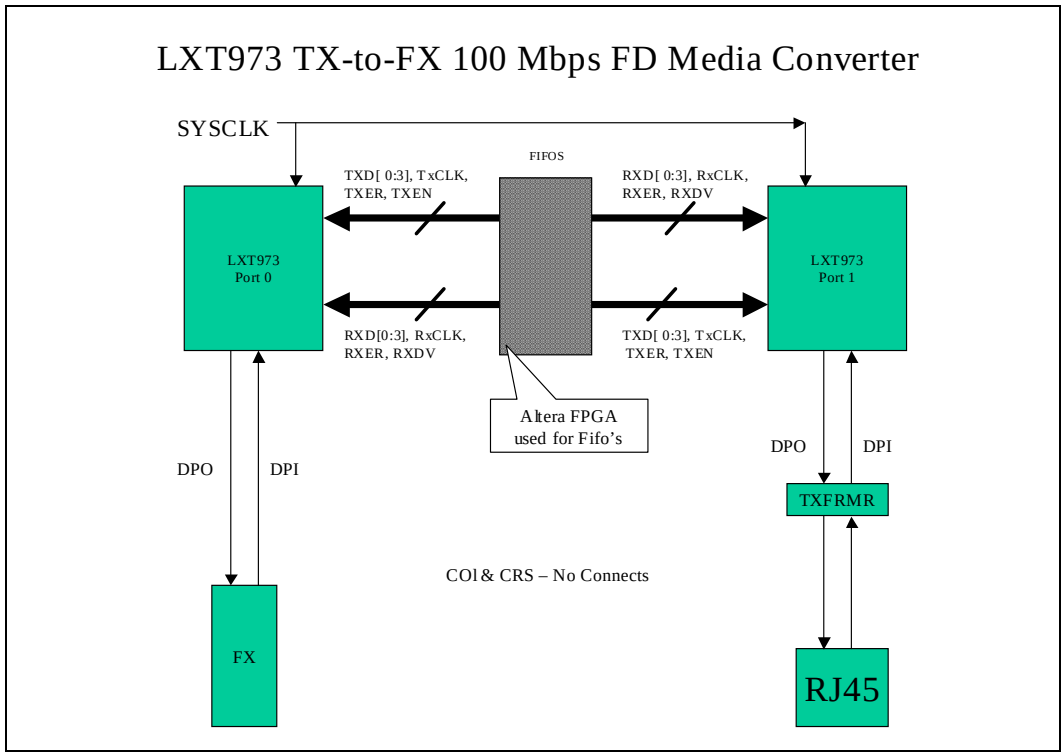


Figure 2 on page 7 shows a topological view of the media converter board. In this design, the LXT973 twisted-pair port may be configured in half-duplex mode for testing purposes via Header 1 on JP1. The default setting is full-duplex when Header 1 on JP1 is jumpered. When the jumper is removed from Header 1 and the board is reset by depressing S1, the twisted-pair port is configured for half-duplex operation.

Headers 2 and 3 on JP1 are used to configure the LXT973 LEDs for different display options. Please refer to the printed table on the converter board for different configuration modes and Table 1 on page 7 for default settings.

Figure 2. LXT973 TX-to-FX 100 Mbps FD Media Converter (Top View)

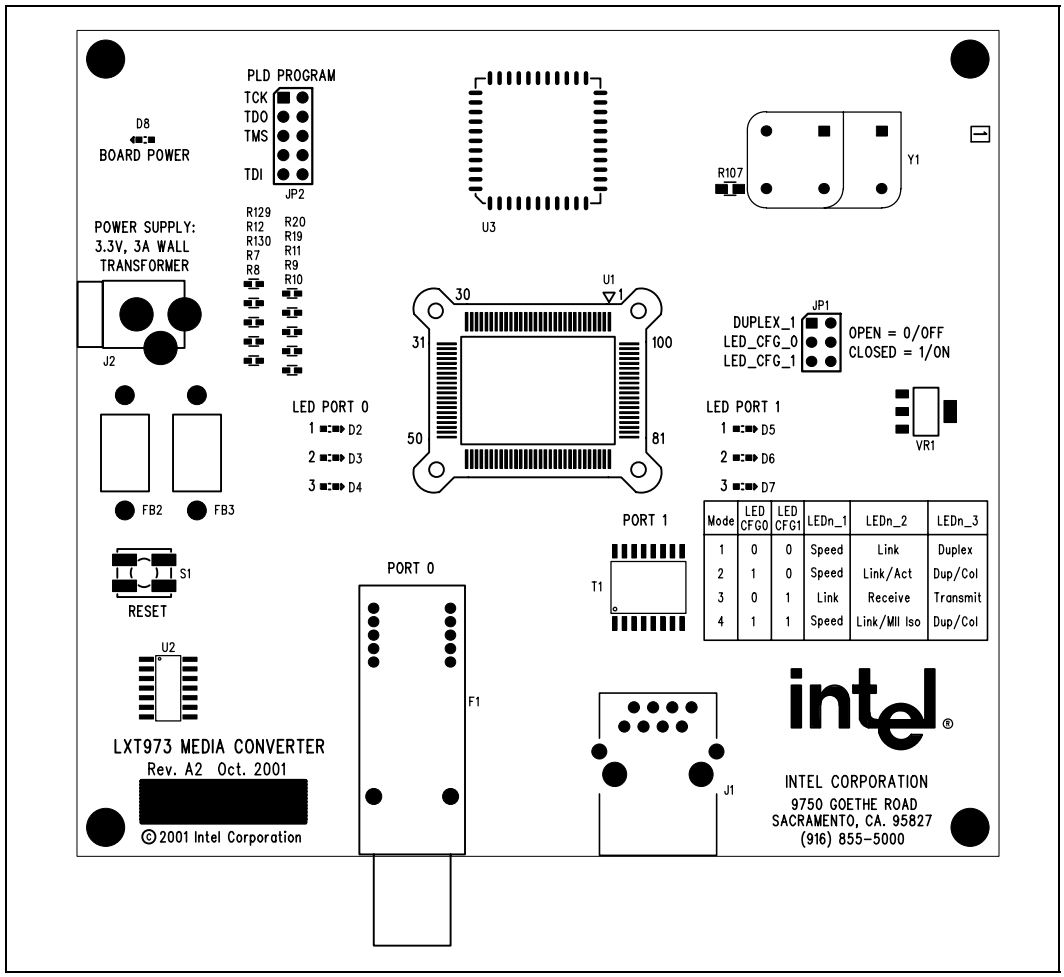


Table 1 provides the configurations for the LXT973 jumpers.

Table 1. LXT973 Jumper Configurations

Jumper	Label	Setting	Configuration
JP1	DUPLEX_1	Header 1 = Jumpered (**Default**)	Enables full-duplex
		Header 1 = Open	Enables half-duplex
	LED_CFG_0	Header 2 = Jumpered	LED_CFG_0 = 1 (High)
		Header 2 = Open (**Default**)	LED_CFG_0 = 0 (Low)
	LED_CFG_1	Header 3 = Jumpered	LED_CFG_1 = 1 (High)
		Header 3 = Open (**Default**)	LED_CFG_1 = 0 (Low)
JP2	PLD Program	Open	N/A

3.0 Twisted-Pair-to-Fiber Converters

3.1 General Operation

The following steps should be followed for proper board operation:

- Connect the power supply to the board power-plug
- Set jumpers on JP1 as desired
- Jumper pins 1 and 2 on JP1 for full-duplex operation (recommended) - default
- Do not jumper Pins 3 through 6 (for LED Mode – 1) - default
- Plug in the power supply to a 110 volt wall outlet
- Reset the board by depressing switch S1
- Connect link partners with a twisted-pair cable to the RJ-45 connector (J1), and a fiber optic cable to the fiber transceiver (F1)
- Proceed with the evaluation

The board is designed for use in 100 Mbps full-duplex operation only and the fiber side of the board operates in full-duplex mode only. The twisted-pair side of the board can be operated in half-duplex mode for evaluation purposes. Remove the jumper from pins 1 and 2 of JP1, and reset the board by depressing switch S1, for half-duplex operation.

Note: Operating the fiber side in full-duplex mode and the twisted-pair side in half-duplex mode causes collisions and packet loss if both sides are trying to transmit and receive at the same time.

Pins 3&4 and 5&6 of JP1 are used to set the modes for the programmable LED display. The LEDs on the twisted-pair side are user configurable for four different modes of status display. The LEDs on the fiber side are set for Mode 1 only.

3.2 About the Board

The LXT973 media converter board uses the Intel LXT973 dual-port physical layer device in a twisted-pair (copper)-to-fiber media conversion application for IEEE 802.3 Ethernet applications. The LXT973 dual-port chip (one port configured for 100BASE-TX and the other port configured for 100BASE-FX) does not require any software or controller to transmit and receive data. The data received on the twisted-pair side is looped out of Port 1 and into Port 0 (the fiber port) through the MII signals, thus using the dual-port LXT973 as a media converter device. A small buffer is required for each data direction. The transmit and receive clocks on the MII are both sourced by the PHY, thus the data flowing from one MII port to the other must be synchronized through a FIFO. The FPGA requires two 3x6 bit FIFOs between Port 1 and Port 0. The parameters used to calculate the FIFO depth are as follows:

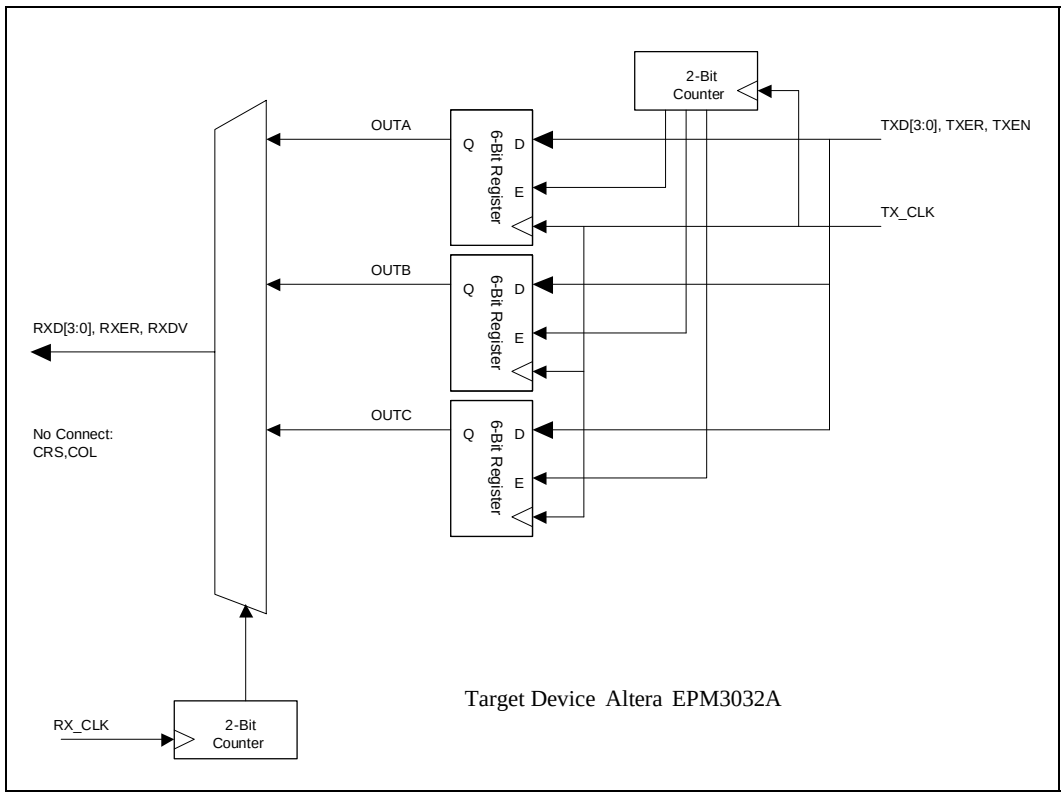
- The MII clock is 25 MHz with a specification of +/-100 ppm.
- The maximum packet size is 1,518 bytes, which is 3,036 nibbles.
- Idle symbols on the line do not generate data across the MII, so the FIFO can reposition its pointer after each packet.
- The clocks from each port are asynchronous.

The following seven MII signals are required on each side of the FIFO for data to flow between the two ports:

- TXCLK
- TXD[3:0]
- TXEN
- TXER
- RXCLK
- RXD[3:0]
- RXDV
- RXER

For the twisted-pair-to-fiber converter, an Altera FPGA is used as the FIFO. Figure 3 provides FIFO implementation in VHDL code in the Altera FPGA (the VHDL code is available with this document).

Figure 3. 3x6 FIFO Block Diagram



4.0 LXT973 Media Converter Board Schematics

Figure 4. Power Control (Rev A2)

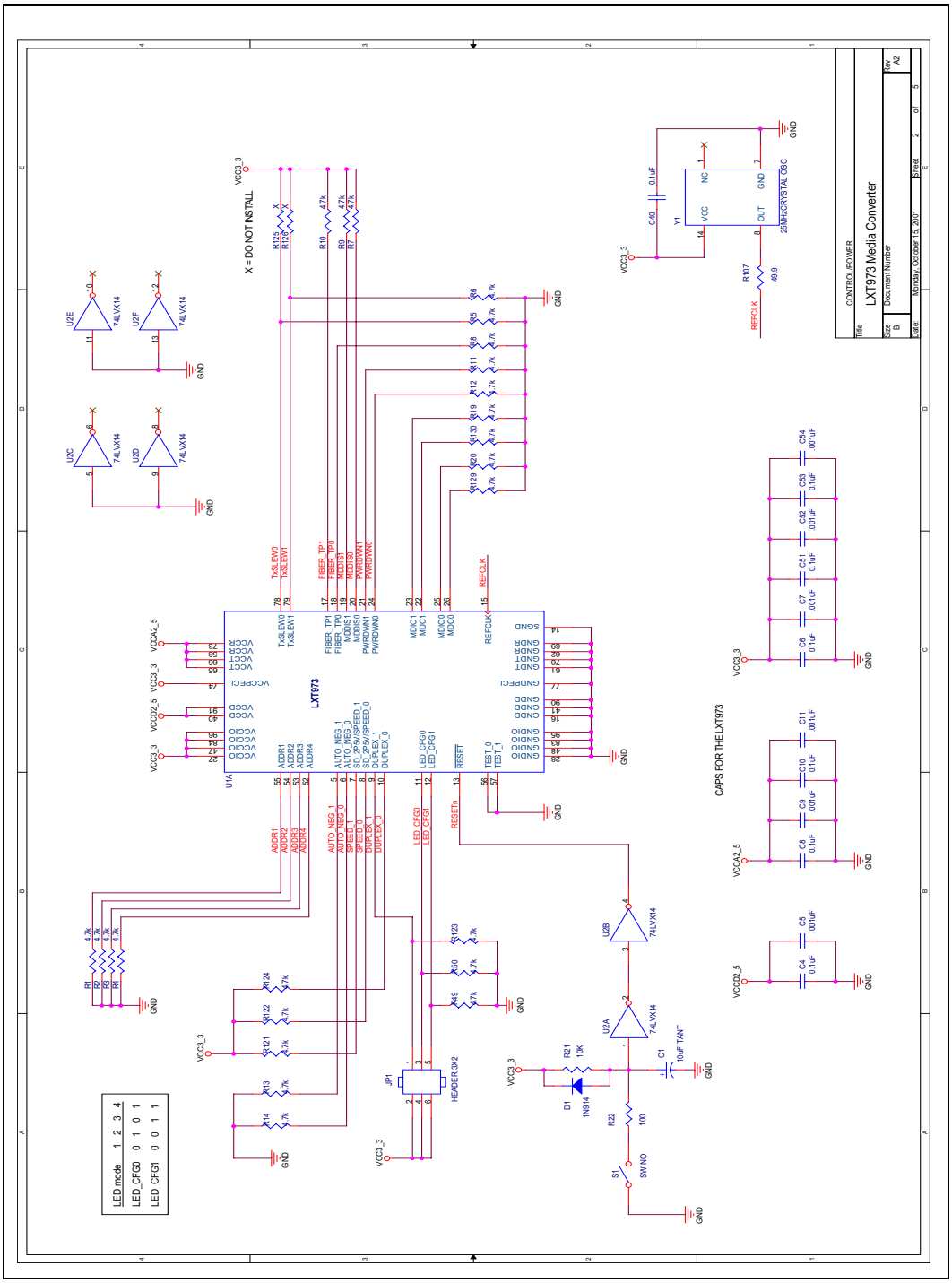


Figure 5. MII Ports - FIFO

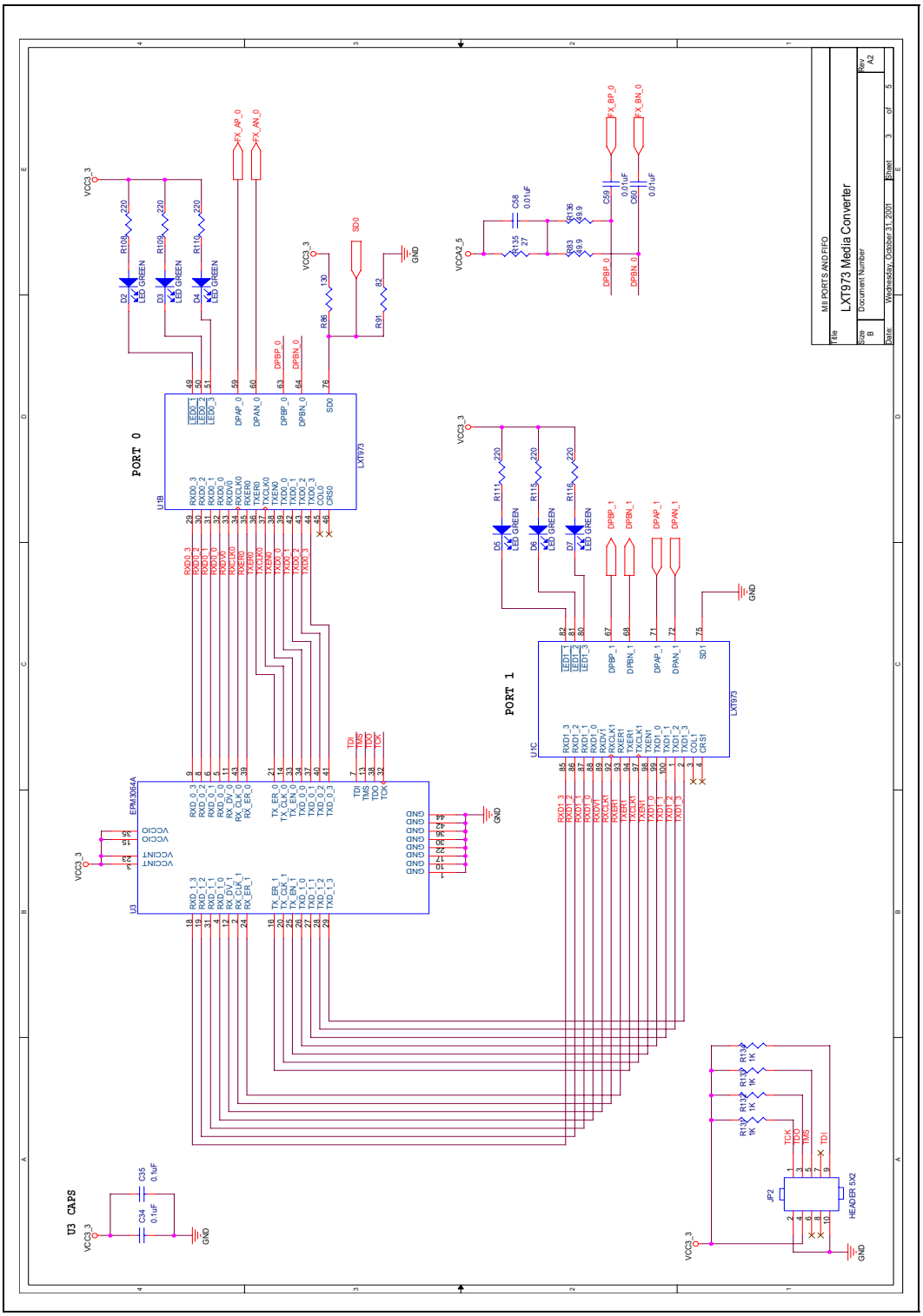


Figure 6. TP Port 1 - Fiber Port 0

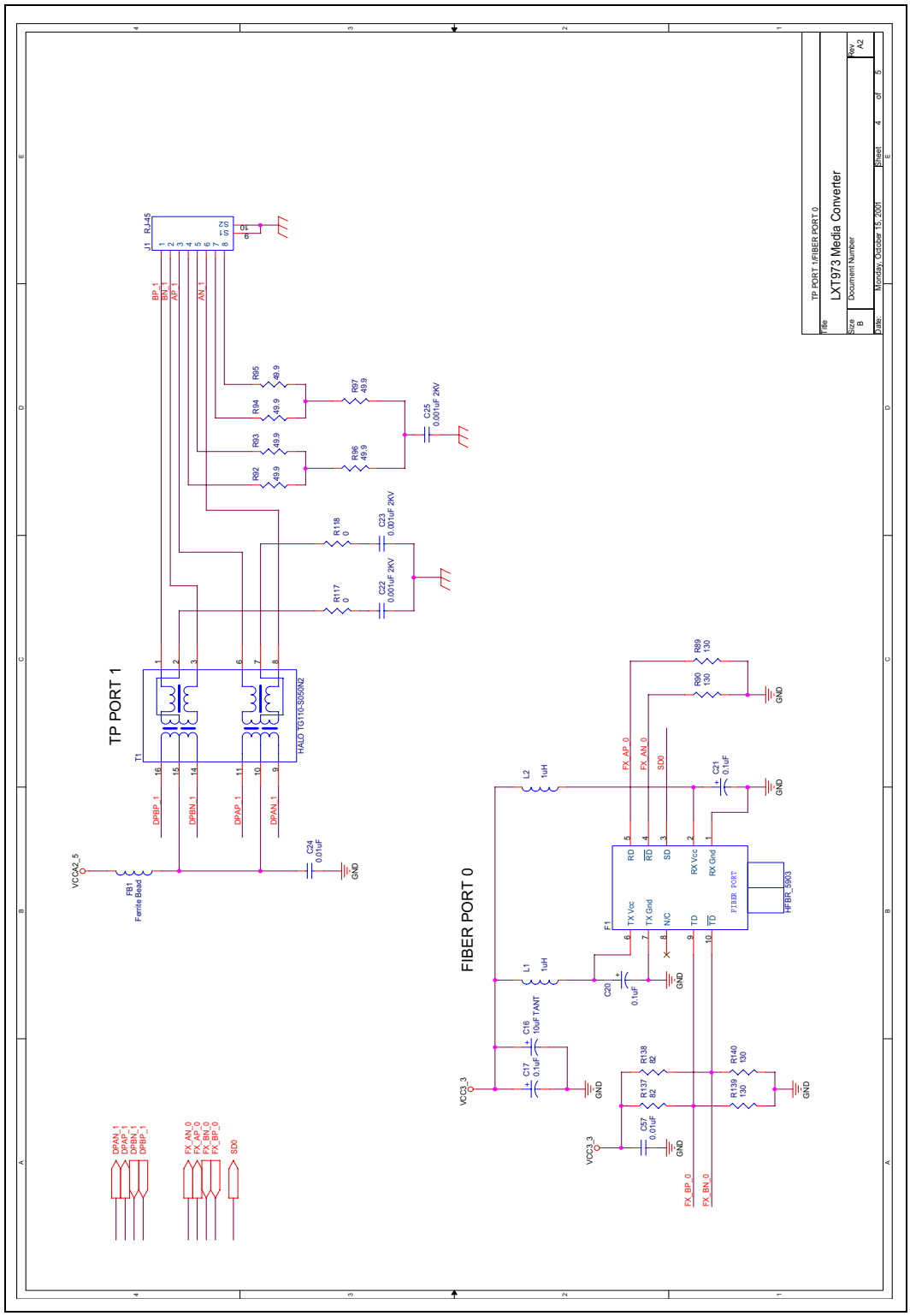
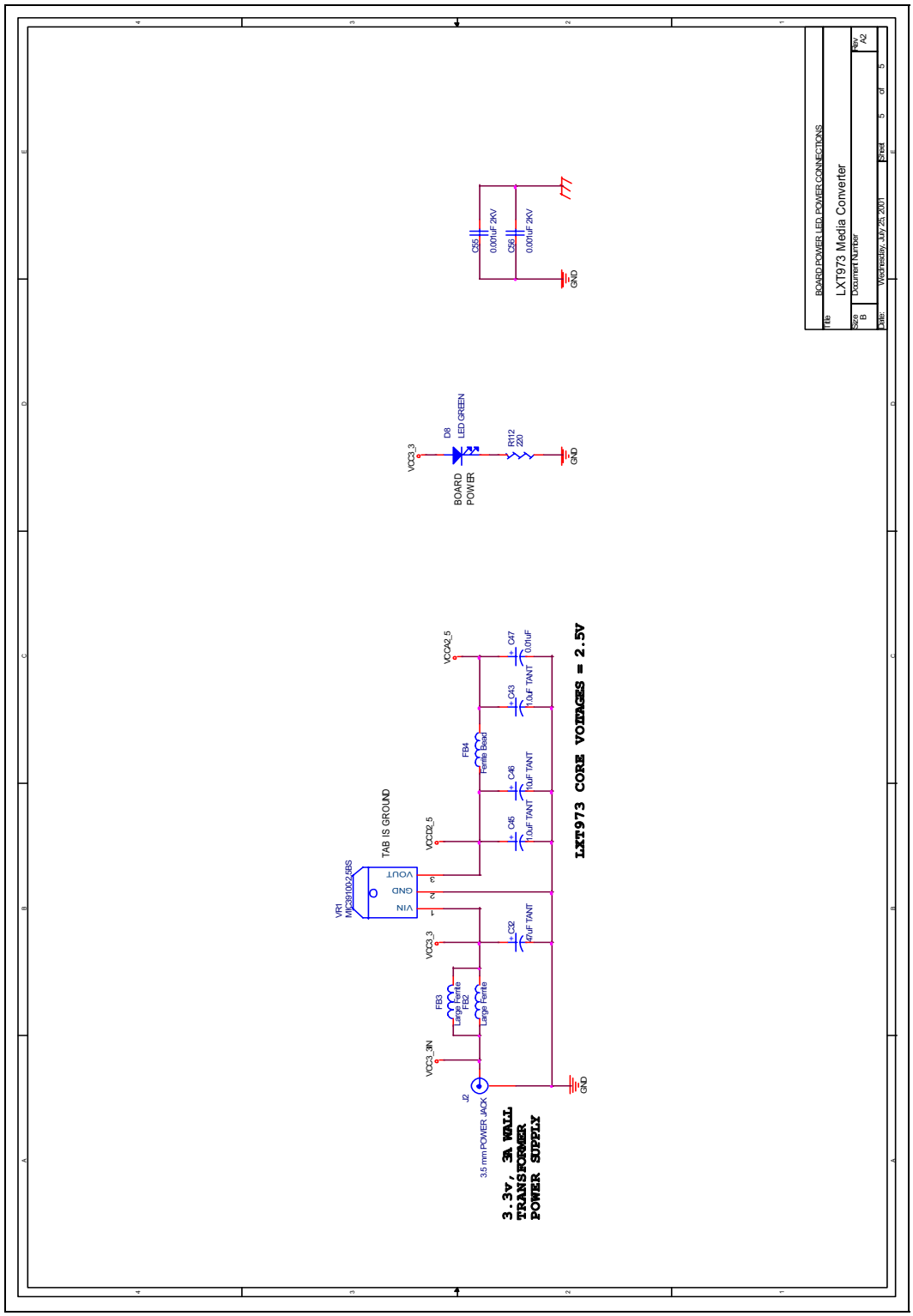


Figure 7. Board Power



5.0 LXT973 Media Converter Board Bill of Materials

Table 2. LXT973 Media Converter Board Bill of Materials (Rev A2)

Reference Designator	Description	Manufacturer	Part Number
C1, 16, 46	CAP 10UF 6.3V TANT (CASEA)	Panasonic	ECS-TOJY106R
C4, 6, 8, 10, 34-35, 40, 51, 53	CAP 0.1UF 16V X7R (0603)	Panasonic	ECJ-1VB1C104K
C5, 7, 9, 11, 52, 54	CAP 1000PF 50V X7R (0603)	Panasonic	ECJ-1VB1H102K
C17, 20-21	CAP 0.1UF 50V X7R +/- 10% (0805)	AVX	08055C104KATMA
C22-23, 25, 55-56	CAP 1000PF 20% 2KV X7R (1812)	AVX	1812GC102KAT1A
C24, 57-60	CAP 0.01UF 25V 10% CER (0603)	Panasonic	ECJ-1VB1E103K
C32	CAP 47UF 10V TAN42EIA (CASED)	Panasonic	ECS-H1AD476R
C43, 45	CAP 1UF 16V TANT (CASEA)	Panasonic	ECS-T1CY105R
C47	CAP 0.01UF 50V 10% CER (0805)	Panasonic	ECU-V1H103KBG
D1	DIODE SK34 40V 3A SCHOTTKY SMD ( )	Diodes, Inc.	SK34DI
D2-8	LED GREEN SS TYPE LOW CUR SMD	Panasonic	LNJ308G8LRA
F1	IC INTERFACE HFBR_5903 3.3V FIBER TRANSCEIVER ( )	HP	HFBR_5903 FIBER PORT
FB1, 4	FBEAD REPL/CT50ACC-322513T	Central Technology	CTCB1210-600-HC
FB2-3	FBEAD	Fair-Rite	2961666671
J1	CONN RJ45 8-POSITION JACK	AMP	520426-4
J2	CONN PWRJACK RAPC722 2.1MM RT-ANGLE	SwitchCraft	RAPC722
JP1	HEADER 3X2	Berg	C9192-280-3
JP2	HEADER 5X2	Berg	C9192-280-5
L1-2	INDUCTOR 1UH SMD (1206)	TDK	TDKMLF3216A1R0 KT000
R1-14, 19-20, 49-50, 121-124, 129-130	RES 4.75K 1/16W 1% (0603)	Panasonic	ERJ-3EKF4751V
R125-126	DO NOT INSTALL	N/A	N/A
R21	RES 10K 1/8W 1% (1206)	Panasonic	ERJ-8ENF1002V
R22	RES 100 OHM 1/8W 1% (1206)	Panasonic	ERJ-8ENF1000V
R83, 92-97, 107, 136	RES 49.9 0HM 1/10W 1% (0805)	Panasonic	ERJ-6ENF49R9V
R86-90, 139-140	RES 130 OHM 1/16W 1% (0603) SMD	Panasonic	ERJ-3EKF1300V
R91, 137-138	RES 82.5 OHM 1/16W 1% (0603) SMD	Panasonic	ERJ-3EKF82R5V

Table 2. LXT973 Media Converter Board Bill of Materials (Rev A2) (Continued)

Reference Designator	Description	Manufacturer	Part Number
R108-112, 115-116	RES 221 OHM 1/16W 1% (0603)	Panasonic	ERJ-3EKF2210V
R117-118	RES 0 OHM 1/10W 5% (0805)	Panasonic	ERJ-6GEY0R00V
R131-134	RES 1.00K 1/16W 1% (0603)	Panasonic	ERJ-3EKF1001V
R135	RES 27.4 OHM 1% 1/10W (0805) SMD	Panasonic	ERJ-6ENF27R4V
S1	SWITCH SPST MOM KEY J-LEAD SMD	C&K Components	KT11P2JM
T1	IC XFMR TG110-S050N2 16 PIN SOIC	Halo	TG110-S050N2
U1	INTEL IC PHY 2 PORT	Intel	LXT973
U2	IC LOGIC 74LVX14 HEX SCHMITT TRIG INV 14 PIN SOIC	Toshiba	TC74LVX14FN
U3	IC EPM3064ALC44-4 CPLD PROG LOGIC	Altera	EPM3064ALC44-4
VR1	REG 1A SOT 223	Micrel Semiconductor	MIC39100-2.5BS
Y1	OSC 25.000MHZ CMOS/TTL FULL SIZE	CTS Reeves	MX045-25.000
	3V, 5A WALL TRANSFORMER	Ault, Inc.	PW160KA0303F01