DATA SHEET

MARCH 1999
Revision 1.1

LXP610

Low-Jitter Multi-Rate Clock Adapter (CLAD)

General Description

The LXP610 Multi-Rate Clock Adapter (CLAD) offers pin-selectable frequency conversion between T1 and E1 rates as well as 8 additional rates from 1.544 MHz to 8.192 MHz. The output clock is frequency-locked to the input clock. When an input frame sync pulse is provided, the CLAD phase-locks the input and output clocks together, and locks the 8 kHz output frame sync pulse to the input frame sync pulse. The frame sync polarity is also pin-selectable.

Five different high frequency output clocks are available for applications which require a higher-than-baud rate backplane or system clock. The high frequency output (HFO) clock varies with the input clock frequency.

Level One's patented locking method enables the CLAD to perform frequency conversion with no external components, while generating very little jitter on the output clock. The conversion is digitally controlled so the output clock is as accurate as the input clock.

The CLAD is an advanced CMOS device and requires only a single +5 V power supply.

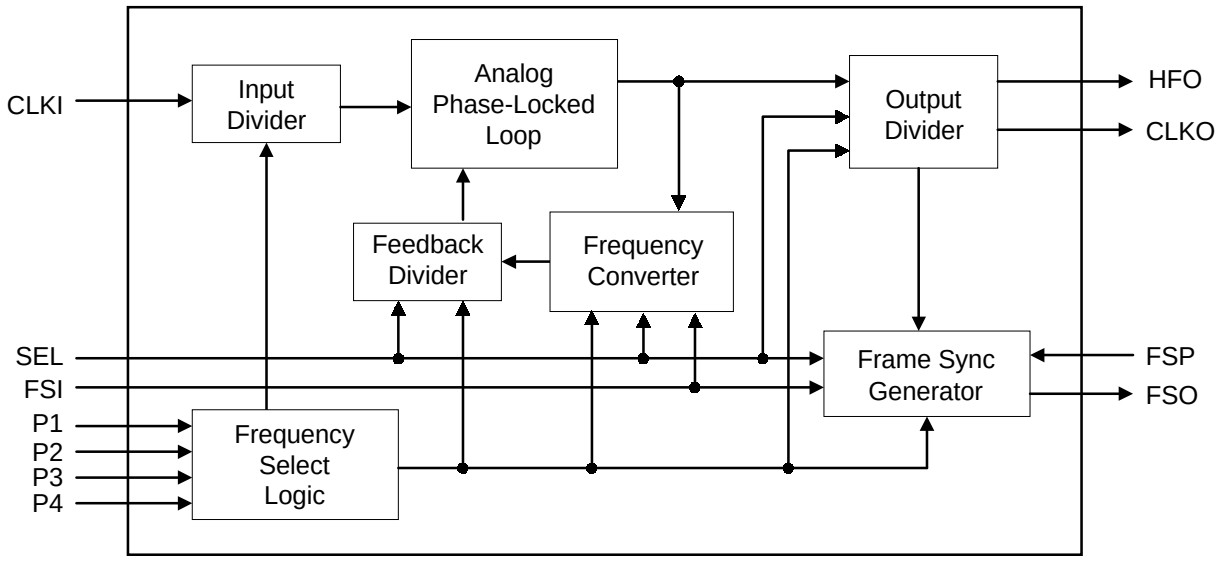
Features

- Translates between 10 different frequencies.
- Generates basic and high frequency output clocks and frame sync from an input clock and its frame sync.
- High Frequency Output clock for higher-than-baud rate backplane systems
- Low output jitter meets AT&T Publication 62411 for 1.544 MHz, and ITU Recommendation G.823 for 2.048 MHz
- Digital control of frequency conversion process
- No external components
- Pin-selectable operation mode
- Low-power 5 V only CMOS in 14-pin plastic DIP, 28-pin PLCC and 16 pin SOIC packages

Applications

- Internal timing system for Channel Banks, Digital Loop Carriers, Multiplexers, Internal Timing Generators, etc.
- Conversion between T1/E1 clock rates and higher frequency backplane rates (T1/E1 converter)
- Special backplane interfaces (e.g. NTI 2.56 MHz)

LXP610 Block Diagram



Refer to www.level1.com for most current information.

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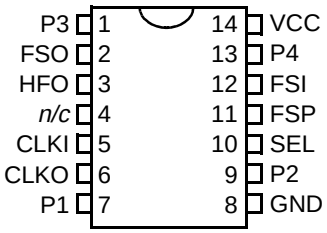
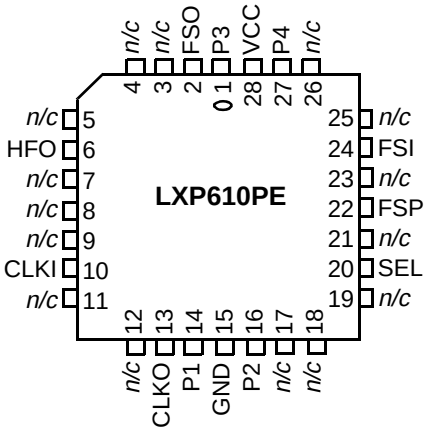
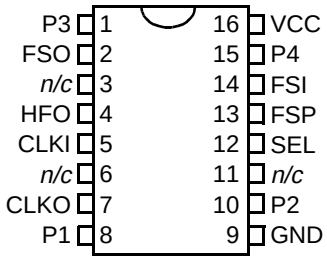
PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXP610 Pin Assignments



LXP610NE





LXP610SE

Table 1: Pin Descriptions

Pin #			Sym	I/O	Description
DIP	PLCC	SOIC			
1	1	1	P3	DI	**Program Pins.** These signals control frequency conversion and FSO pulse width as specified in Table 2. Used in conjunction with SEL pin.
7	14	8	P1	DI	
9	16	10	P2	DI	
13	27	15	P4	DI	
2	2	2	FSO	DO	**Frame Sync Output.** Frame synchronization output pulse at 8 kHz. FSO is synchronized to CLKO and to FSI (if FSI is provided). Pulse width is programmable as specified in Table 2. FSO is active Low when FSP = 0; active High when FSP = 1.
3	6	4	HFO	DO	**High Frequency Output.** A high frequency output that may be used to clock external devices. The HFO output frequency is determined by P1-P4 and SEL pins as specified in Table 2.
5	10	5	CLKI	DI	**Clock Input.** Primary rate clock to be converted.
6	13	7	CLKO	D0	**Clock Output**. Primary rate clock derived from CLKI.
8	15	9	GND	S	**Ground**. Connect to power supply ground
10	20	12	SEL	DI	**Mode Select.** Controls frequency conversion and FSO pulse width. Used in conjunction with P1-P4 pins as specified in Table 2.
11	22	13	FSP	DI	**Frame Sync Polarity.** When High, causes FSI and FSO to be active High pulses.
12	24	14	FSI	DI	**Frame Sync Input**. Frame synchronization pulse (8 kHz or any sub-rate multiple). Active Low when FSP = 0. Active High when FSP = 1.
14	28	16	VCC	S	**Power Supply.** +5 V power supply.
4	3, 4, 5, 7, 8, 9, 11, 12, 17, 18, 19, 21, 23, 25, 26	3, 6, 11	*n/c*	–	**Not Connected.** These pins must be left unconnected.

1. DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output; S = Supply.

FUNCTIONAL DESCRIPTION

The CLAD converts an input clock (CLKI) at a particular frequency to an output clock (CLKO) at a different frequency. It also produces a frame sync output (FSO) and a high frequency output clock (HFO). The HFO frequency is a multiple (2x, 3x, 4x, or 5x) of CLKO. The specific frequencies are determined by the Mode Select (SEL) and Program (P1 - P4) inputs. Tables 2 and 3 list the CLKO and HFO frequencies available with a given input CLKI. Table 2 is keyed to Program Pin settings; Table 3 is keyed to CLKI frequencies. Refer to Test Specifications for output frame sync alignments.

CLKO is always frequency-locked to CLKI. When a frame sync input (FSI) is supplied, CLKI and CLKO are also phase-locked. The CLAD accepts FSI pulses at 8 kHz, or at any sub-rate multiple (i.e., 1, 2 or 4 kHz). The frame sync output (FSO) pulse is synchronized to the FSI pulse.

The pulse width of FSO is programmable as shown in Tables 2 and 3. A long FSO pulse is one CLKO period wide and centered on the rising edge of CLKO. A short pulse is one half of the CLKO period wide and centered on the rising edge of CLKO.

When an 8 kHz FSI is first asserted, the CLKI and CLKO rising edges will be aligned within a maximum of 500 ms. For other FSI rates, the alignment period is correspondingly lengthened. For example, at 4 kHz, the FSI/FSO alignment is completed within a maximum of one second.

If an input frame sync pulse is not provided, the FSI pin should be tied High or Low. CLKO and FSO are still generated with the CLKO frequency locked to CLKI.

Table 2: Program Pin Functions

				SEL = 0				SEL = 1			
P4	P3	P2	P1	CLKI (MHz)	CLKO (MHz)	HFO (MHz)	FSO pulse width	CLKI (MHz)	CLKO (MHz)	HFO (MHz)	FSO pulse width
0	0	0	0	1.544	2.048	6.144	Long	2.048	3.088	6.176	Long
0	0	0	1	3.088	2.048	8.192	Short	2.048	3.088	6.176	Long
0	0	1	0	1.544	2.048	6.144	Long	2.048	1.544	6.176	Long
0	0	1	1	1.544	2.048	8.192	Short	2.048	1.544	6.176	Long
0	1	0	0	1.544	2.560	7.680	Long	2.560	1.544	7.720	Long
0	1	0	1	6.176	4.096	8.192	Long	8.192	3.088	6.176	Long
0	1	1	0	1.544	2.560	7.680	Long	2.560	1.544	7.720	Long
0	1	1	1	6.176	2.048	8.192	Short	8.192	1.544	6.176	Long
1	0	0	0	3.088	2.048	6.144	Long	2.048	3.088	6.176	Long
1	0	0	1	3.088	4.096	8.192	Long	4.096	3.088	6.176	Long
1	0	1	0	3.088	2.048	6.144	Long	2.048	3.088	6.176	Long
1	0	1	1	1.544	4.096	8.192	Long	4.096	1.544	6.176	Long
1	1	0	0	6.176	2.560	7.680	Long	2.560	1.544	7.720	Long
1	1	0	1	6.176	4.096	8.192	Long	8.192	3.088	6.176	Long
1	1	1	0	6.176	2.560	7.680	Long	2.560	1.544	7.720	Long
1	1	1	1	6.176	4.096	8.192	Long	8.192	1.544	6.176	Long

Output Jitter

The CLAD output jitter meets the following specifications:

- 2.048 MHz or 4.096 MHz to 1.544 MHz: In this mode of operation, the CLAD meets the output jitter requirements of AT&T Publication 62411. When there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.020 UI pp with no bandlimiting, 0.010 UI in the 10 Hz - 40 kHz band, and 0.012 UI in the 8 - 40 kHz band.
- 1.544 MHz to 2.048 MHz or 4.096 MHz: In this mode of operation, when there is no jitter on input clock CLKI, the maximum jitter on CLKO is 0.035 UI pp over the range of 20 Hz to 100 kHz, and 0.025 UP pp in the 18-100 kHz band.

Jitter Transfer

The CLAD is sensitive to jitter on the input clock in certain frequency bands. The jitter transfer curve is determined by the frequency and amplitude of the input jitter. Figures 4 and 5 on page 9 show nominal jitter transfer measured in nanoseconds. These figures graph output jitter (less intrinsic jitter) divided by input jitter (0.25 UI). Jitter transfer from a 2.048 MHz CLKI to a 1.544 MHz CLKO is shown in Figure 4. In this mode, jitter in the critical 8 kHz band is attenuated while jitter in the 18 - 70 kHz band is transferred with a small net gain. Jitter transfer from a 1.544 MHz CLKI to a 2.048 MHz CLKO is shown in Figure 5. In both modes, with an input jitter level of 0.25 UI, jitter transfer is held below a net gain of 1.110. (Jitter transfer varies with the input jitter level. Performance in a particular application should be verified in the actual circuit.)

Table 3: Input to Output Frequency Conversion Options

CLKI (MHz)	CLKO (MHz)	HFO (MHz)	FSO pulse width	P4	P3	P2	P1	SEL
1.544	2.048	6.144	Long	0	0	X	0	0
1.544	2.048	8.192	Short	0	0	1	1	0
1.544	2.560	7.680	Long	0	1	X	0	0
1.544	4.096	8.192	Long	1	0	1	1	0
2.048	1.544	6.176	Long	0	0	1	X	1
2.048	3.088	6.176	Long	0	0	0	X	1
2.048	3.088	6.176		1	0	X	0	1
2.560	1.544	7.720	Long	X	1	X	0	1
3.088	2.048	6.144	Long	1	0	X	0	0
3.088	2.048	8.192	Short	0	0	0	1	0
3.088	4.096	8.192	Long	1	0	0	1	0
4.096	1.544	6.176	Long	1	0	1	1	1
4.096	3.088	6.176	Long	1	0	0	1	1
6.176	2.048	8.192	Short	0	1	1	1	0
6.176	2.560	7.680	Long	1	1	X	0	0
6.176	4.096	8.192	Long	0	1	0	1	0
6.176	4.096	8.192		1	1	X	1	0
8.192	1.544	6.176	Long	X	1	1	1	1
8.192	3.088	6.176	Long	X	1	0	1	1

APPLICATION INFORMATION

Frame Sync Generation

A frame sync pulse (FSI) is required to synchronize the CLAD input and output clocks. If a frame sync pulse is not provided on the backplane, one can be generated from the existing 2.048 MHz backplane clock. A typical FSI generation circuit is shown in Figure 2.

Power Supply Decoupling and Filtering

The LXP610 CLAD is designed to meet AT&T Publication 62411 specifications for jitter in the range from 10 Hz to 100 kHz. Proper power supply decoupling is critical for meeting these specifications. As shown in Figure 3, a standard 0.1 µF bypass capacitor is recommended.

The CLAD is a monolithic silicon device which incorporates both analog and digital circuits. CLAD application circuit design may require closer attention to power supply filtering and bypassing than required for strictly digital devices.

Switching power supplies which operate below 100 kHz may produce noise spikes which can affect the analog sections of the CLAD. These spikes should be filtered with an RC network at the CLAD VCC pin.

Typical Application

Figure 3 shows a typical application circuit using a pair of LXP610 CLADs to convert between the 2.56 MHz backplane frequency and the 1.544 MHz T1 rate. The CLAD at the top of the figure provides the 1.544 MHz TCLK for the T1 framer and transceiver. For conversion from 2.56 MHz to 1.544 MHz, P1, P2, and P4 are tied Low; and P3 and SEL are tied High. In this configuration, the LXP610 HFO is 7.720 MHz.

The CLAD at the bottom of Figure 3 produces the 2.56 MHz backplane clock. For conversion from 1.544 MHz to 2.56 MHz, P1, P2, P3 and P4 are tied High; and SEL is tied Low. The HFO produced in this configuration is 7.680 MHz.

Figure 2: Frame Sync (FSI) Generation Circuit

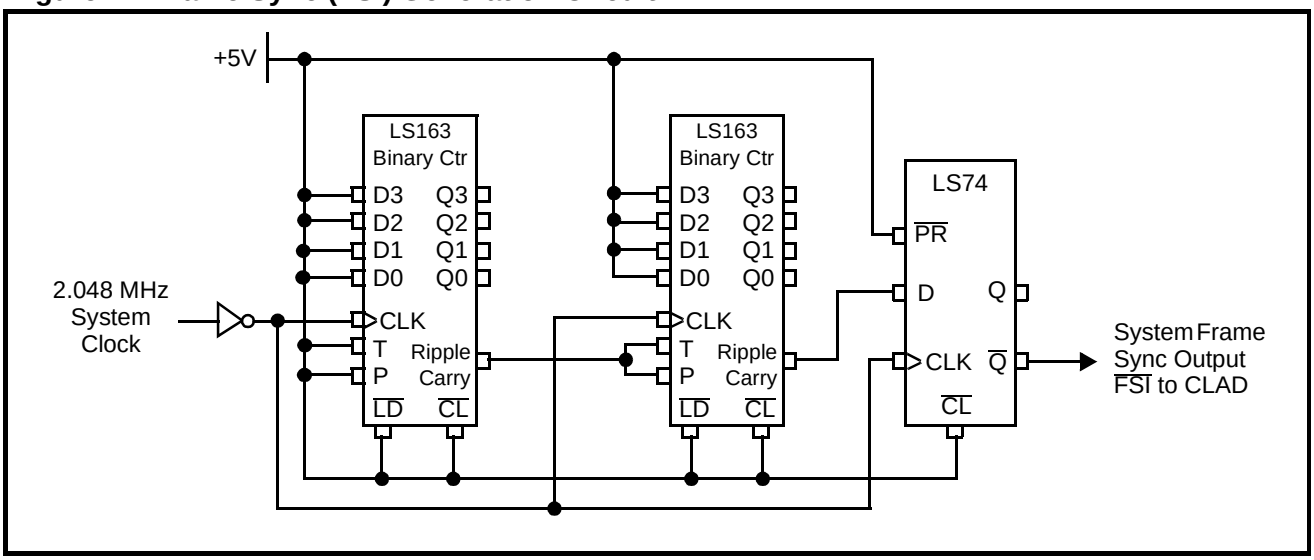
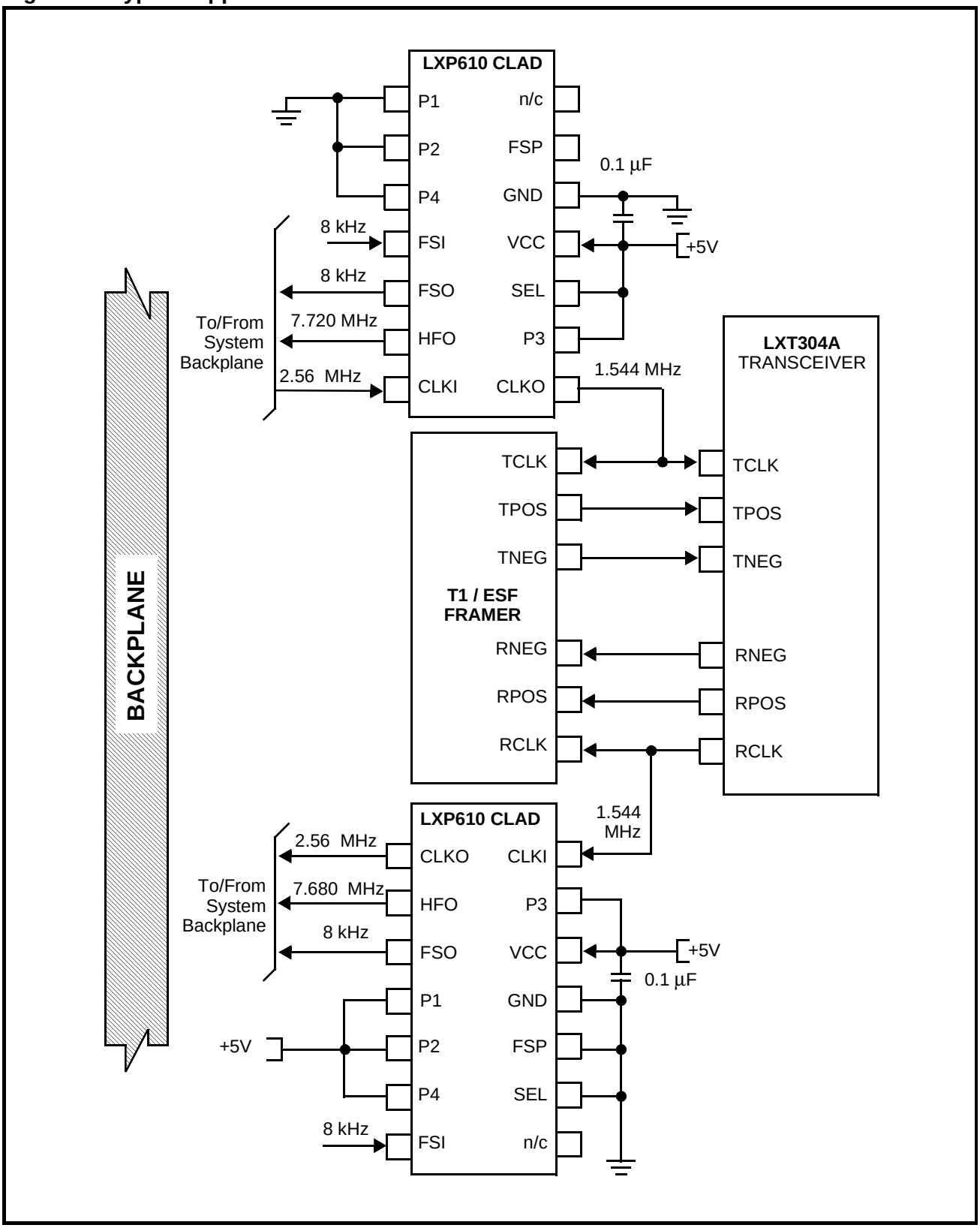


Figure 3: Typical Application Circuit



TEST SPECIFICATIONS

NOTE

Tables 4 through 9 and Figures 4 through 11 represent the performance specifications of the LXP610 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 6 through 9 are guaranteed over the recommended operating conditions specified in Table 5.

Table 4: Absolute Maximum Values

Parameter	Symbol	Min	Max	Unit
Supply voltage (referenced to GND)	RV+, TV+	-0.3	7.0	V
Voltage, any I/O pin	V_{IO}	GND - 0.3	VCC + 0.3	V
Current, any I/O pin[1]	I_{IO}	-10	10	mA
Storage temperature	T_{STG}	-65	+150	ºC
Power dissipation	Pd	–	340	mW

CAUTION

Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

1. Transient currents of up to 100 mA will not cause SCR latch-up.

Table 5: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage[1]	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}	–	–	8	mA	No TTL loading
	I_{CC}	–	–	14	mA	Full TTL loading
Operating temperature	T_{OP}	-40	–	85	ºC	

1. Voltages with respect to ground unless otherwise specified.

Table 6: Digital Electrical Characteristics

Parameter	Sym	Min	Max	Unit
Input Low voltage	V_{IL}	–	0.8	V
Input High voltage	V_{IH}	2.0	–	V
Output Low voltage (I_{OL} = +1.6 mA)	V_{OL}	–	0.4	V
Output Low voltage (I_{OL} < +10 µA)	V_{OL}	–	0.2	V
Output High voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	–	V
Output High voltage (I_{OH} < -10 µA)	V_{OH}	4.5	–	V
Input leakage current	I_{LL}	-10	10	µA

Table 7: Output Jitter Specifications

Parameter	Sym	Frequency	Spec[1]	Typ[2]	Max	Unit	Test Conditions
Output Jitter on CLKO CLKO=1.544 MHz	TJ	No Bandlimiting	0.050	0.010	0.020	UI pp	CLKI=2.048 or 4.096 MHz JI=0 $\overline{FSI}$ applied
		10 Hz to 40 kHz	0.025	0.005	0.010	UI pp	
		8 kHz to 40 kHz	0.025	0.006	0.012	UI pp	
Output Jitter on CLKO CLKO=2.048 MHz	TJ	20 Hz to 100 kHz	1.500	0.025	0.035	UI pp	CLKI=1.544 MHz, JI=0 $\overline{FSI}$ applied
		18 kHz to 100 kHz	0.200	0.015	0.025	UI pp	

1. Specifications from AT&T Publication 62411 and ITU Recommendations G.823 (for 1.544 MHz and 2.048 MHz, respectively).
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 4: Nominal Jitter Transfer - 2.048 MHz CLKI to 1.544 MHz CLKO (Input Jitter = 0.25 UI)

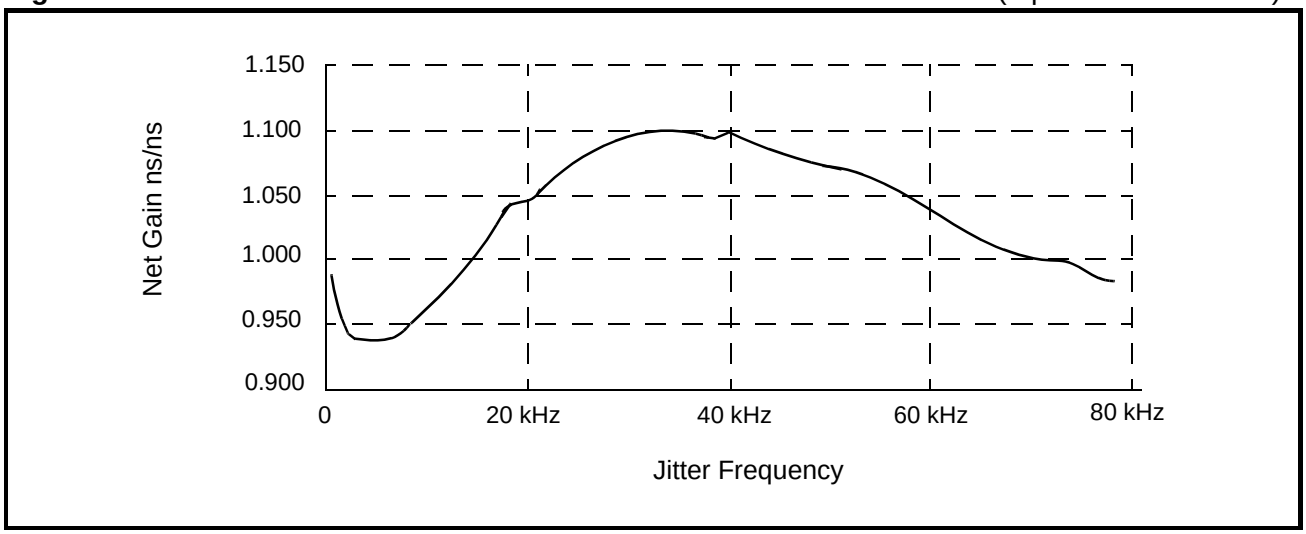


Figure 5: Nominal Jitter Transfer - 1.544 MHz CLKI to 2.048 MHz CLKO (Input Jitter = 0.25 UI)

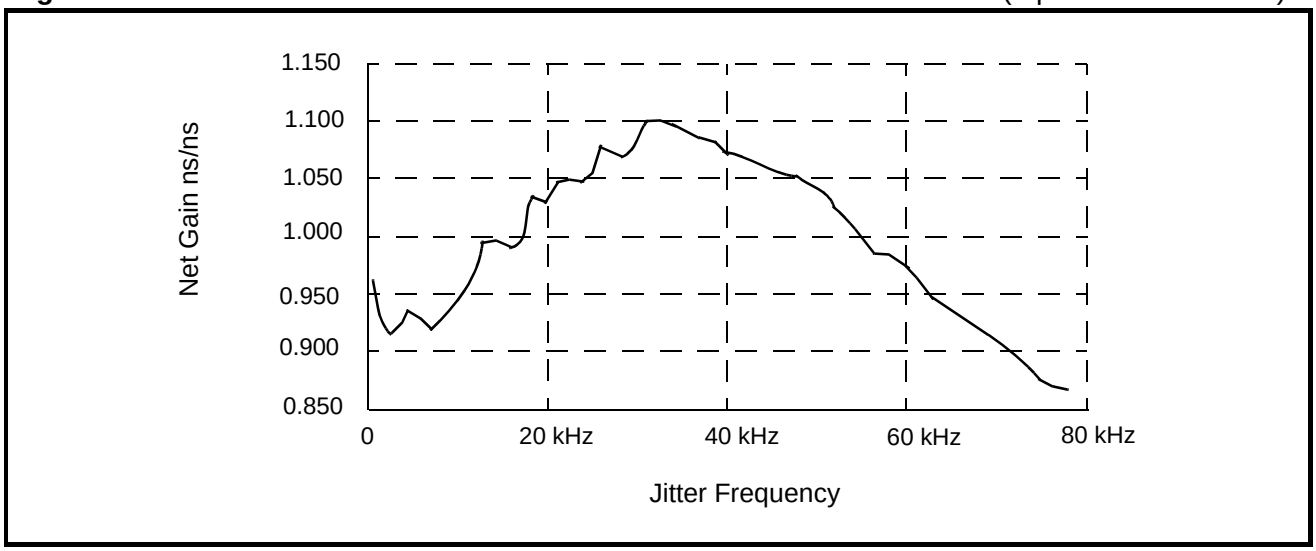


Table 8: Timing Values (See Figure 6)

Parameter	Symbol	Minimum	Maximum	Unit
Capture range on CLKI	–	±10000	–	ppm
Lock range on CLKI	–	±10000	–	ppm
Input clock duty cycle	–	35	65	%
Rise/fall time on CLKI, FSI	Trf	–	40	ns
Rise/fall time on CLKO, FSO, HFO with a 25 pF load	Trf	–	40	ns

Figure 6: Rise and Fall Times

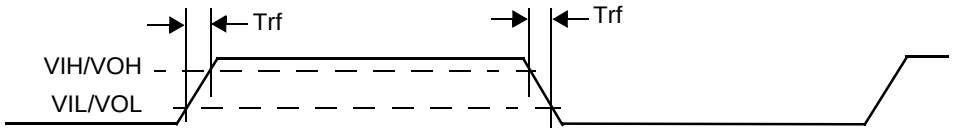


Table 9: Timing Values (See Figure 7 through Figure 11)

Parameter	Sym	Minimum	Typical	Maximum	Unit
$\overline{\text{FSI}}$ setup time from CLKI rising	Tsui	46	–	–	ns
$\overline{\text{FSI}}$/CKLI hold time	Thi	30	–	–	ns
$\overline{\text{FSI}}$ pulse width (Low)	Twi	76	–	T_{CLKI}[1]	ns
CLKO delay from CLKI	Td_C	-15	0	+15	ns
CLKO duty cycle	Cdc	49	–	51	%
FSO delay from HFO	Td_F	-5	–	30	ns
FSO pulse width (Low)	Two	–	–	T_{CLKO}[2]	ns
CLKO delay from HFO	Td_H	-15	–	+15	ns

1. T_{CLKI} is the period of CLKI.
2. T_{CLKO} is the period of CLKO.

Figure 7: Timing Relationships - FSI / CLKI to CLKO / FSO and HFO

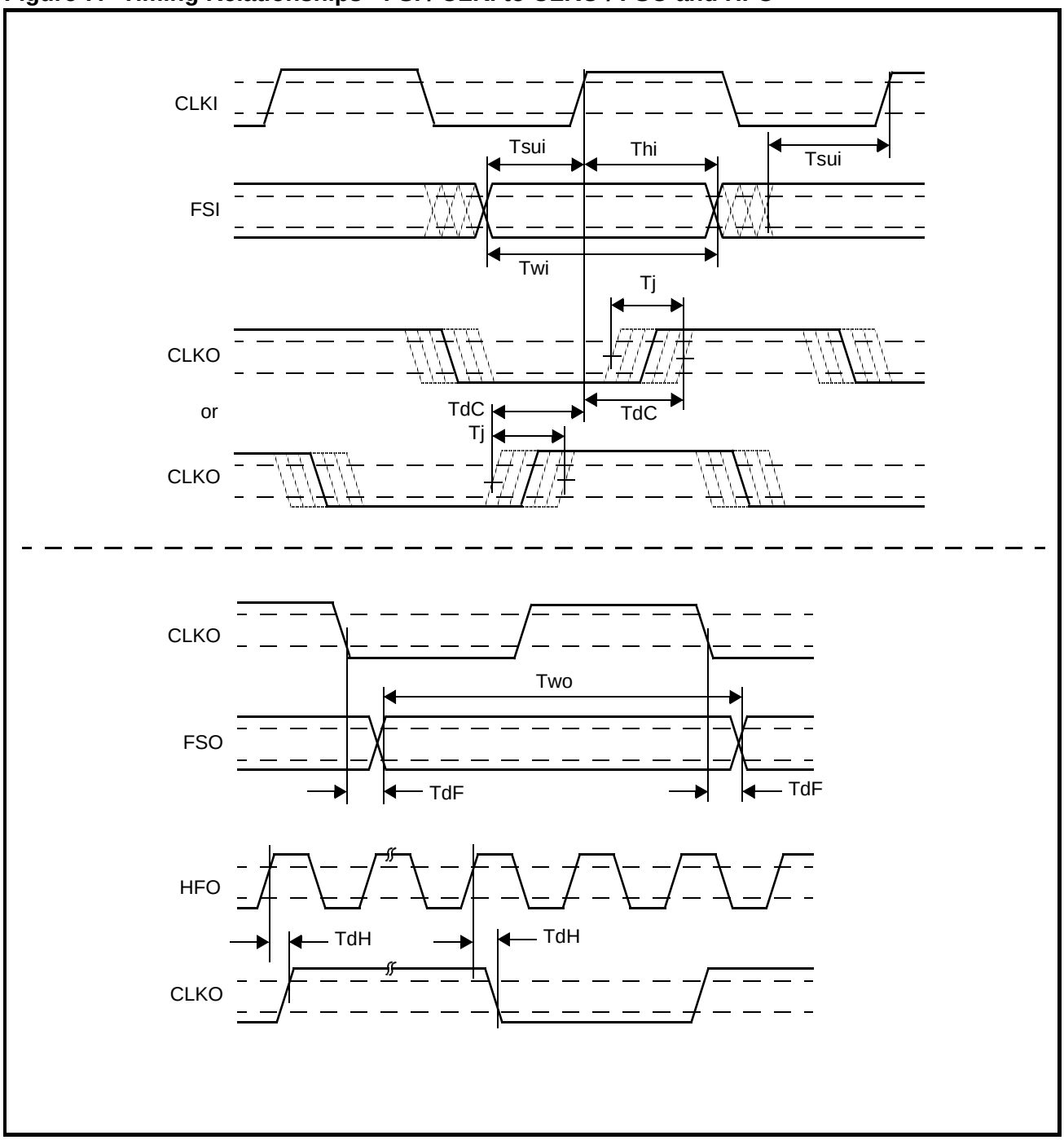


Figure 8: Output Frame Sync Alignment when HFO = 2 x CLKO

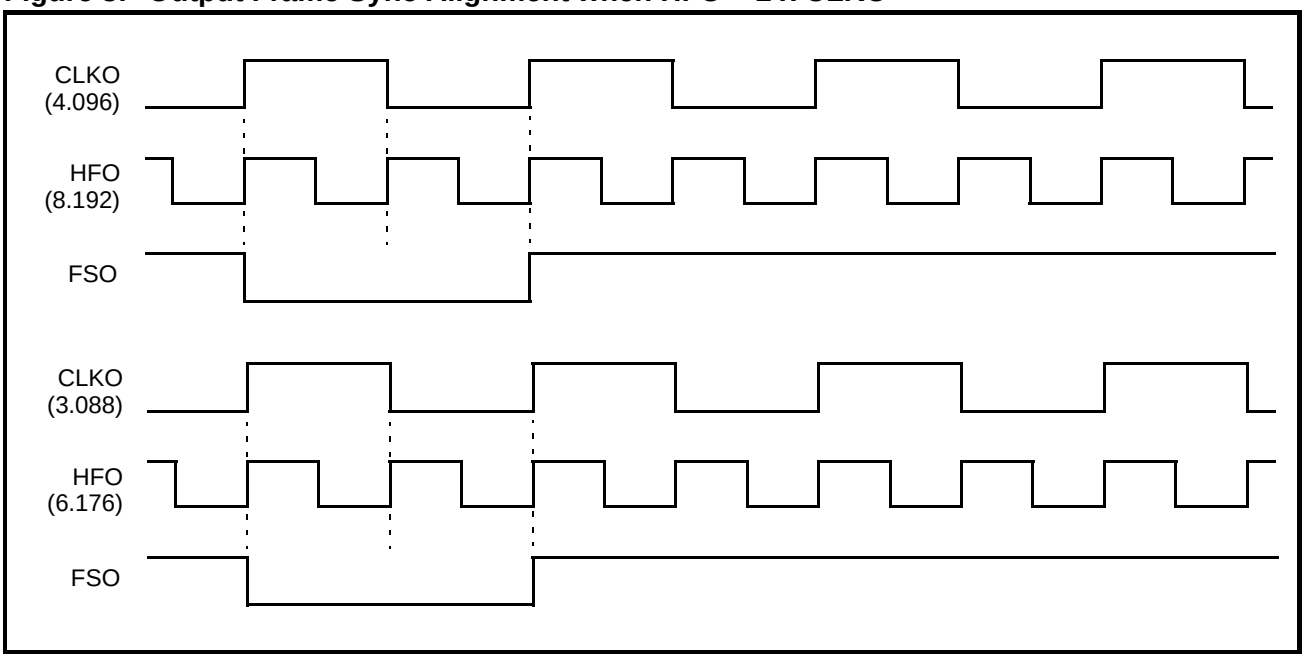


Figure 9: Output Frame Sync Alignment when HFO = 3 x CLKO

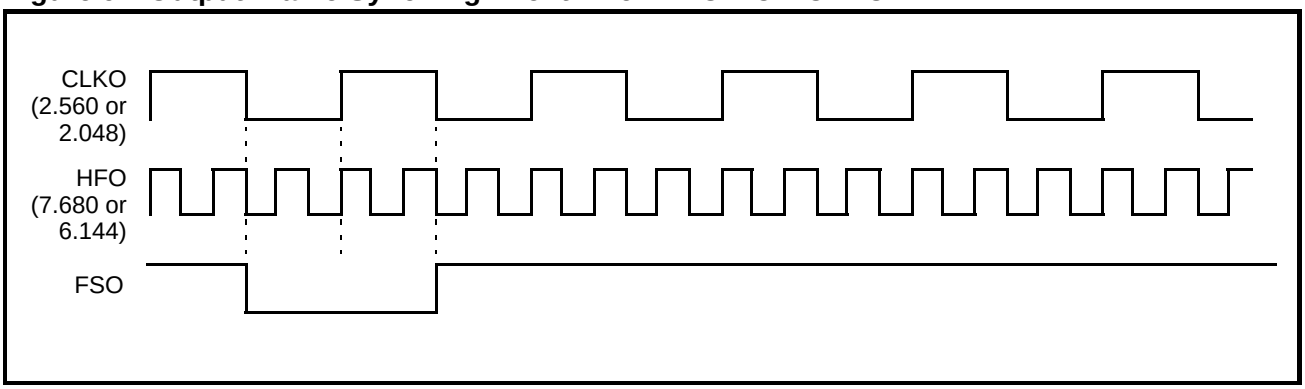


Figure 10: Output Frame Sync Alignment when HFO = 4 x CLKO

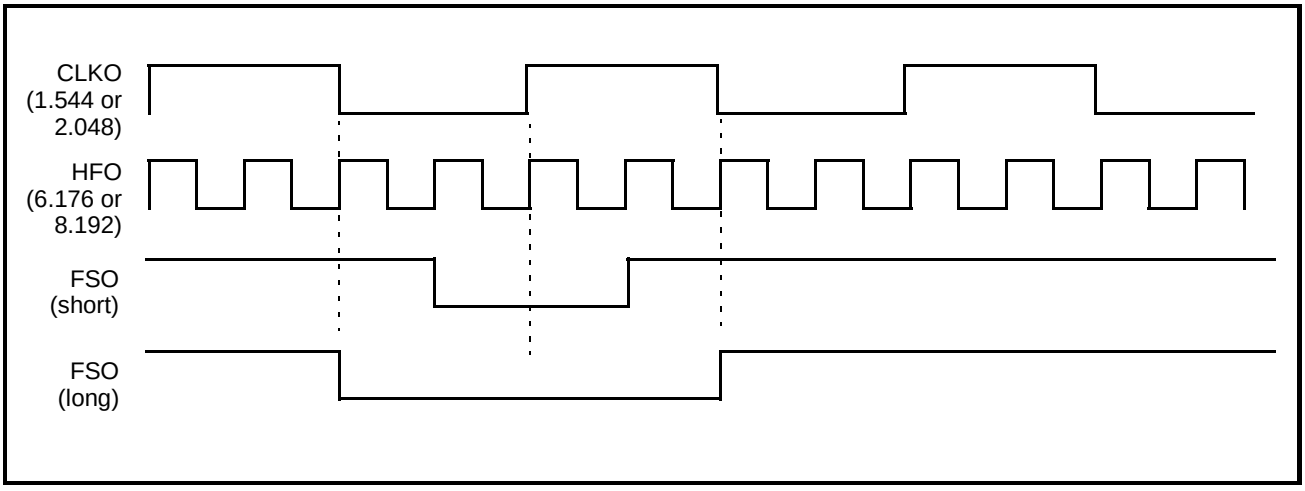
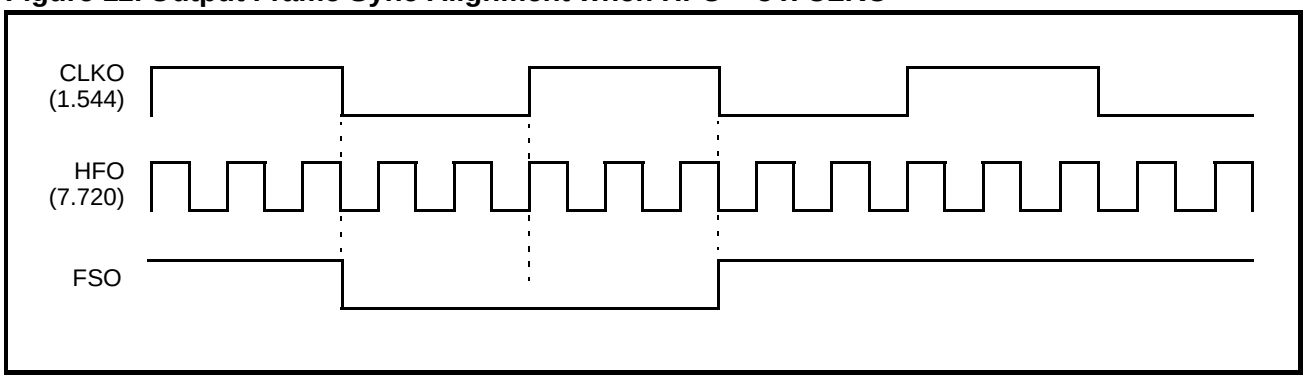


Figure 11: Output Frame Sync Alignment when HFO = 5 x CLKO

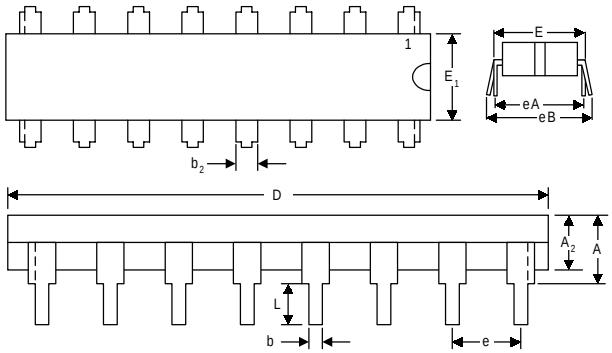


MECHANICAL SPECIFICATIONS

Figure 12: LXP610NE and LXP610PE Package Specifications

14-pin DIP

- Part Number LXP610NE
- Extended Temperature Range (-40 °C to 85 °C)

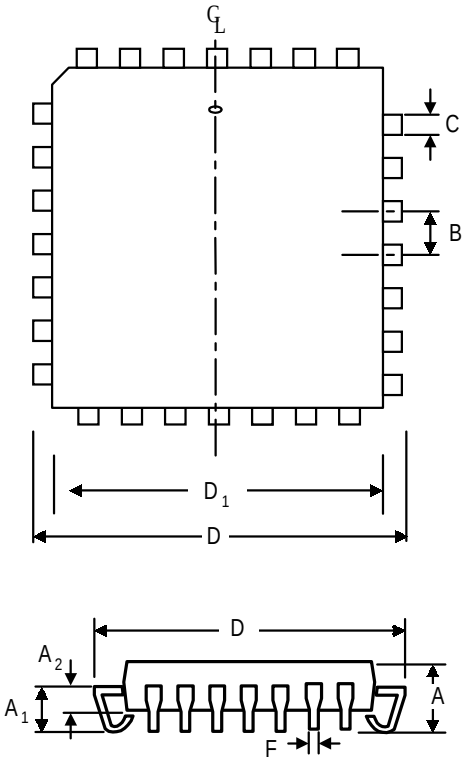


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	–	0.210	–	5.334
A2	0.115	0.195	2.921	4.953
b	0.014	0.022	0.356	0.559
b2	03045	0.070	1.143	1.778
D	0.735	0.775	18.669	19.685
E	0.300	0.325	7.620	8.255
E1	0.240	0.280	6.096	7.112
e	0.100 BSC[1] (nominal)		2.540 BSC[1] (nominal)	
eA	0.300 BSC[1] (nominal)		7.620 BSC[1] (nominal)	
eB	–	0.430	–	10.922
L	0.115	0.150	2.921	3.810

1. BSC—Basic Spacing between Centers

28-Pin PLCC

- Part Number LXP610PE
- Extended Temperature Range (-40 °C to 85 °C)



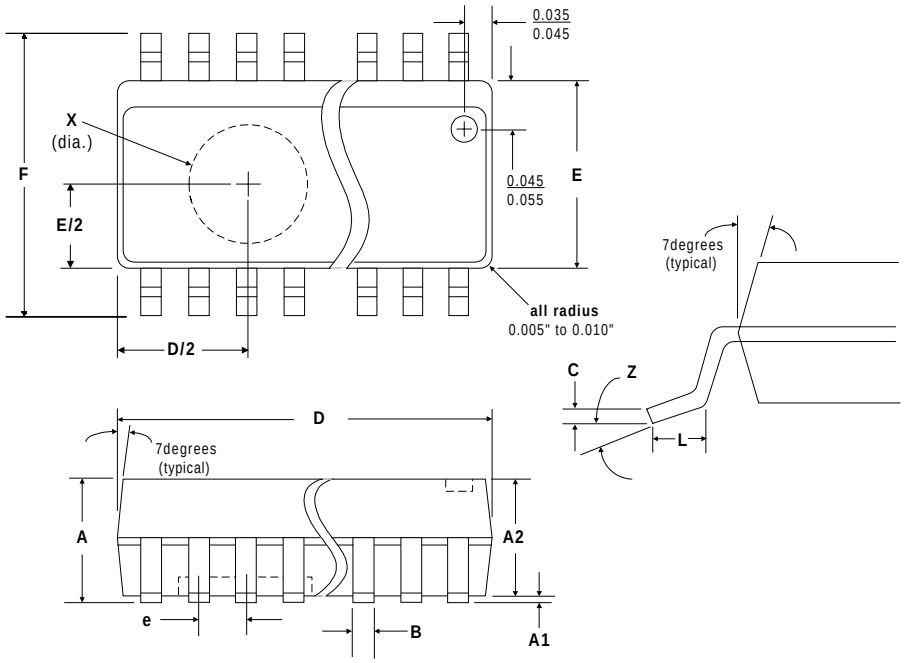
Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers

Figure 13: LXP610SE Package Specifications

16 Pin SOIC

- Part Number LXP610SE
- Extended Temperature Range (-40 °C to 85 °C)



Dim	Inches			Millimeters		
	Min	Nom	Max	Min	Nom	Max
A	0.093	0.099	0.104	2.362	2.515	2.642
A1	0.004	0.008	0.0115	0.102	0.203	0.292
A2	0.088	0.094	0.100	2.235	2.388	2.54
B	0.013	0.016	0.020	0.33	0.406	0.508
C	0.0091	0.010	0.0125	0.231	0.254	0.317
D	0.398	0.405	0.412	10.109	10.287	10.465
E	0.292	0.296	0.299	7.417	7.518	7.595
e	0.0508 B.S.C. (nominal)			1.27 B.S.C. (nominal)		
F	0.394	0.402	0.419	10.008	10.211	10.643
L	0.016	0.033	0.050	0.406	0.838	1.27
X	0.114	0.118	0.122	2.90	3.00	3.10
Z	0°	5°	8°	0°	5°	8°

1. BSC—Basic Spacing between Centers

Corporate Headquarters

9750 Goethe Road
Sacramento, California 95827
Telephone: (916) 855-5000
Fax: (916) 854-1101
Web: www.level1.com

LEVEL ONE™
an Intel company

The Americas

EAST

Eastern Area Headquarters & Northeastern Regional Office
234 Littleton Road, Unit 1A
Westford, MA 01886
USA
Tel: (978) 692-1193
Fax: (978) 692-1124

North Central Regional Office
One Pierce Place
Suite 500E
Itasca, IL 60143
USA
Tel: (630) 250-6044
Fax: (630) 250-6045

Southeastern Regional Office
4020 WestChase Blvd
Suite 100
Raleigh, NC 27607
USA
Tel: (919) 836-9798
Fax: (919) 836-9818

WEST

Western Area Headquarters
3375 Scott Blvd., #110
Santa Clara, CA 95054
USA
Tel: (408) 496-1950
Fax: (408) 496-1955

South Central Regional Office
2340 E. Trinity Mills Road
Suite 306
Carrollton, TX 75006
USA
Tel: (972) 418-2956
Fax: (972) 418-2985

Southwestern Regional Office
28202 Cabot Road
Suite 300
Laguna Niguel, CA 92677
USA
Tel: (949) 365-5655
Fax: (949) 365-5653

Latin/South America
9750 Goethe Road
Sacramento, CA 95827
USA
Tel: (916) 855-5000
Fax: (916) 854-1102

International

ASIA/PACIFIC

Asia / Pacific Area Headquarters
101 Thomson Road
United Square #08-01
Singapore 307591
Thailand
Tel: +65 353 6722
Fax: +65 353 6711

Central Asia/Pacific Regional Office
Suite 305, 4F-3, No. 75,
Hsin Tai Wu Road
Sec. 1, Hsi-Chih,
Taipei County, Taiwan
Tel: +886 22 698 2525
Fax: +886 22 698 3017

Northern Asia/Pacific Regional Office
Nishi-Shinjuku, Mizuma Building 8F
3-3-13, Nishi-Shinjuku,
Shinjuku-Ku
Tokyo, 160-0023 Japan
Tel: +81 3 3347-8630
Fax: +81 3 3347-8635

EUROPE

European Area Headquarters
Parc Technopolis-Bat. Zeta 3,
avenue du Canada -
Z.A. de Courtaboeuf
Les Ulis Cedex 91974
France
Tel: +33 1 64 86 2828
Fax: +33 1 60 92 0608

Central and Southern Europe Regional Office
"Regus"
Feringastrasse 6
D-85774 Muenchen-
Unterfoerhring, Germany
Tel: +49 89 99 216 375
Fax: +49 89 99 216 319

Northern Europe Regional Office
Torshamnsgatan 35
164/40 Kista/Stockholm,
Sweden
Tel: +46 8 750 3980
Fax: +46 8 750 3982

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