

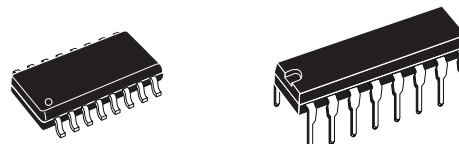
# PWM POWER MOS CONTROLLER

- HIGH EFFICIENCY DUE TO PWM CONTROL AND POWERMOS DRIVER
- LOAD DUMP PROTECTION
- LOAD POWER LIMITATION
- EXTERNAL POWERMOS PROTECTION
- LIMITED OUTPUT VOLTAGE SLEW RATE

### DESCRIPTION

The L9610C/11C is a monolithic integrated circuit working in PWM mode as controller of an external powerMOS transistor in High Side Driver configuration.

Features of the device include controlled slope of the leading and trailing edge of the gate driving voltage, linear current limiting with protection timer, settable switching frequency  $f_o$ , TTL compatible enable function, protection status output pin. The device is mounted in SO16 micropackage, and DIP16 package.

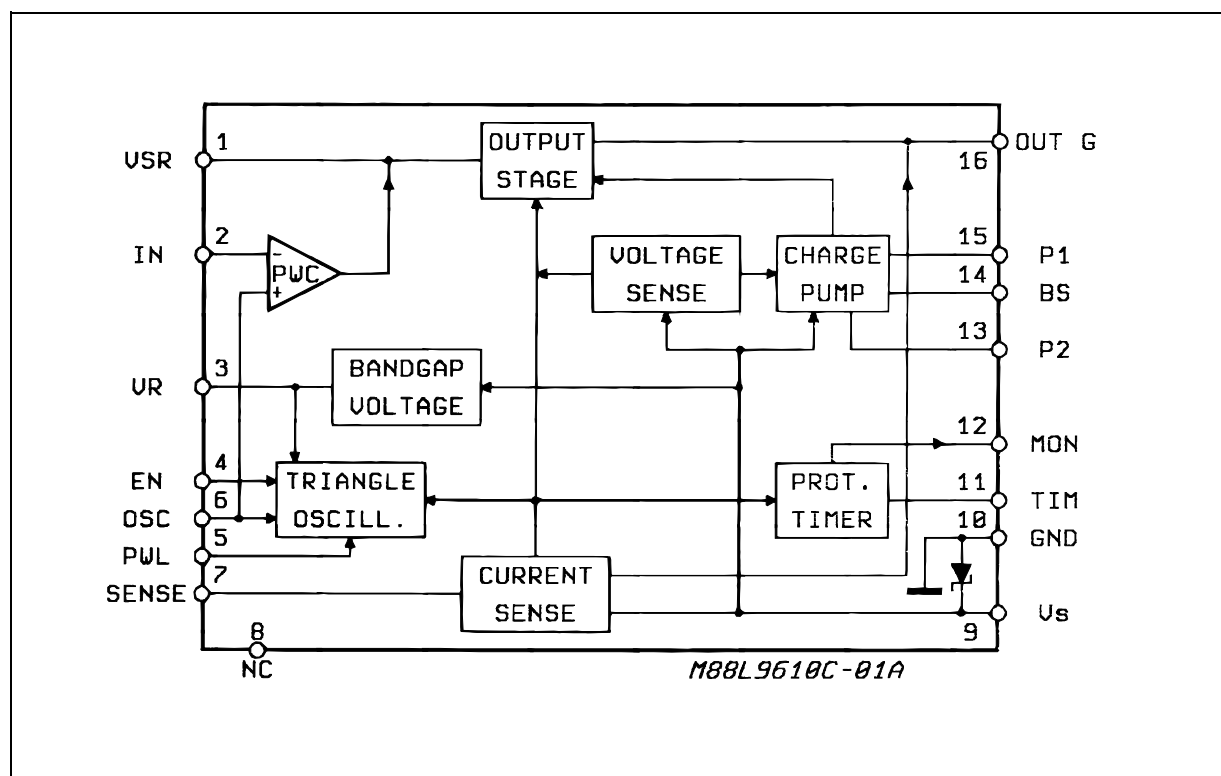


SO16

DIP16

**ORDERING NUMBERS:** L9610C  
L9611C

### BLOCK DIAGRAM



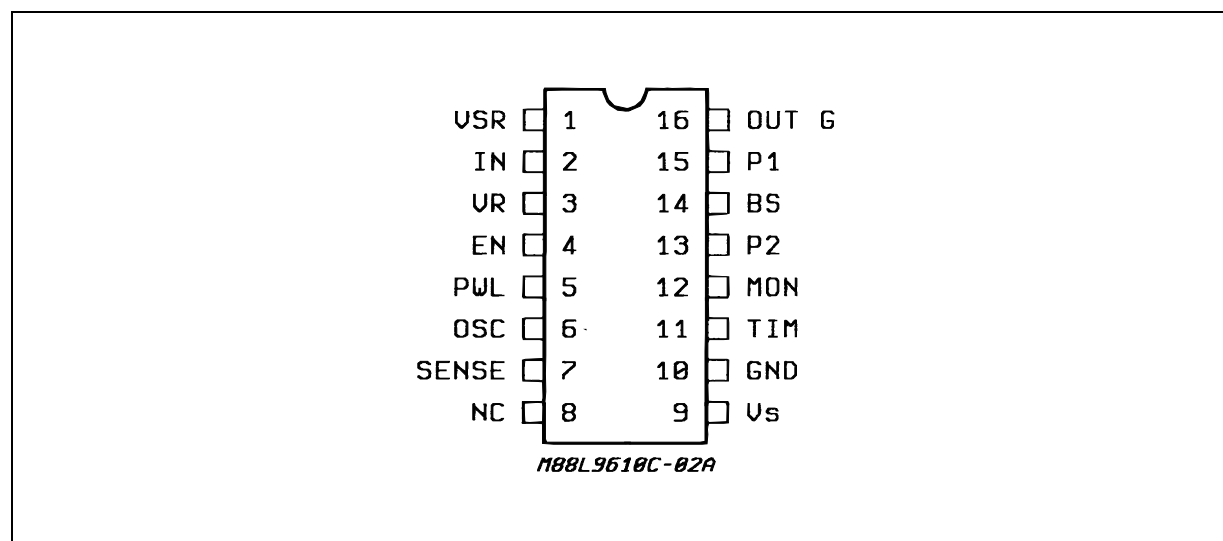
## ABSOLUTE MAXIMUM RATINGS

| Symbol               | Parameter                                                                                                                                  | Value                              | Unit |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|------|
| $V_S$                | Max. Supply Voltage                                                                                                                        | 26                                 | V    |
|                      | Transient Peak Supply Voltage ( $R_1 \geq 100\Omega$ ):                                                                                    |                                    |      |
|                      | Load Dump:<br>$5\text{ms} \leq t_{\text{rise}} \leq 10\text{ms}$ ; $\tau_f$ Fall Time Constant = 100ms; $R_{\text{SOURCE}} \geq 0.5\Omega$ | 60                                 | V    |
|                      | Field Decay:<br>$5\text{ms} \leq t_{\text{fall}} \leq 10\text{ms}$ ; $\tau_r$ Rise Time Constant = 33ms; $R_{\text{SOURCE}} \geq 10\Omega$ | -80                                | V    |
|                      | Low Energy Spike: $t_{\text{rise}} = 1\mu\text{s}$ , $t_{\text{fall}} = 2\text{ms}$ , $R_{\text{SOURCE}} \geq 10\Omega$                    | $\approx 100$                      | V    |
| $I_S$                | Max. Supply Current ( $t < 300\text{ms}$ )                                                                                                 | 0.3                                | A    |
| $V_{\text{IN}}$      | Input Voltage                                                                                                                              | $-0.3 < V_{\text{IN}} < V_S - 2.5$ | V    |
| $T_J/T_{\text{stg}}$ | Junction and Storage Temperature Range                                                                                                     | - 55 to 150                        | °C   |

## THERMAL DATA

| Symbol                | Parameter                           | SO16 | DIP16 | Value |
|-----------------------|-------------------------------------|------|-------|-------|
| $R_{\text{th j-amb}}$ | Thermal Resistance Junction-alumina | Max  | 50    | 90    |
|                       |                                     |      |       | °C/W  |

## PIN CONNECTION (Top view)



## PIN FUNCTIONS

| Pin   | Name           | Functions                                                                                                                                                                     |
|-------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | INT            | A Capacitor Connected Between this Pin and Out <sub>G</sub> Defines the GATE Voltage Slew Rate.                                                                               |
| 2     | IN             | Analog Input Controlling the PWM Ratio. The operating range of the input voltage is 0 to V <sub>R</sub> .                                                                     |
| 3     | V <sub>R</sub> | Output of an Internal Voltage Reference                                                                                                                                       |
| 4     | EN             | TTL Compatible Input for Switching off the Output.                                                                                                                            |
| 5     | PWL            | If this Pin is Connected to GND and V <sub>S</sub> > 13 V, the Duty Cycle and the Frequency f <sub>o</sub> are Reduced : this Allows to Transfer a Costant Power to the Load. |
| 6     | Osc            | Current Sink and Source Stage Connection of a Triangle Oscillator with Definite Voltage Swing.                                                                                |
| 7     | IND            | Input of an Operational Amplifier for Short Current Sensing and Regulation.                                                                                                   |
| 8     | NC             | Not Connected.                                                                                                                                                                |
| 9     | V <sub>S</sub> | Common Supply Voltage Input                                                                                                                                                   |
| 10    | GND            | Common Ground Connection                                                                                                                                                      |
| 11    | TIM            | A Capacitor Connected Between this Pin and GND Defines the Protection Delay Time.                                                                                             |
| 12    | MON            | Open Collector Monitoring Output off the PowerMOS Protection.                                                                                                                 |
| 13,15 | P2, P1         | Connection for the Charge Pump Capacitor.                                                                                                                                     |
| 14    | BS             | The Capacitor Connected Between thisPin and theSource of the Power MOS Allows to Bootstrap the Gate Driving Voltage.                                                          |
| 16    | Out G          | Output for Driving the Gate of the External PowerMOS.                                                                                                                         |

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$  ;  $6\text{ V} < V_S < 16\text{ V}$  unless otherwise specified)

| Symbol       | Parameter                       | Test Conditions                 | Min. | Typ. | Max. | Unit             |
|--------------|---------------------------------|---------------------------------|------|------|------|------------------|
| $V_S$        | Operating Supply Voltage        |                                 | 6    |      | 16   | V                |
| $I_q$        | Quiescent Current               |                                 |      | 2.5  | 6    | mA               |
| $V_{SC}$     | Internal Supply Voltage Clamp   | $I_S = 200\text{ mA}$           | 28   | 32   | 36   | V                |
| $V_{SH}$     | Supply Voltage High Threshold   |                                 | 16   | 18.5 | 21   | V                |
| $V_{SL}$     | Supply Voltage Low Threshold    |                                 | 4    | 5    | 6    | V                |
| $V_R$        | Reference Voltage               |                                 | 3.3  | 3.5  | 3.7  | V                |
| $I_R$        | Reference Current               | $\Delta V_R \leq 100\text{ mV}$ |      |      | 1    | mA               |
| $V_{INL}$    | Input Low Threshold             |                                 | 0.13 | 0.15 | 0.2  | $V_{IN}/V_R$     |
| $K_F$        | Oscillator Freq. Constant       | Note 1                          | 800  |      | 2500 | nF/s             |
| $K_S$        | Gate Voltage Slew Rate Constant | Note 2                          | 3    | 5    | 9    | nFV/ms           |
| $K_T$        | Protection Time Delay Constant  | Note 3                          | 0.12 |      | 0.44 | ms/nF            |
| $V_{Si}$     | Sense Input Volt.               |                                 | 80   | 100  | 120  | mV               |
| $V_{GON}$    | Gate Driving Volt. above $V_S$  | $V_S = 16\text{ V}$             | 8    |      | 16   | V                |
| $V_{GOFF}$   | Gate Voltage in OFF Condition   | $I_G = 100\text{ }\mu\text{A}$  |      |      | 1.2  | V                |
| $I_{IN}$     | Input Current                   |                                 | - 5  | - 1  |      | $\mu\text{A}$    |
| $V_{ENL}$    | Low Enable Voltage              |                                 |      |      | 0.8  | V                |
| $V_{ENH}$    | High Enable Voltage             |                                 | 2.0  |      |      | V                |
| $I_{EN}$     | Enable Input Current            |                                 |      |      | 2    | $\mu\text{A}$    |
| $SR$         | Slew Rate                       | Without $C_S$                   |      | 0.5  |      | V/ $\mu\text{s}$ |
| $V_{MONsat}$ | Saturation Voltage (pin 12)     | $I_{MON} = 2.5\text{ mA}$       |      |      | 1.5  | V                |

- Notes :**
1.  $f_0 = K_F/C_F$ .
  2.  $dV_G/dt = K_S/C_S$ .
  3.  $t_{prot} = K_T \cdot C_T$ .

**FUNCTIONAL DESCRIPTION**
**PULSE WIDTH COMPARATOR**

A ground compatible comparator generates the PWM signal which controls the gate of the external powerMOS.

The slopes of the leading and trailing edges of the gate driving signal are defined by the external capacitor  $C_S$  according to :

$$dV_G/dt = K_S/C_S$$

This feature allows to optimize the switching speed for the power and RFI performance best suited for the application.

The lower limit of the duty cycle is fixed at 15 % of the ratio between the input and the reference voltage (see fig. 1). Input voltages lower than this value disable the internal oscillator signal and therefore the gate driver.

**GROUND COMPATIBLE TRIANGLE OSCILLATOR**

The triangle oscillator provides the switching frequency  $f_0$  set by the external capacitor  $C_F$  according to :

$$f_0 = K_F/C_F$$

If the pin PWL (power limitation) is connected to ground and  $V_S$  is higher than the PWL threshold voltage, the duty cycle and the  $f_0$  frequency are reduced : this allows to transfer a constant power to the load (see fig. 2).

**TIMER AND PROTECTION LATCH**

When an overcurrent occurs, the device starts charging the external capacitor  $C_T$  ; the protection time is set according to :

$$t_{prot} = K_T \cdot C_T$$

After the overcurrent protection time is reached, the powerMOS is switched-off ; this condition is latched by setting an internal flip-flop and is externally monitored by the low state of the MON pin.

To reset the latch the supply voltage has to fall below  $V_{SL}$  or the device must be switched off.

#### UNDER AND OVERVOLTAGE SENSE WITH LOAD DUMP PROTECTION

The undervoltage detection feature resets the timer and switches off the output driving signal when the supply voltage is less than  $V_{SL}$ .

If the supply voltage exceeds the max operating supply voltage value, an internal comparator disables the charge pump, the oscillator and the external powerMOS.

In both cases the thresholds are provided with suitable hysteresis values.

The load dump protection function allows the device to withstand - for a limited time - high overvoltages. It consists of an active clamping diode which limits the circuit supply voltage to  $V_{CLAMP}$  and an external current limiting resistor  $R_1$ . The maximum pulse supply current (see abs. max. ratings) is equal to 0.3A. Therefore the maximum load dump voltage is given by :

$$V_{DUMP} = V_{SC} + 0.3R_1$$

In this condition the gate of the powerMOS is held at the GND pin potential and thus the load voltage is :

$$V_L = V_S - V_{CLAMP} - V_{GS}$$

**Figure 1 : Typical Transfer Curve.**

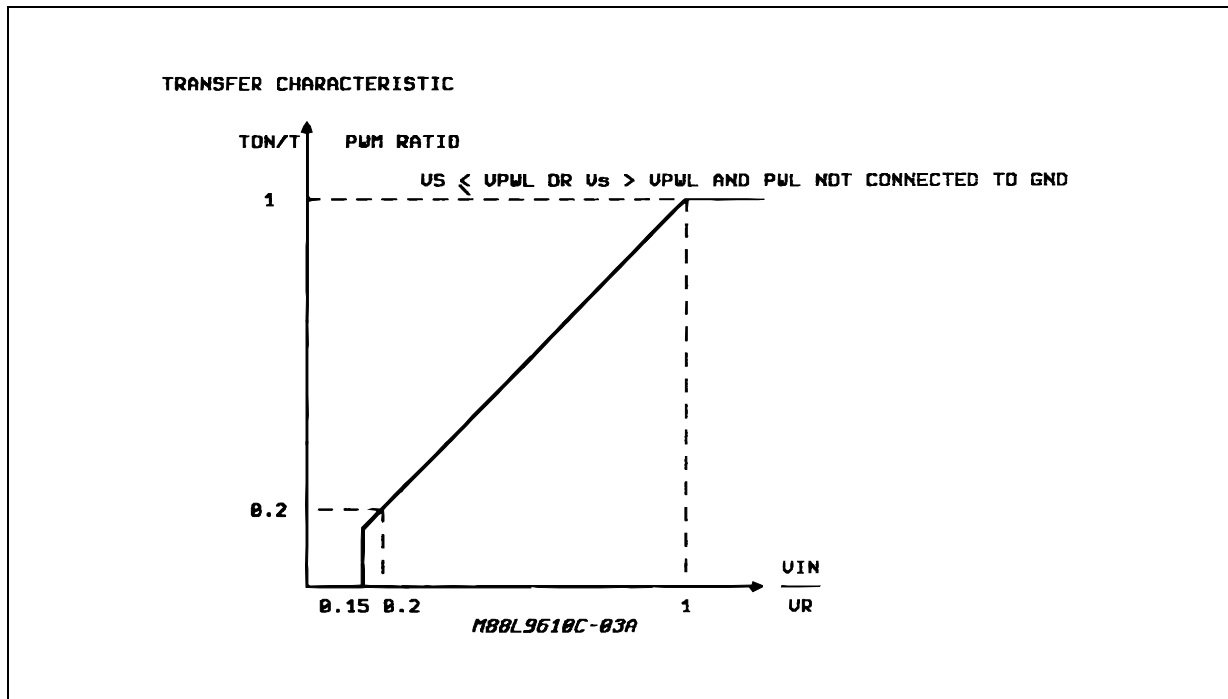
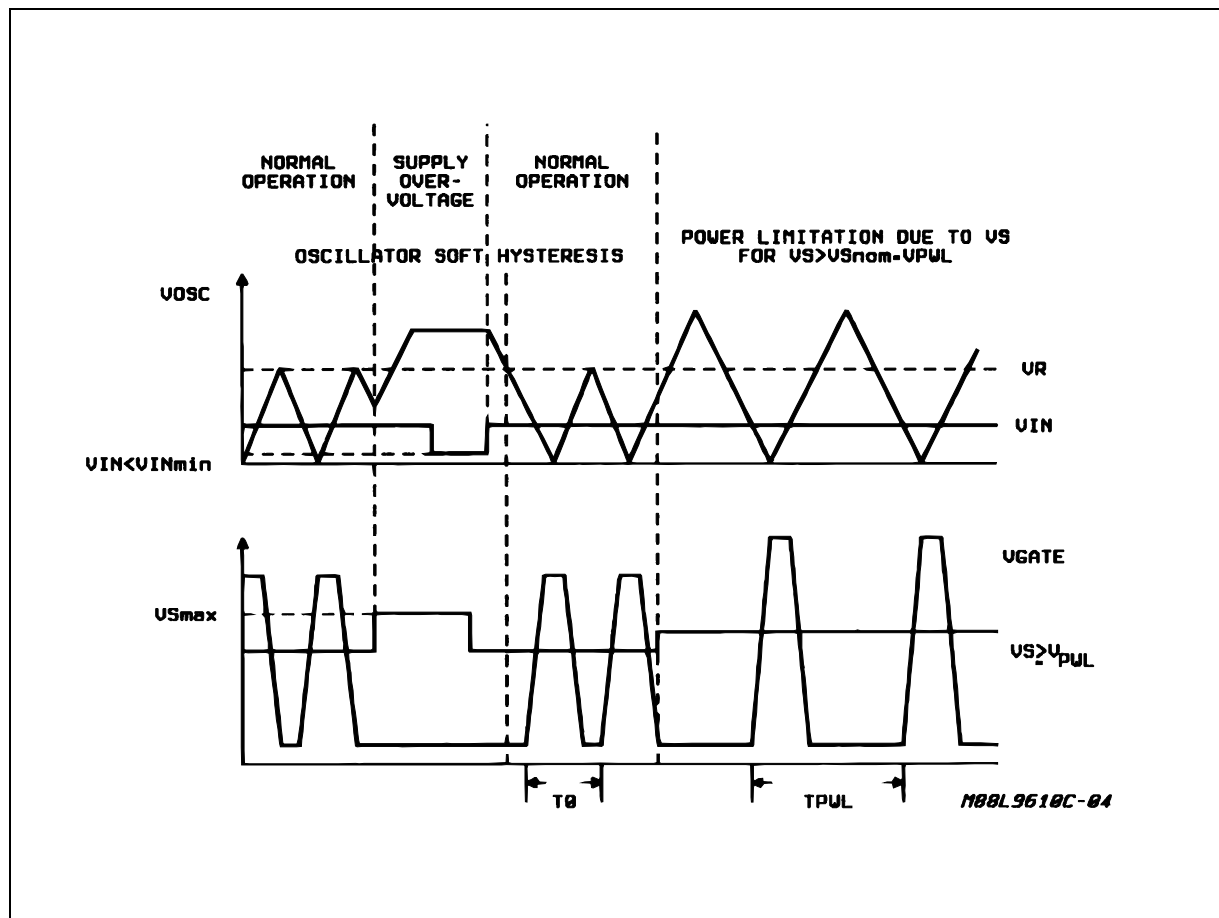


Figure 2 : The Typical Waveforms for the Power Limitation Function.



#### SHORT CIRCUIT CURRENT REGULATION

The maximum load current in the short circuit condition can be chosen by the value of the current sensing resistor  $R_S$  according to :

$$I_{sc} = V_{SI}/R_S$$

Two identical  $V_S$  compatible comparators are provided to realize the short circuit protection.

After reaching the lower threshold voltage (typical value  $V_{SI}$ -10 mV), the first comparator enables the timer and the gate is driven with the full continuous pump voltage : when the upper threshold voltage value is reached the second comparator maintains the chosen  $I_{sc}$  driving the NMOS gate in continuous mode.

This function - showed in fig. 3 - speeds up the switch on phase for a lamp as a load.

#### BANDGAP VOLTAGE REFERENCE

The circuit provides a reference voltage which may

be used as control input voltage through a resistive divider. This reference is protected against the short circuit current.

#### CHARGE PUMP

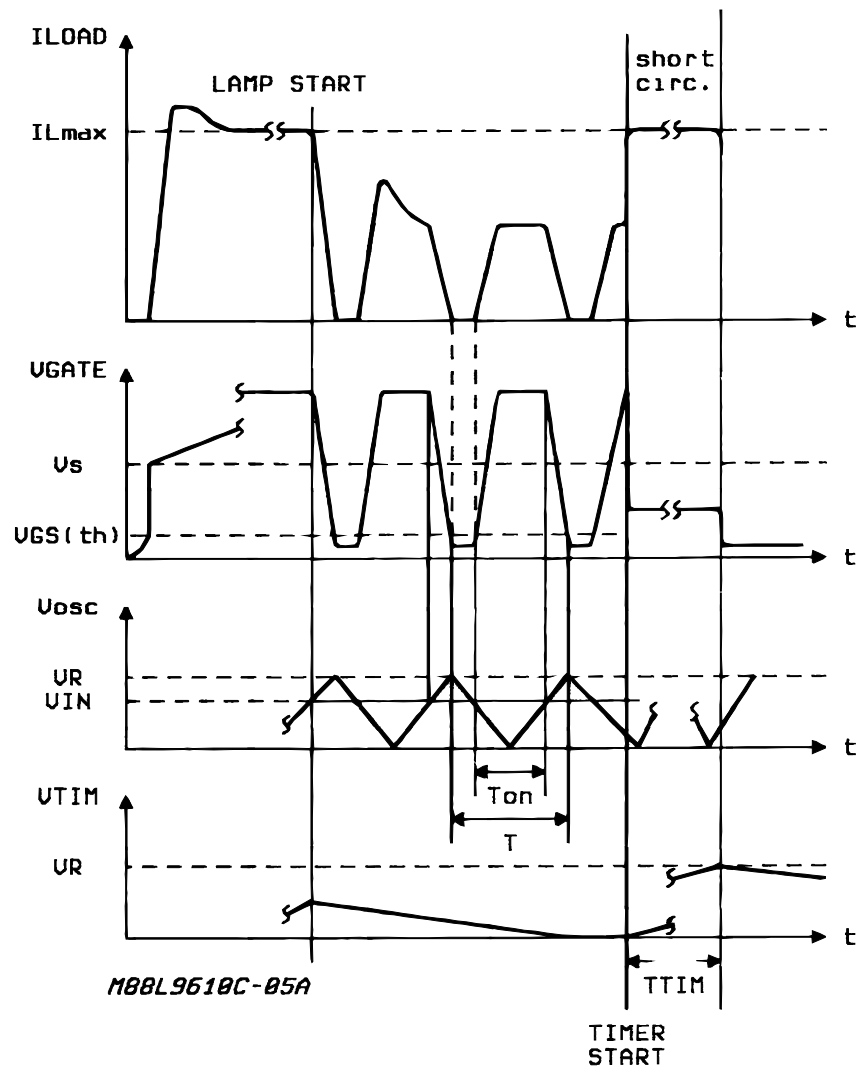
The charge pump circuit holds the N-MOS gate above the supply voltage during the ON phase. This circuit consists of an RC astable which drives a comparator with a push-pull output stage. The external charge pump capacitor  $C_P$  must be at least equal to the NMOS parasitic input capacitance.

For fast gate voltage variation  $C_P$  must be increased or the bootstrap function can be used. The bootstrap capacitor should be at least 10 times greater than the powerMOS parasitic capacitance.

The charge pump voltage  $V_{PUMP}$  can reach to :

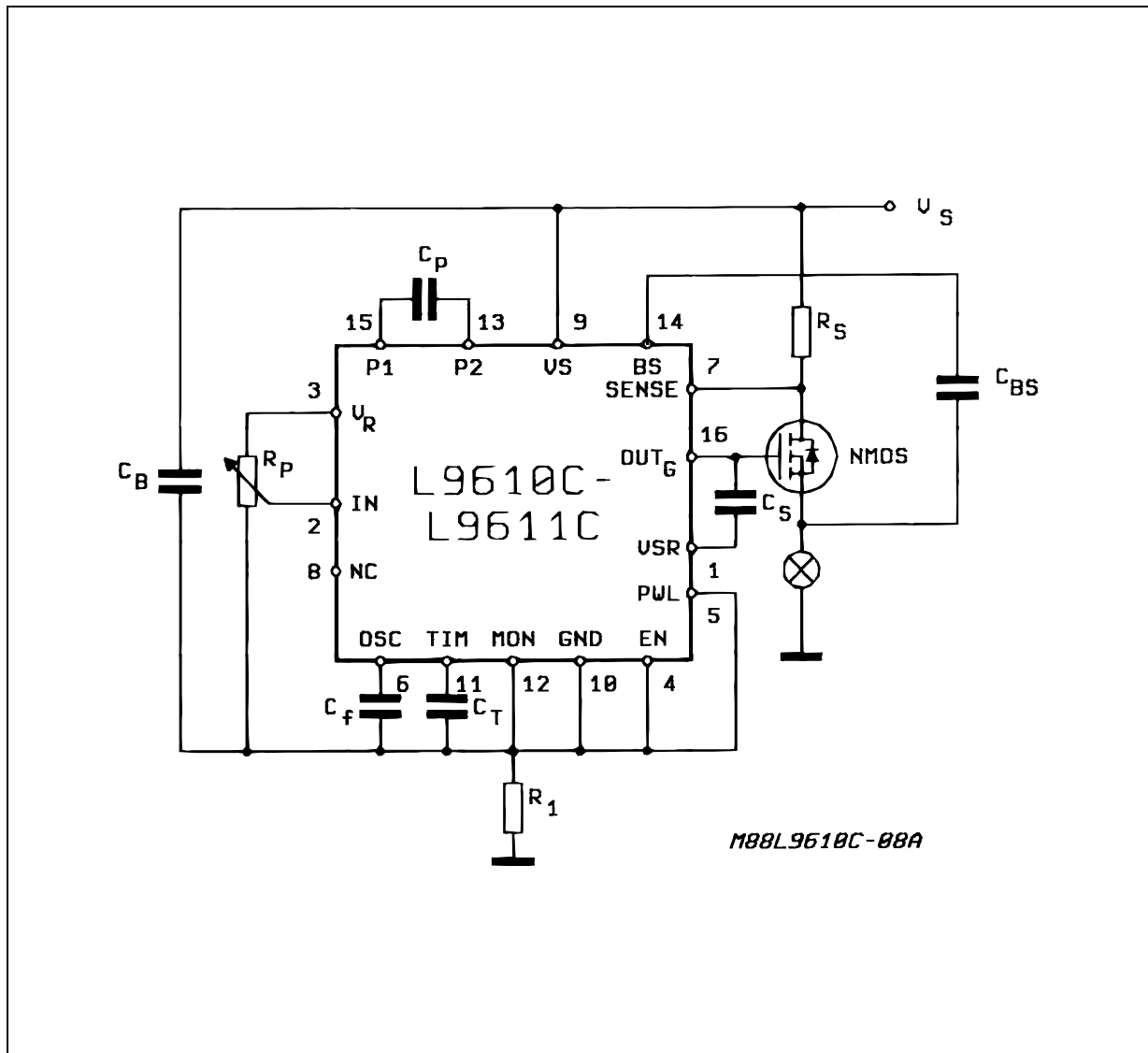
$$V_{PUMP} = 2 V_S - V_{BE} - V_{CESAT}$$

The circuit is disabled if the supply voltage is higher than  $V_{SH}$ .

**Figure 3 :** The Typical Waveforms for Short Circuit Current Condition.

# APPLICATION CIRCUIT

Figure 4.



**Note :** All node voltages are referred to ground pin (GND)

The currents flowing in the arrow direction are assumed positive

without C<sub>BS</sub> : C<sub>P</sub> = 1nF

without C<sub>BS</sub> : C<sub>BS</sub> must be at least 10 times higher than the gate capacitance : C<sub>P</sub> = 100 pF.

## CONTROLLING A 120W HALOGEN LAMP WITH THE L9610C/11C DIMMER

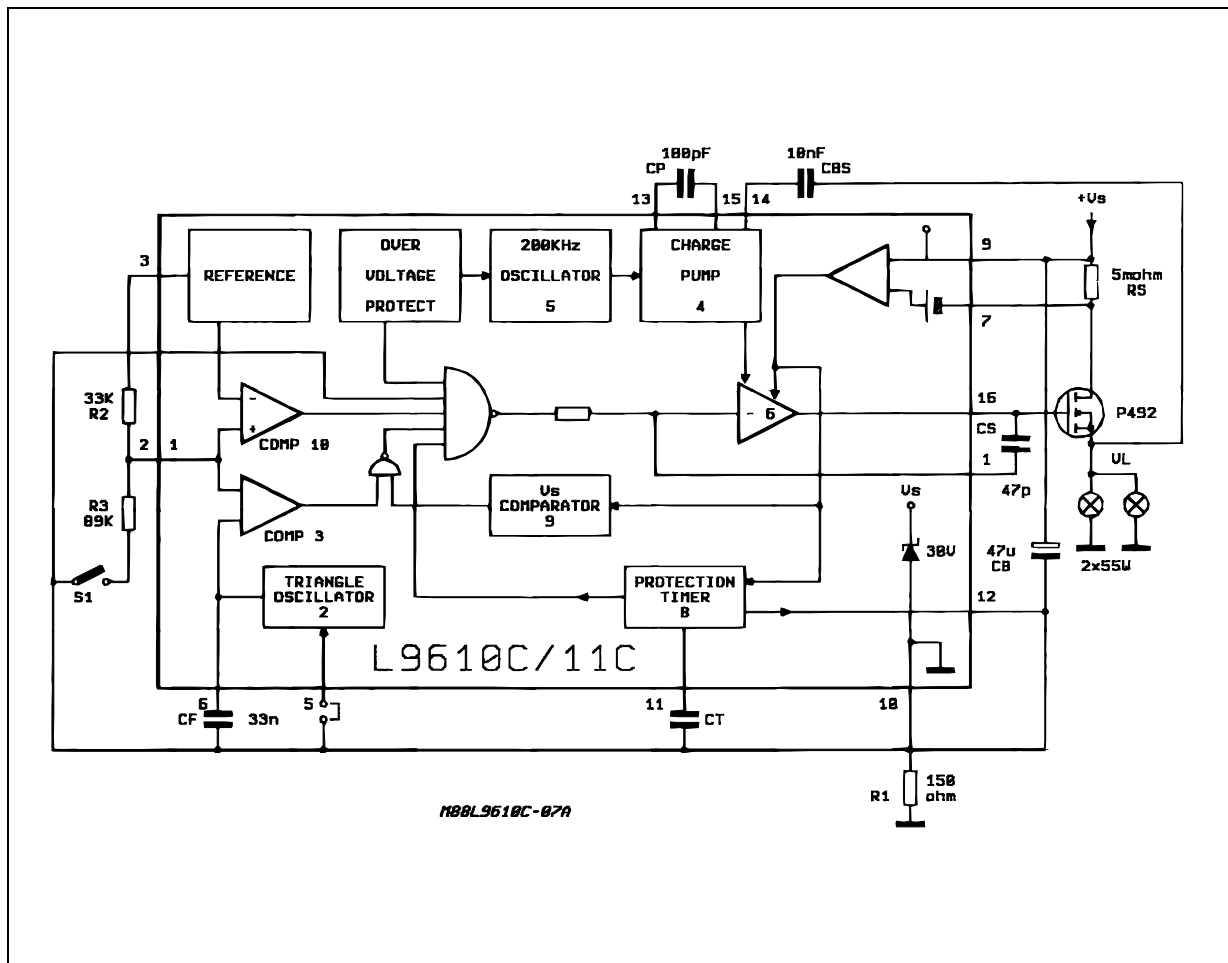
The L9610C/11C Lamp Dimmer is used to control the brightness of vehicle headlamps using H4 type lamps (see fig. 5). With switch S1 open the full supply voltage is applied to the lamps : closing the

switch it is a possible to reduce the average lamp voltage as desired :

$$V_L = V_S \frac{R_3}{R_2 + R_3}$$

If pin 5 is connected to ground the average lamp voltage is constant, even for supply voltages in excess of 13 V.

Figure 5 : Application Circuit.



The sensing resistor  $R_S$  and timing capacitor  $C_t$  should be dimensioned according to :

$$R_S = \frac{V_{Si}}{2I_{nom}} (@V_S=14V)$$

$$C_t = \frac{2 \times \text{limitation time}}{K_T}$$

In normal conditions ( $V_{CC} = 14V$ , maximum brightness) the voltage drop across the sense resistor must be 50 mV. The current limiter intervenes at twice the nominal current,  $I_{nom}$ .

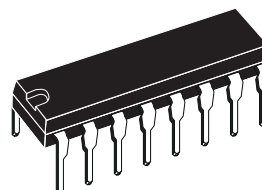
The timing capacitor  $C_t$  ( $V_{ct} = 3.5V$ ) must be chosen so that the delay before intervention is twice the duration of the current limitation at power-on.

The optimal value of the oscillator frequency, taking tolerances into account, must be slightly higher than the frequency at which lamp flicker is noticeable (min 60 Hz).

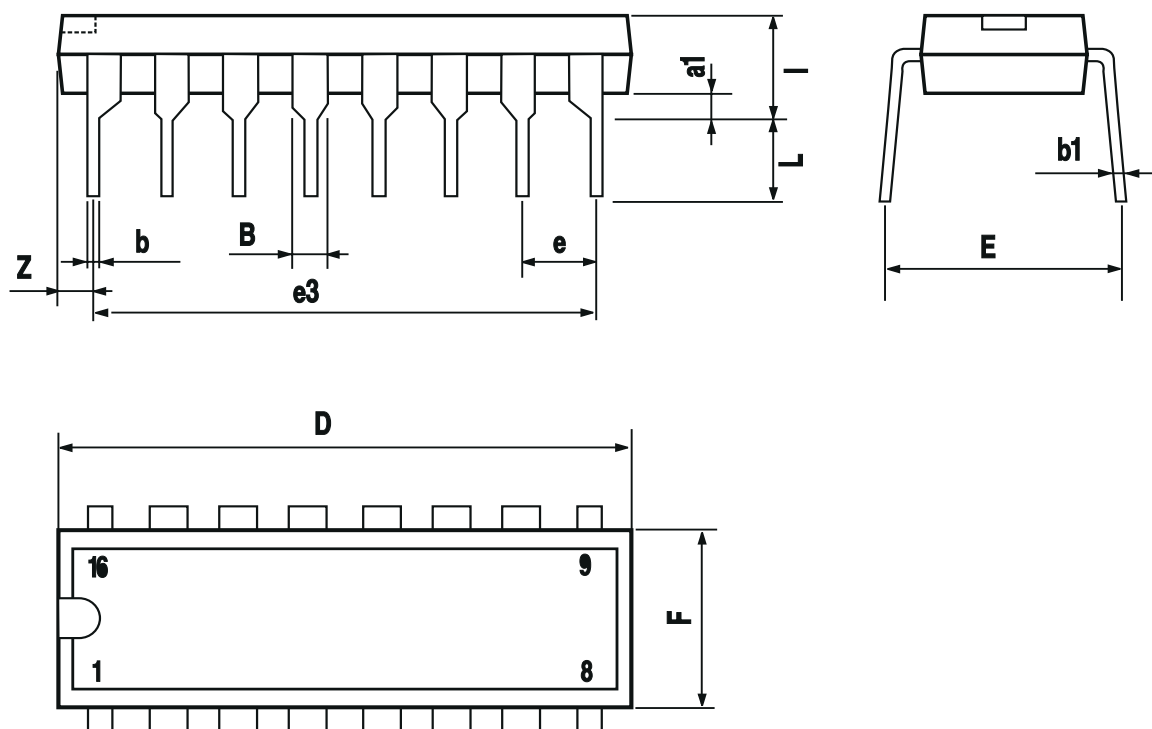
The switching times are a compromise between possible EMI and switching power losses. The recommended value for  $C_s$  is 47pF.

| DIM. | mm   |       |      | inch  |       |       |
|------|------|-------|------|-------|-------|-------|
|      | MIN. | TYP.  | MAX. | MIN.  | TYP.  | MAX.  |
| a1   | 0.51 |       |      | 0.020 |       |       |
| B    | 0.77 |       | 1.65 | 0.030 |       | 0.065 |
| b    |      | 0.5   |      |       | 0.020 |       |
| b1   |      | 0.25  |      |       | 0.010 |       |
| D    |      |       | 20   |       |       | 0.787 |
| E    |      | 8.5   |      |       | 0.335 |       |
| e    |      | 2.54  |      |       | 0.100 |       |
| e3   |      | 17.78 |      |       | 0.700 |       |
| F    |      |       | 7.1  |       |       | 0.280 |
| I    |      |       | 5.1  |       |       | 0.201 |
| L    |      | 3.3   |      |       | 0.130 |       |
| Z    |      |       | 1.27 |       |       | 0.050 |

## OUTLINE AND MECHANICAL DATA

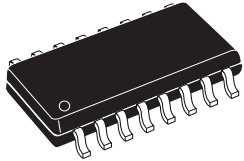


**DIP16**



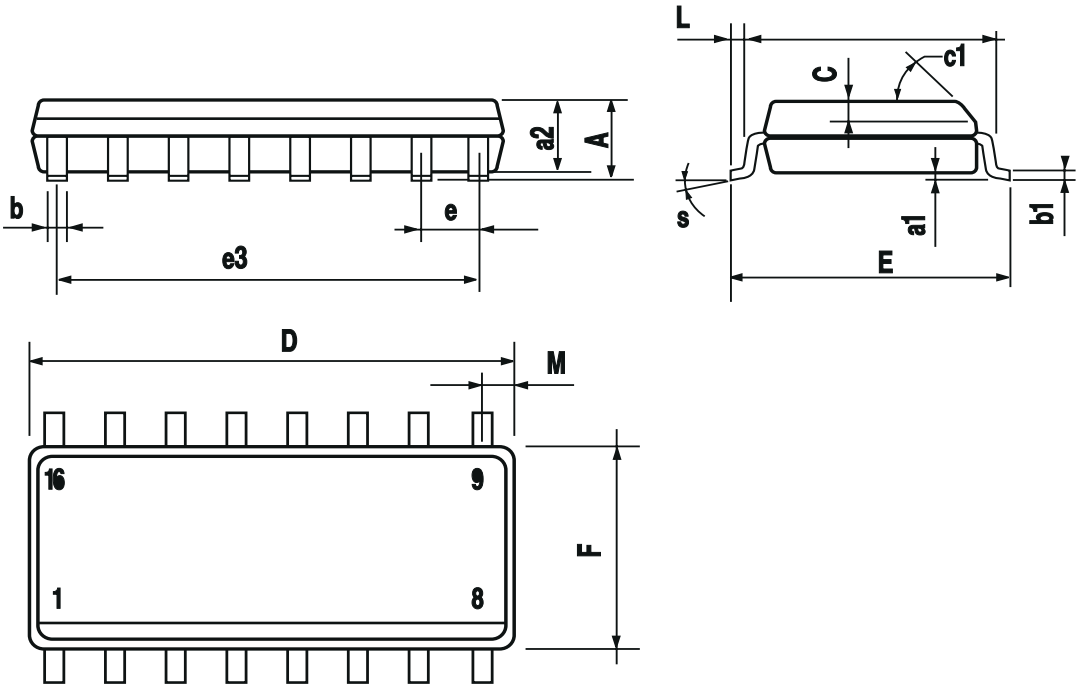
| DIM.  | mm         |      |      | inch  |       |       |
|-------|------------|------|------|-------|-------|-------|
|       | MIN.       | TYP. | MAX. | MIN.  | TYP.  | MAX.  |
| A     |            |      | 1.75 |       |       | 0.069 |
| a1    | 0.1        |      | 0.25 | 0.004 |       | 0.009 |
| a2    |            |      | 1.6  |       |       | 0.063 |
| b     | 0.35       |      | 0.46 | 0.014 |       | 0.018 |
| b1    | 0.19       |      | 0.25 | 0.007 |       | 0.010 |
| C     |            | 0.5  |      |       | 0.020 |       |
| c1    | 45° (typ.) |      |      |       |       |       |
| D (1) | 9.8        |      | 10   | 0.386 |       | 0.394 |
| E     | 5.8        |      | 6.2  | 0.228 |       | 0.244 |
| e     |            | 1.27 |      |       | 0.050 |       |
| e3    |            | 8.89 |      |       | 0.350 |       |
| F (1) | 3.8        |      | 4    | 0.150 |       | 0.157 |
| G     | 4.6        |      | 5.3  | 0.181 |       | 0.209 |
| L     | 0.4        |      | 1.27 | 0.016 |       | 0.050 |
| M     |            |      | 0.62 |       |       | 0.024 |
| S     | 8° (max.)  |      |      |       |       |       |

OUTLINE AND  
MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



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