ISLIC™

Intelligent Subscriber Line Interface Circuit
Le79R251 device

APPLICATIONS

- **Provides a cost-effective voice solution for long loop applications providing POTS and integrated test capabilities.**
  - — CO
  - — DLC
  - — PBX/KTS
  - — Pair Gain

FEATURES

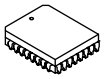
- **Monitor of two-wire interface voltages and currents supports**
  - — Voice transmission
  - — Through chip ring generation
  - — Programmable DC feed characteristics
    - – Independent of battery
    - – Current limited
  - — Selectable off-hook and ground-key thresholds
  - — Subscriber line diagnostics
    - – Leakage and Loop resistance
    - – Line capacitance and Bell
    - – Foreign voltage sensing
  - — Power cross and fault detection
- **Integrates through chip ringing**
  - — High voltage operation supports long loops
  - — Provides the highest ringing capability in Legerity's Intelligent Access Voice family.
- **Dual battery operation for system power saving**
  - — Automatic high/low battery switching
  - — Intelligent thermal management
  - — +5 V and battery voltages required
- **Compatible with inexpensive protection networks**
  - — Maintains longitudinal balance with low tolerance fuse resistors or PTC thermistors
- **Provides pulse metering**
  - — 12 kHz and 16 kHz
  - — Smooth polarity reversal
- **Tip-open state supports ground start signaling**
- **Integrated test load switches/relay drivers**
- **5 REN with 20 V DC offset trapezoid.**

  For US standard:
  - — drives ring up to 16.9 kft of 26 gauge wire.

  or
  - — drives ring up to 26.8 kft of 24 gauge wire.

  For European (British) standard:
  - — drives ring up to 6.5 km of 0.5 mm copper cable.

ORDERING INFORMATION



An ISLAC™ device must be used with this part.

Device	Package
Le79R251JC	32-pin PLCC

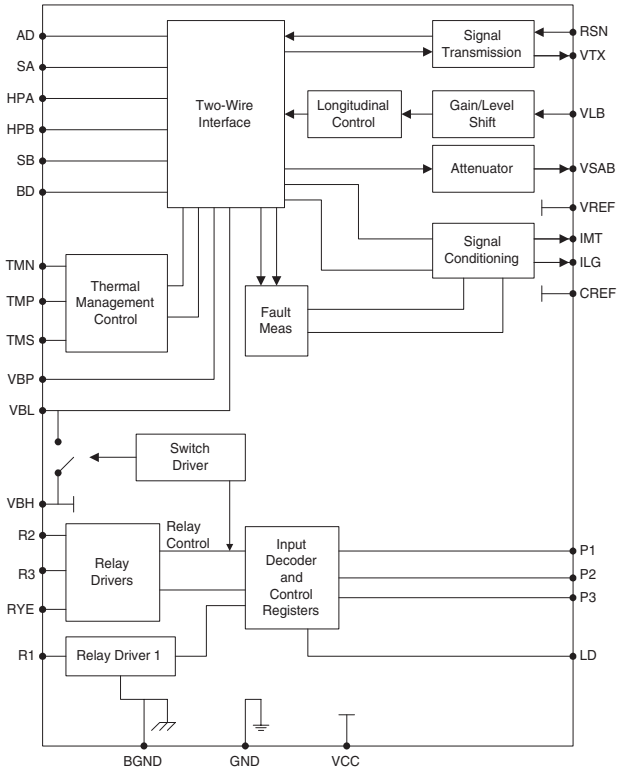
DESCRIPTION

The Le79R251 device, in combination with an ISLAC™ device, implements telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the ISLAC device. Le79R251 device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. Integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

RELATED LITERATURE

- **080274 Am79D2251 Dual ISLAC Data Sheet**
- **080250 Am79Q224x Quad ISLAC Data Sheet**
- **080345 Am79R2xx/Am79D2251 Technical Reference**
- **080344 Am79R2xx/Am79Q224x Technical Reference**

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

Legerity's Intelligent Access™ voice chipsets integrate all the functions of a subscriber line. Two chip types are used to implement the line card: an Le79R251 device and an ISLAC device. Current ISLAC devices include the following: 79Q2241, 79Q2242, 79Q2243, and 79D2251. These provide the following basic functions:

1. The Le79R251 device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The ISLAC device: A low voltage CMOS IC that provides conversion, control and DSP functions for the Le79R251 device.

A complete schematic of the line card using the Intelligent Access voice chipsets for internal ringing is shown in "Internal Ringing Line Card Schematic" on page 18.

The Le79R251 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling, enabling it to have full control over the subscriber loop. The Le79R251 device is designed to be used exclusively with the ISLAC devices, and requires only +5 V, 3.3 V battery supplies for its operation.

The Le79R251 device implements a linear loop-current feeding method with the enhancement of intelligent thermal management. This limits the amount of power dissipated on the Le79R251 device chip by dissipating power in external resistors in a controlled manner.

The ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice (codec), DC-feed and supervision signals. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chipset provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chipsets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge, and it allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Le79R251 device includes circuitry to report metallic voltages and longitudinal currents on Tip/Ring to the ISLAC device. These inputs allow the ISLAC device to place several key Le79R251 device performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic (IMT) and longitudinal (ILG) loop currents
- The AC (VTX) and DC (VSAB) loop voltage

The outputs supplied by the ISLAC device to the ISLIC device are then:

- A voltage (VHLi) that provides control for the following high-level ISLIC device outputs:
  - DC loop current
  - Internal ringing signal

  - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal (VOUTi)
- A voltage that controls longitudinal offset for test purposes (VLBi)

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software and loaded into the ISLAC device registers using the system microprocessor. The PCM codes can be either 16-bit linear, twos-complement, or 8-bit companded A-law or µ-law.

Besides the codec functions, the Intelligent Access voice chipset provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus (P1–P3) and tri-level load signal (LDi).

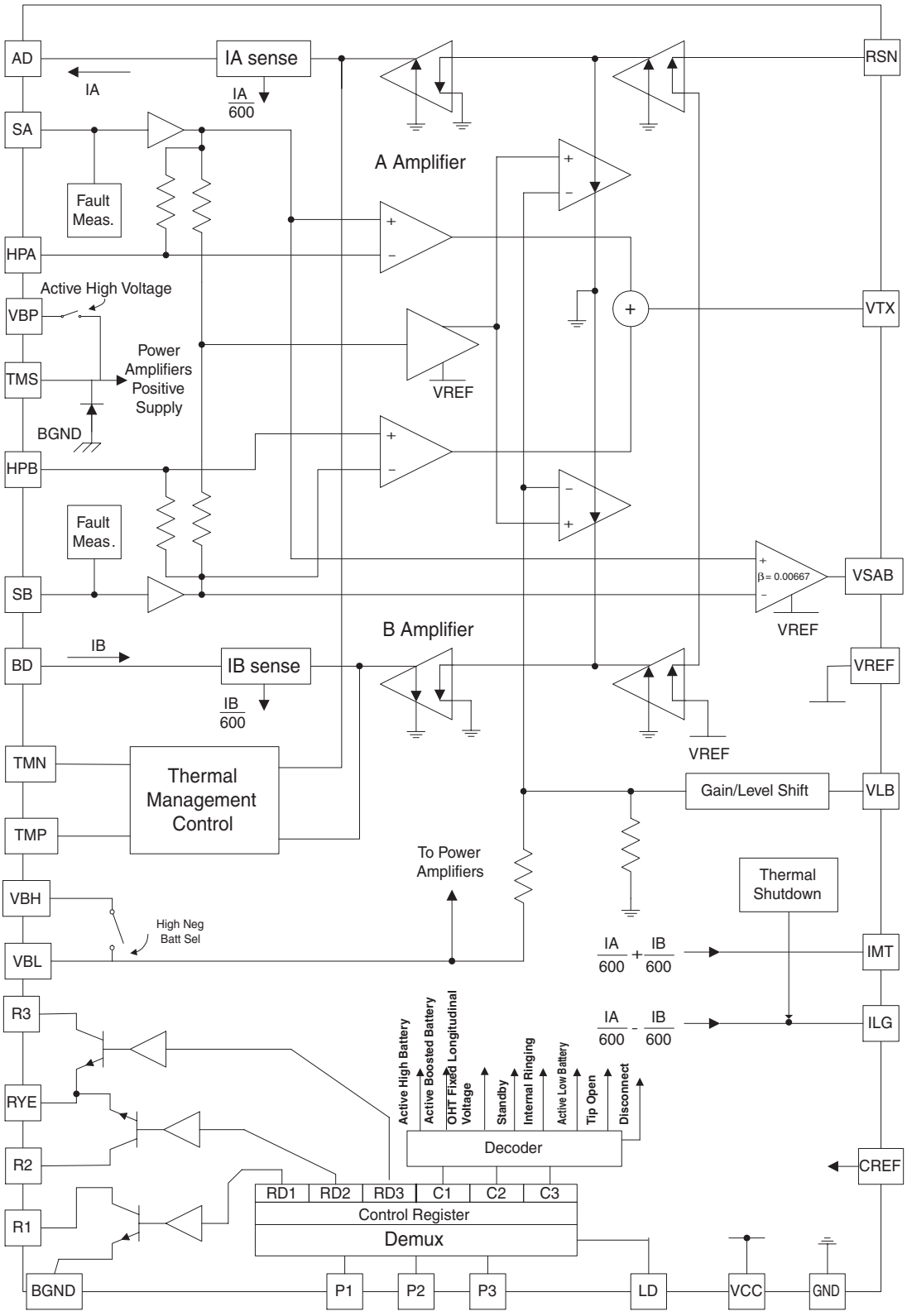
The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable and a programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit and the user can choose to send the measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and the number telephone ringers to be identified.

Note:

"i" denotes channel number.

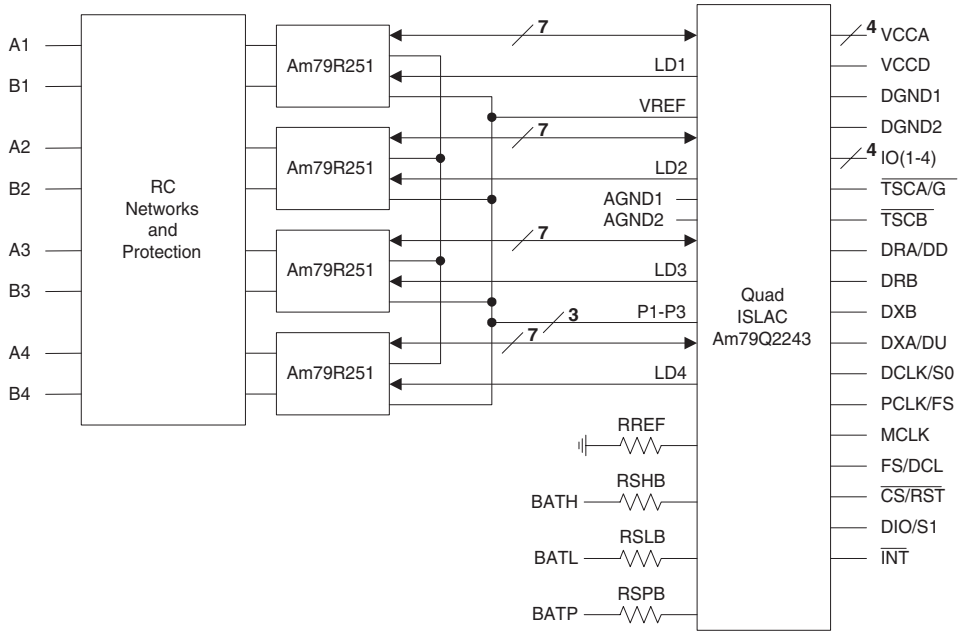
LE79R251 DEVICE INTERNAL BLOCK DIAGRAM



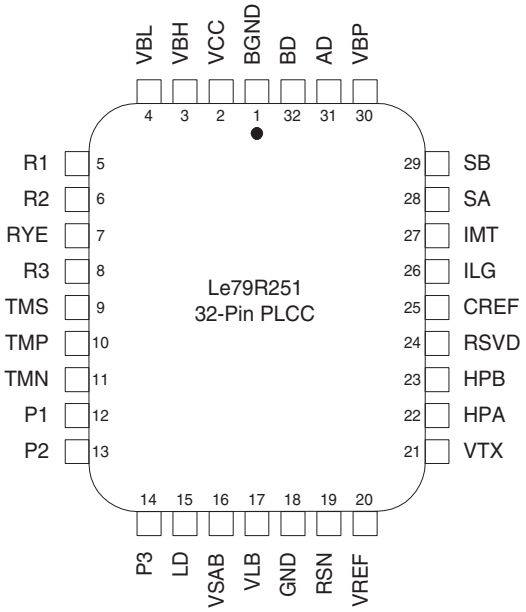
FEATURES OF THE INTELLIGENT ACCESS™ CHIPSET

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
    - Off-hook debounce circuit
    - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
- Supports internal and external battery-backed ringing
  - Self-contained ringing generation and control
  - Supports external ringing generator and ring relay
  - Ring relay operation synchronized to zero crossings of ringing voltage and current
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
  - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
  - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 5 V, 3.3 V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice-path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
  - Leakage
  - Line and ringer capacitance
  - Loop resistance
- Integrated self-test features
  - Echo gain, distortion, and noise
- Guaranteed performance over commercial and industrial temperature ranges.
- Up to three relay drivers per ISLIC™ device
  - Configurable as test load switches

CHIPSET BLOCK DIAGRAM - FOUR CHANNEL LINE CARD EXAMPLE



CONNECTION DIAGRAM



Note:

Pin 1 is marked for orientation.

RSVD = Reserved. Don not connect to this pin.

PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
AD, BD	A, B Line Drivers	O	Provide the currents to the A and B leads of the subscriber loop.
BGND	Ground		Ground return for high and low battery supplies.
CREF	+3.3 VDC		VCCD reference. It is the digital high logic supply rail, used by the ISLIC to ISLAC interface.
GND	Ground		Analog and digital ground return for VCC.
HPA, HPB	High-Pass Filter Capacitor	O	These pins connect to CHP, the external high-pass filter capacitor that separates the DC loop-voltage from the voice transmission path.
ILG	Longitudinal Current Sense	O	ILG is proportional to the common-mode line current (IAD – IBD), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT	Metallic Current Sense	O	IMT is proportional to the differential line current (IAD + IBD), except in disconnect mode, where IMT is proportional to the current into grounded SA.The Le79R251 device indicates thermal overload by pulling IMT to >2.8 V.
LD	Register Load	I	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 (CREF - 1), the logic levels on P1–P3 latch into the Le79R251 device control register bits that operate the mode-decoder. When the LD pin is a logic 0 (< 0.6 V), the logic levels on P1–P3 latch into the Le79R251 device control register bits that control the relay drivers (RD1–RD3). When the LD pin level is at ~V_{REF} ± 0.3 V the control register contents are locked.
P1–P3	Control Bus	I	Inputs to the latch for the operating-mode decoder and the relay-drivers.
R1	Relay 1 Driver	O	Collector connection for relay 1 driver. Emitter internally connected to BGND.
R2	Relay 2 Driver	O	Collector connection for relay 2 driver. Emitter internally connected to RYE
R3	Relay 3 Driver	O	Collector connection for relay 3 driver. Emitter internally connected to RYE.
RSN	Receive Summing Node	I	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD	Reserved		This is used during Legerity testing. In the application, this pin must be left floating.
RYE	Relay 2, 3 Common Emitter	O	Emitter connection for R2 and R3. Normally connected to relay ground.
SA, SB	A, B Lead Voltage Sense	I	Sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
TMP, TMN, TMS	Thermal Management		External resistors connected from TMP to TMS and TMN to VBL to offload excess power from the Le79R251 device.
VBH	Battery (Power)		Connection to high-battery supply used for ringing and long loops. Connects to the substrate. When only a single negative battery is available, it connects to both VBH and VBL.
VBL	Battery (Power)		Connection to low-battery supply used for short loops. When only a single negative battery is available, this pin must be connected to VBH.
VBP	Positive Battery (Power)		Used in Ringing State and for Extended Loop operation.
VCC	+5 V Power Supply		Positive supply for low voltage analog and digital circuits in the Le79R251 device.
VLB	Longitudinal Voltage	I	Sets the DC longitudinal voltage of the Le79R251 device. It is the reference for the longitudinal control loop. When the VLB pin is greater than VREF, the Le79R251 device sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0V and VREF, the longitudinal voltage decreases linearly with the voltage on the VLB pin.
VREF	1.4 V Analog Reference	I	The ISLAC chip provides this voltage which is used by the Le79R251 device for internal reference purposes. All analog input and output signals interfacing to the ISLAC chip are referenced to this pin.
VSAB	Loop Voltage	O	Scaled-down version of the voltage between the sense points SA and SB on this pin.
VTX	4-Wire Transmit Signal	O	The voltage between this pin and VREF is a scaled down version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative with respect to VREF.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage Temperature	–55 to +150° C
Ambient temperature, under bias	–40 to +85° C
V_{CC} with respect to GND	–0.4 to +7 V
V_{BH}, V_{BL} with respect to GND (see Note 2)	+0.4 to –85 V
V_{BP} with respect to GND	–0.4 to +85 V
V_{BP} with respect to VBH	150 V
BGND with respect to GND	–3 to +3V
Voltage on R1 relay outputs	+7 V
AD or BD to BGND:	
Continuous	V_{BH} – 1 to VBP + 1
10 ms (F = 0.1 Hz)	V_{BH} – 5 to VBP + 5
1 µs (F = 0.1 Hz)	V_{BH} – 10 to VBP + 10
250 ns (F = 0.1 Hz)	V_{BH} – 15 to VBP + 15
Current into SA or SB: 10 µs rise to Ipeak; 1000 µs fall to 0.5 Ipeak; 2000 µs fall to I =0	I_{PEAK} = ±5 mA
Current into SA or SB: 2 µs rise to Ipeak; 10 µs fall to 0.5 Ipeak; 20 µs fall to I = 0	I_{PEAK} = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to GND	–0.4 to VCC + 0.4 V
ESD Immunity (Human Body Model)	1000 V min
Charged device model	900 V
Maximum power dissipation, (See Note 1) T_A = 70°C T_A = 85°C	 1.67 W 1.33 W

Note:

1. *Thermal-limiting circuitry on chip will shut down the circuit at a junction temperature of about 160° C. Operation above 145° C junction temperature may degrade device reliability.*
2. *Rise time of VBH (dv/dt) must be limited to less than 27 V/µs.*

Thermal Resistance

The junction to air thermal resistance of the Le79R251 device in a 32-pin, PLCC package is 43°C/W. The typical junction to case thermal resistance is 14°C/W. Measured under free air convection conditions and without external heat-sinking.

Electrical Operating Ranges

Legerity guarantees the performance of this device over commercial (0°C to 70°C) and industrial (–40°C to 85°C) temperature ranges by conducting electrical characterization over each range, and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore TR-TSY-000357 Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial
	–40 to +85 °C extended temperature
Ambient Relative Humidity	5 to 95%

Electrical Ranges

VCC	5 V ± 5%
VBL	–15 V to VBH
VBH	–18 to –79 V
VBP	+79 to +8 V
Maximum supply voltage across device, VBP–VBH	140 V
BGND with respect to GND	–100 to +100 mV
Load resistance on VTX to Vref	20 kΩ minimum
Load resistance on VSAB to Vref	20 kΩ minimum

SPECIFICATIONS

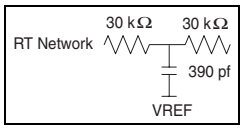
Power Dissipation

Loop resistance = 0 to ∞ unless otherwise noted (not including fuse resistors), 2 x 50 Ω fuse resistors.
For case 1: BATL = –36 V, BATH = –68 V, BATP = +52 V, and VCC = +5 V.
For case 2, BATL = -24 V, BATH = -48 V, BATP = +79 V, and VCC = +5 V.
For power dissipation measurements, DC-feed conditions are as follows:

- ILA (Active mode current limit) = 25 mA (IRSN = 50 µA)
- RFD (Feed resistance) = 500 Ω
- VAS (Anti-sat activate voltage) = 10 V
- VAPP (Apparent Battery Voltage) = 48 V
- RMGL = RMGP (Thermal management resistors) = 1 kΩ

Description	Test Conditions		Case 1		Case 2		Unit
			Typ	Max	Typ	Max	
Power Dissipation Normal Polarity	On-Hook Disconnect		65	85	55	80	mW
	On-Hook Standby		110	140	90	120	
	On-Hook Transmission Fixed Longitudinal Voltage	ISLIC	210	270	170	220	
	On-Hook Active High Battery	ISLIC	300	420	220	350	
	Off-Hook Active Low Battery RL = 294 Ω	ISLIC TMG	700 200	800 240	400 40	500 60	
	On-Hook Active Boost Battery		600	970	660	1050	
Power Supply Currents	On-Hook Disconnect	VBH VBL VCC VBP	0.6 0.1 3.9 0.08	0.9 0.2 4.5 0.15	0.6 0.1 3.9 0.08	0.9 0.2 4.5 0.15	mA
	On-Hook Standby	VBH VBL VCC VBP	1.3 0 4.3 0.12	1.7 0 5 0.3	1.3 0 4.3 0.12	1.7 0 5 0.3	
	On-Hook Transmission Fixed Longitudinal Voltage	VBH VBL VCC VBP	3.5 0 7.2 0.10	4.0 0 8.5 0.2	3.5 0 7.2 0.10	4.0 0 8.5 0.2	
	On-Hook Active High Battery	VBH VBL VCC VBP	4 0 8.2 0.10	6 0 11 0.2	4 0 8.2 0.10	6 0 11 0.2	
	Off-Hook Active Low Battery RL = 294 Ω	VBH VBL VCC VBP	2.2 27.5 8.2 0.10	3 30 11 0.2	2.2 27.5 8.2 0.10	3 30 11 0.2	
	Active Boost Battery On-Hook	VBH VBL VCC VBP	5 0 5 5	8.5 0 8.5 7.5	5 0 5 5	8.5 0 8.5 7.5	

DC Specifications



Unless otherwise specified, test conditions are: V_{CC} = 5 V, R_{MGP} = R_{MGL} = 1 kΩ, BATH = –68 V, BATL = –36 V, BATP = +52 V, R_{RX} = 150 kΩ, R_L = 600 Ω, R_{SA} = R_{SB} = 200 kΩ, R_{FA} = R_{FB} = 50 Ω, C_{HP} = 22 nF, C_{AD} = C_{BD} = 22 nF, I_{RSN} = 50 µA. DC-feed conditions are normally set by the ISLAC device. When the Le79R251 device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ISLAC device.

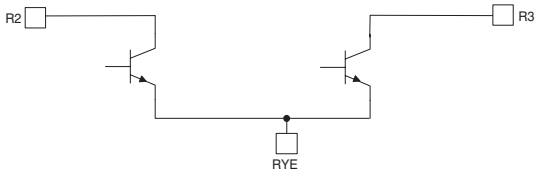
No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire loop voltage, including offset (V_A-V_B)	Standby mode, open circuit, |VBH| < 55 V |VBH| > 55 V GND – VB Any Active mode (does not include OHT), RL = 600 Ω, I_{RSN} = 50 µA OHT mode, RL = 2200 Ω, I_{RSN} = 20 µA	 |VBH| – 9 48 13.88 19.8	 |VBH|–8 52 15 22	 |VBH|–7 55 55 16.13	V	2
2	Feed resistance per leg at pins AD & BD	Standby mode	130	250	375	Ω	
3	Feed current limit	Feed current Standby mode, RL = 600 Ω	 18	 30	 40	mA	
	IMT current	Standby mode, RL = 2200 Ω	44.6	56		µA	
	ILG current	Standby mode A to VBH B to Ground	 25.7 25.7				
4	Ternary input voltage boundaries for LD pin. Mid-level input source must be Vref.	Low boundary Medium boundary High boundary Input high current Input low current Mid-level current	 VREF–0.3 CREF – 1 –20 –20 –20		0.6 VREF+0.3 20 20 20	V V V µA µA µA	 2 2 2
5	Logic Inputs P1, P2, P3	Input high voltage Input low voltage Input high current Input low current	2.0 –20 –20		 0.6 20 20	V V µA µA	
6	VTX output offset		–50		+50	mV	
7	VREF input current	VREF = 1.4 V, Active Low Battery I_{LOOP} = -25 mA I_{LOOP} = 0 mA		 60 200	 120 300	µA	2
8	CREF input current	CREF = 3.3 V		1	10	µA	2
9	β, DC Ratio of VSAB to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	Tj < 145°C, VSA – VSB = 22 V	0.00606	0.00667	0.00740	V/V	
10	Gain from VLB pin to A or B pin		41	45	49	V/V	2
11	VLB pin input current	VLB = VREF ±1V	–100		100	µA	2
12	ILOOP/IMT	ILOOP = 10 mA	290	300	350	A/A	
13	ILONG/ILG	ILONG = 10 mA	580	600	700	A/A	
14	Input current, SA and SB pins	Active modes		1.0	3.0	µA	2
15	K1	Incremental DC current gain	462	500	538		2
16	ISA/IMT	Disconnect, ISA = 2 mA	5.0	6	7	A/A	
17	ISB/ILG	Disconnect, ISB = 2 mA	10	12	14		
18	VSAB output offset		-20		20	mV	
19	IMT output offset		–3	0	3	µA	

No.	Item	Condition	Min	Typ	Max	Unit	Note
20	ILG output offset		–3	0	3	µA	

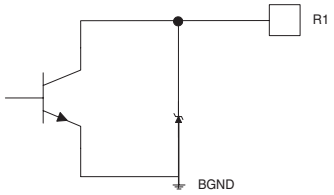
Relay Driver Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	On Voltage	25 mA/relay sink 40 mA/ relay sink		0.4 0.8	0.5 1.0	V	2
2	R2,R3 Off Leakage	R2,R3 = BGND RYE = VBH		0	100	µA	
3	Zener Break Over, R1	Iz = 100 µA	9	9.5	10.5	V	
4	Zener On Voltage, R1	Iz = 30 mA	8.0	8.8	9.5		

Figure 1. Relay Drivers



A. Relay Driver Configuration



B. Ring Relay

Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	f = 300 to 3400 Hz		1	10	Ω	2
2	VTX output impedance			3	20		
3	Max, AC + DC loop current	Active High Battery, Active Low Battery, Active Boosted Battery	70			mA	2
4	Input impedance, A or B to GND	Active mode		70	135	Ω	
5	2-4 wire gain	–10 dBm, 1 kHz, 0 to 70°C T_A = –40°C to 85°C	–14.13 –14.18	–13.98 –13.98	–13.83 –13.78	dB	 2
6	2-4 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz T_A=–40°C to 85°C	–0.1 –0.15		+0.1 +0.15		 2
7	2-4 wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm T_A = –40 to 85°C	–0.1 –0.15	0 0	+0.1 +0.15		5 2, 5
8	4-2 wire gain	–10 dBm, 1 kHz T_A= –40°C to 85°C	–0.15 –0.2	0 0	+0.15 +0.2		 2
9	4-2 wire gain variation with frequency	300 to 3400 Hz, relative to 1 kHz	–0.1		+0.1		
10	4-2 wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm	–0.1		+0.1		2, 5

No.	Item	Condition	Min	Typ	Max	Unit	Note
11	Total harmonic distortion level 2-wire 4-wire 4-wire overload level at VTX	300 Hz to 3400 Hz 0 dBm 11.2 dBm –12 dBm –0.8 dBm RLOAD = 600 Ω		 ±1	 –50 –40 –48 –38 	 dB dB dB dB Vp	 2
12	Idle channel noise C-message Weighted Psophometric Weighted	Active modes, R_L = 600 Ω 2-wire 4-wire 2-wire 4-wire		 +7 –7 –83 –97	 +11 –79 	 dBrnC dBmp 	
13	Longitudinal balance (IEEE method) Normal Polarity	L - T 200 to 1000 Hz T_A = –40°C to 85°C 1000 to 3400 Hz T_A = –40°C to 85°C	58 53 53 48	63 58 		dB	 2 2
		T - L 200 to 3400 Hz	40				
		L - T IL = 50 to 3400 Hz		63			2
	Reverse Polarity	L - T 200 to 1000 Hz T_A = –40°C to 85°C	50 48				
14	PSRR (VBH, VBL, VBP)	50 to 3400 Hz 3.4 K to 50 kHz	25	45 40			3,4 1, 2, 4
15	PSRR (VCC)	50 to 3400 Hz 3.4 K to 50 kHz	25	45 35			3, 4 1, 2, 4
16	Longitudinal AC current per wire	F = 15 to 60 Hz Active mode	20	30		mArms	2
17	Metering distortion	Freq = 12 kHz 2.8 Vrms Freq = 16 kHz metering load = 200 Ω	40	56		dB	2

Ringing Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Peak Ringing Voltage	Active Internal Ringing	(VBP-VBH) - 10 V		133	V	7

Current-Limit Behavior

No.	SLIC Mode	Condition	Min	Typ	Max	Unit	Note
1	Disconnect	Applied fault between ground and T/R VBH applied to Tip or Ring		1 VBH/200K	100	µA A	6
2	Tip Open	Short to GND		30	40	mA	
3	Standby	Short Tip-to-VBH Short Ring-to-GND		30 30	45 40		
4	Active Ringing	ISLAC generating internal ringing		100			

Thermal Shutdown Fault Indications

No.	Fault	Indication
1	No Fault	ILG, IMT operates normally (Vref ±1V)
2	Thermal Shutdown	ILG, IMT above 2.8 V

Note:

1. *These tests are performed with the following load impedances:*
   Frequency < 12 kHz – Longitudinal impedance = 500 Ω; metallic impedance = 300 Ω
   Frequency > 12 kHz – Longitudinal impedance = 90 Ω; metallic impedance = 135 Ω
2. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
3. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

4. When the Le79R251 device and ISLAC device is in the anti-sat operating region, this parameter is degraded. The exact degradation depends on system design.

5. –55 dBm gain tracking level not tested in production. This parameter is guaranteed by characterization and correlation to other tests.

6. This spec is valid from 0 V to VBL or –50 V, whichever is lower in magnitude.

7. Other ringing-voltage characteristics are set by the ISLAC device.

OPERATING MODES

The Le79R251 device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin controls the loading of P1, P2, and P3 values into the proper bits in the Le79R251 device control register. The device control register is a register in within the Le79R251 that latches the multiplexed relay and state data. This is organized as two sets of three bits: RD1-RD3 for the relay data and C1-C3 for the state control. When the LD pin is less than 0.6 V, P1–P3 will contain data for relay control bits RD1, RD2 and RD3. These are latched into the first three bits in the Le79R251 device control register. When the LD pin is more than CREF - 1, P1–P3 will contain ISLIC control data C1, C2, and C3, which are latched into the last three bits of the Le79R251 device control register. Setting the voltage on the LD pin to VREF ± 0.3 V locks the contents of the Le79R251 device control register.

The operating mode of the Le79R251 device is determined by the C1, C2, and C3 bits in the control register of the Le79R251 device. The table below defines the Le79R251 device operating modes set by these signals.

Under normal operating conditions, the ISLIC device does not have active relays. The Le79R251 device to ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Le79R251 devices.

To perform external ringing, the ISLAC device from the Intelligent Access voice family is set to external ringing mode (RMODE = 1), enables the ring relay, and puts the Le79R251 device in the Standby mode.

Table 1. Operating Mode Descriptions

C3	C2	C1	Operating Mode	Battery Voltage Selection	Operating Mode	Connection to RMGPi & RMGLi Resistors	Notes
0	0	0	Standby	High Battery (BATH) and BGND	(High ohmic feed): Loop supervision active, A and B amplifiers shut down	Open	1
0	0	1	Tip Open	High Battery (BATH) and BGND	Tip Open: AD at High-Impedance, Channel A power amplifier shut down	Open	1
0	1	0	On-Hook Transmission, Fixed Longitudinal Voltage	High Battery (BATH) and BGND	Fixed longitudinal voltage of –29 V	A and B Amplifier Output	
0	1	1	Disconnect	Low Battery selection at VBL	AD and BD at High-Impedance, Channel A and B power amplifiers shut down		
1	0	0	Active Boosted Battery	High Battery (BATH) and Positive Battery (BATP)	Active feed, normal or reverse polarity		
1	0	1	Active High Battery	High Battery (BATH) and BGND			
1	1	0	Active Low Battery	Low Battery (BATL) and BGND			
1	1	1	Active Internal Ringing	High Battery (BATH) and Positive Battery (BATP)	Active internal ringing		

Note:

1. In these modes, the ring lead (B-lead) output has a –50 V internal clamp to battery ground (BGND).

Operating Mode Descriptions

Operating Mode	Description
Disconnect	This mode disconnects both A and B output amplifiers from the AD and BD outputs. The A and B amplifiers are shut down and the Le79R251 device selects the low battery voltage at the VBL pin. In the Disconnect state, the currents on IMT and ILG represent the voltages on the SA and SB pins, respectively. These currents are scaled to produce voltages across RMTi and RLGi of $\frac{V_{SA}}{400}$ and $\frac{V_{SB}}{400}$, respectively.
Standby	The power amplifiers are turned off. The AD output is driven by an internal 250 Ω (typical) resistor, which connects to ground. The BD output is driven by an internal 250 Ω (typical) resistor, which connects to the high battery (BATH) at the VBH pin, through a clamp circuit, which clamps to approximately –50 V with respect to BGND. For VBH values above–55 V, the open-circuit voltage, which appears at this output is ~VBH + 8 V. If VBH is below –55 V, the voltage at this output is –50 V. The battery selection for the balance of the circuitry on the chip is VBL. Line supervision remains active. Current limiting is provided on each line to limit power dissipation under short-loop conditions as specified in the “Le79R251 device Current-Limit Behavior” section. In external ringing, the standby ISLIC state is selected.
Tip Open	In this mode, the AD (Tip) lead is opened and the BD (Ring) lead is connected to a clamp, which operates from the high battery on VBH pin and clamps to approximately –50 V with respect to BGND through a resistor of approximately 250 Ω (typical). The battery selection for the balance of the circuitry on the chip is VBL.
Active High Battery	In the Active High Battery mode, battery connections are connected as shown in “Operating Modes” on page 14. Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. Active High Battery mode is enabled during a call in applications when a long loop can be encountered. SBAT = VBH.
Active Low Battery	Both output amplifiers deliver the full power level determined by the programmed DC-feed conditions. VBL, the low negative battery, is selected in the Active Low Battery mode. This is typically used during the voice part of a call. SBAT = VBL.
Active Boosted Battery	In the Active Boosted Battery mode, battery connections are as shown in “Operating Modes” on page 14. Both output amplifiers deliver the power level determined by the programmed DC-feed conditions. Active Boosted Battery mode is enabled during a call in applications when an extended loop can be encountered. SBAT = VBP - VBH.
Active Internal Ringing	In the Internal Ringing mode, the Le79R251 device selects the battery connections as shown in “Operating Modes” on page 14. When using internal ringing, both the AD and BD output amplifiers deliver the ringing signal determined by the programmed ringing level. SBAT = VBP - VBH.
On-Hook Transmission (OHT), Fixed Longitudinal Voltage	In the On-Hook Transmission, Fixed Longitudinal Voltage mode, battery connections are as shown in “Operating Modes” on page 14. The longitudinal voltage is fixed (as defined in the Table , “Operating Modes,” on page 14) to allow compliance with safety specifications for some classes of products, such as ones needing to meet the requirements of UL1950. SBAT = VBH.

Driver Descriptions

Control bits RD1, RD2, and RD3 do not affect the operating mode of the Le79R251 device. These signals perform the following functions:

Driver	Description
R1	A logic 1 on RD1 turns the R1 driver on and operates a relay connected between the R1 pin and VCCD. R1 drives the ring relay when external ringing is selected.
R2	A logic 1 on the RD2 signal turns the R2 driver on and routes current from the R2 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R2 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the BD (Ring) lead and connect a test load between R2 and the AD(Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R251 device side of the protection resistor to avoid damage to the R2 driver.
R3	A logic 1 on the RD3 signal turns the R3 driver on and routes current from the R3 pin to the RYE pin. In the option where the RYE pin is connected to ground, the R3 pin can sink current from a relay connected to VCCD. Another option is to connect the RYE pin to the B (Ring) lead and connect a test load between R3 and the A(Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79R251 device side of the protection resistor to avoid damage to the R3 driver.

Thermal-Management Equations

Applies to all Modes except Standby and Ringing which have no thermal management:

$I_L < 7.5$ mA $P_{SLIC} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) \bullet I_L + 0.3$ W $PT_{RTMG} = 0$	TMG resistor-current is limited to be 7.5 mA < I_L. If $I_L < 7.5$ mA, no current flows in the TMG resistor and it all flows in the Le79R251.
$I_L > 7.5$ mA $R_{TMG} = (S_{BAT} - I_L(R_L + 2R_{FUSE})) / (2(I_L - 7.5\text{ mA}))$ $P_{SLIC} = I_L(S_{BAT} - I_L(R_L + 2R_{FUSE})) + 0.3\text{ W} - PT_{RTMG}$ $PT_{RTMG} = (I_L - 7.5\text{ mA})^2(2R_{TMG})$	These equations are valid when $R_{TMG} \bullet (I_L - 7.5\text{ mA}) < (S_{BAT} - (R_F + R_L)I_L) / 2 - 2$ because the longitudinal voltage is one-half the battery voltage and the TMG switches require approximately 2 V. To choose a power rating for RTMG: $P_{RATING} > PT_{RTMG} / 2$ Note that for reliable operation, P_{SLIC} should be less than 1.33 W.

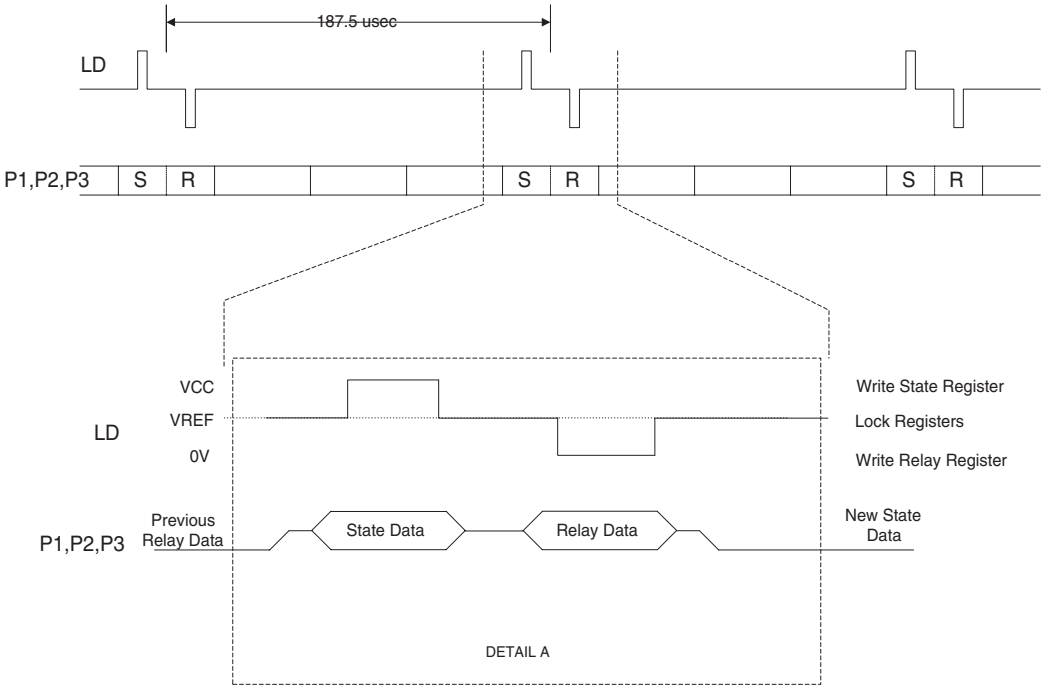
TIMING SPECIFICATIONS

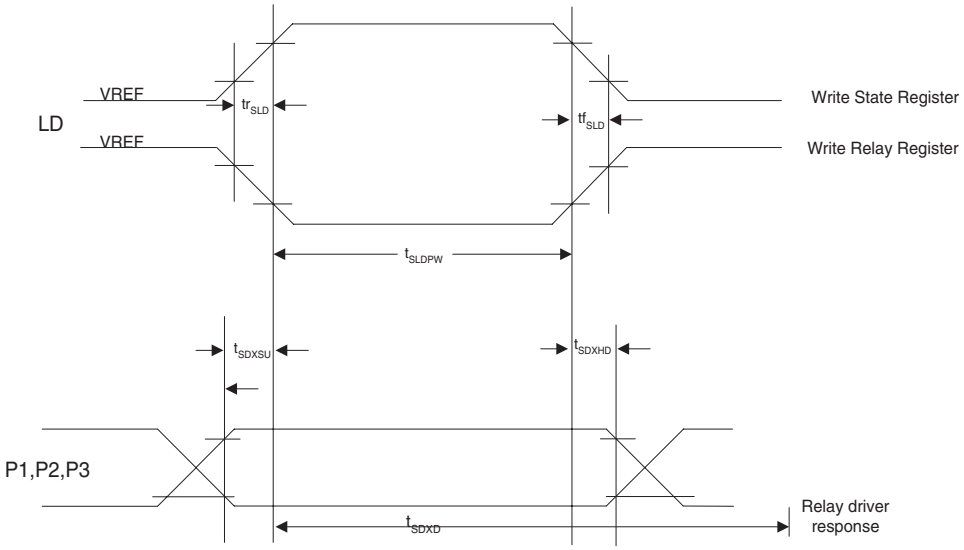
Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD	Rise time Le79R251 device LD pin			2	µs
tfSLD	LD	Fall time Le79R251 device LD pin			2	
tSLDPW	LD	LD minimum pulse width	3			
tSDXSU	P1,P2,P3	P1–3 data Setup time	4.5			
tSDXHD	P1,P2,P3	P1–3 data hold time	4.5			
tSDXD	P1,P2,P3	Max P1–3 data delay			5	

Note:

1. *The P1–3 pins are updated continuously during operation by the LD signal.*
2. *After a power-on reset or hardware reset, the relay outputs from the Le79R251 device turn all relays off. An unassuming state is to place the relay control pins, which are level triggered, to a reset state for all relays. Any noise encountered only raises the levels toward the register lock state.*
3. *When writing to the ISLIC registers, the sequence is:*
   a) *Set LD pin to mid-state*
   b) *Place appropriate data on the P1–3 pins*
   c) *Assert the LD pin to High or Low to write the proper data*
   d) *Return LD pin to mid-state*
4. *Le79R251 device registers are refreshed at 5.33 kHz when used with an ISLAC device.*
5. *If the clock or MPI becomes disabled, the LD pins and P1–3 returns to 0 V state, thus protecting the Le79R251 device and the line connection.*
6. *Not tested in production. Guaranteed by characterization.*

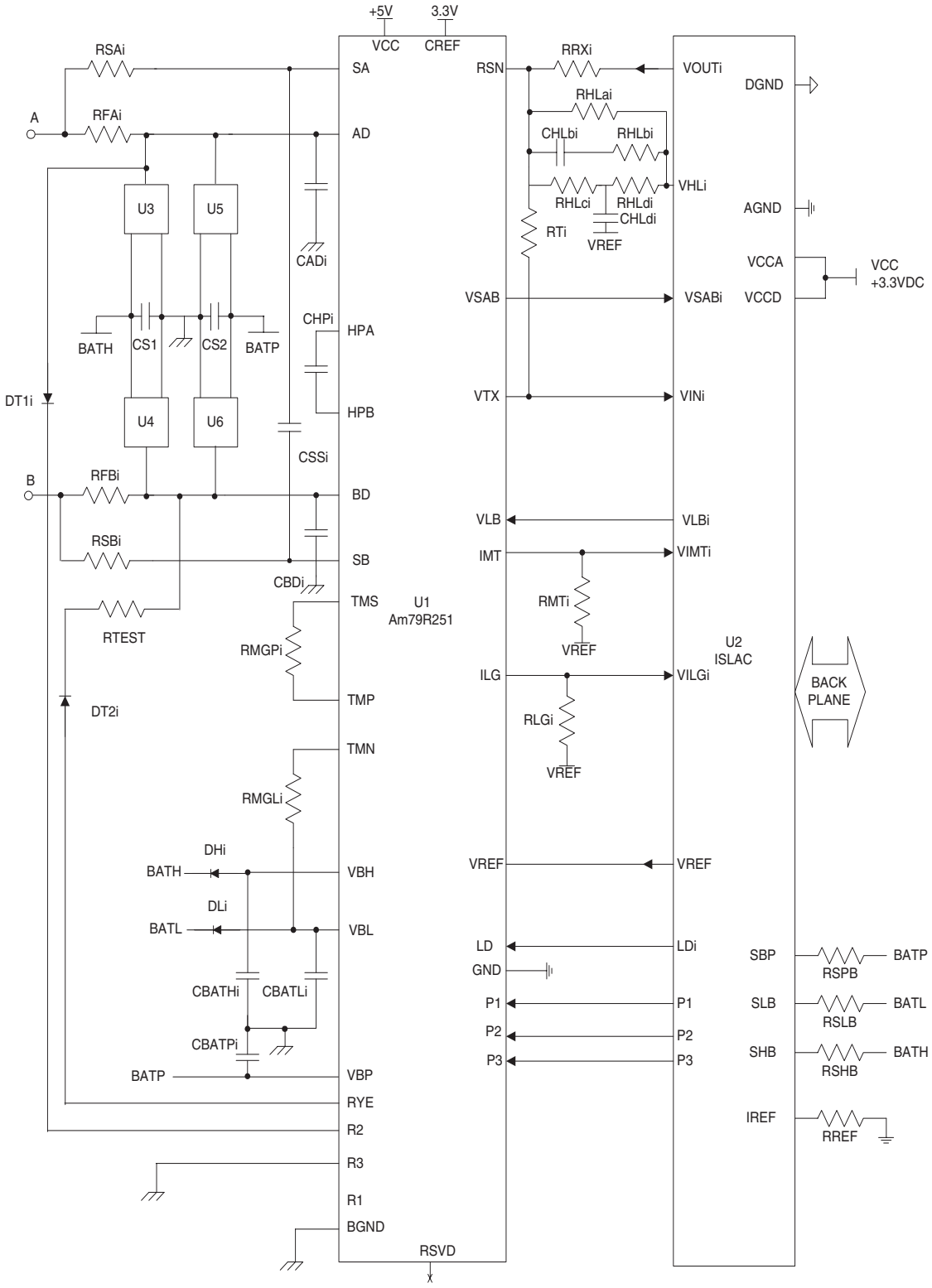
WAVEFORMS


187.5 usec
LD
P1,P2,P3
S
R
S
R
S
R
VCC
VREF
0V
LD
Write State Register
Lock Registers
Write Relay Register
Previous
Relay Data
P1,P2,P3
State Data
Relay Data
New State
Data
DETAIL A


VREF
LD
VREF
tr SLD
tf SLD
Write State Register
Write Relay Register
t SLDPW
t SDXSU
t SDXHD
P1,P2,P3
t SDXD
Relay driver
response

APPLICATION CIRCUIT

Internal Ringing Line Card Schematic



Note:

1. *CSS required for > 2.2 VRMS metering.*
2. *Connections are shown for one channel.*

LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2,3,4).

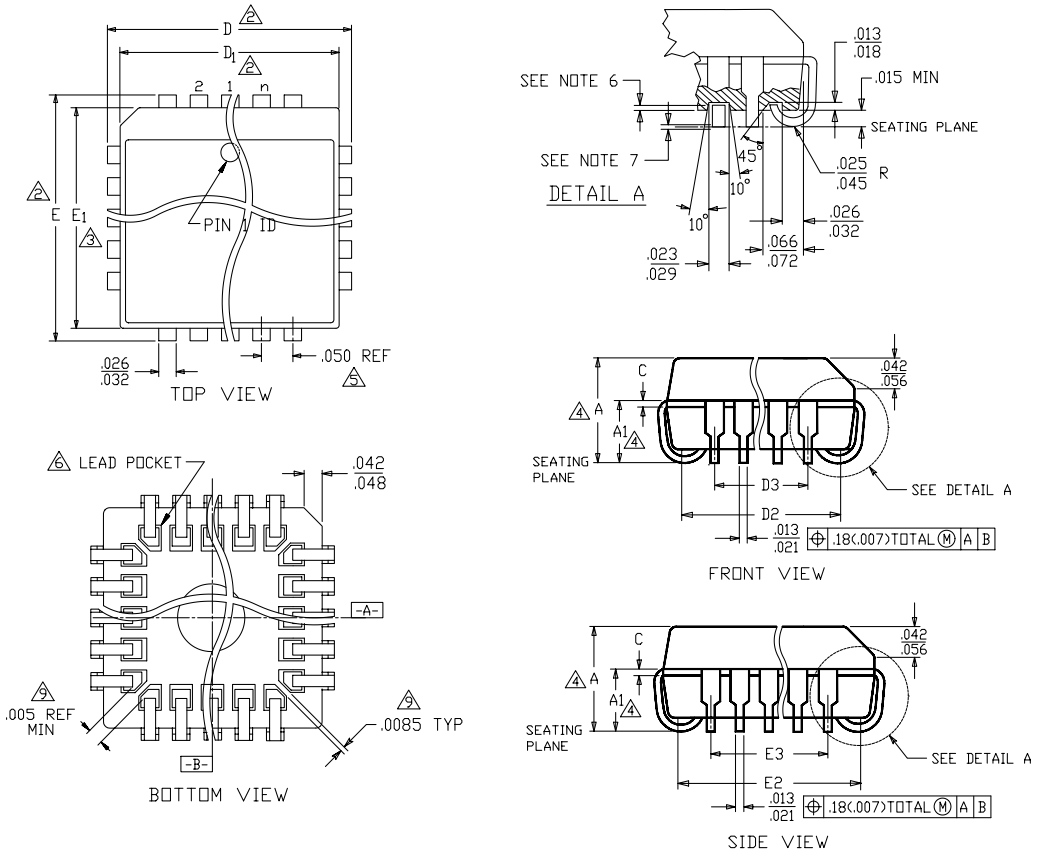
Item	Type	Value	Tol.	Rating	Comments
Components for Internal and External Ringing					
U1	Le79R251 device				ISLIC device
U2	Am79X22xx				ISLAC device
U3, U4	B1100CC			100 V	TECCOR Battrax protector
U5, U6	B2100CC			100 V	TECCOR Battrax protector
DHi, DLi, DT1i, DT2i	Diode	100 mA		100 V	50 ns
RFAi, RFBi	Resistor	50 Ω	2%	2 W	Fusible PTC protection resistors
RSAi, RSBi	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RTi	Resistor	80.6 kΩ	1%	1/10 W	
RRXi	Resistor	90 kΩ	1%	1/10 W	
RREF	Resistor	69.8 kΩ	1%	1/10 W	Current reference
RMGLi, RMGPi	Resistor	1 kΩ	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 kΩ	1%	1/8 W	
RHLai	Resistor	40.2 kΩ	1%	1/10 W	
RHLbi	Resistor	4.32 kΩ	1%	1/10 W	
RHLci	Resistor	2.87 kΩ	1%	1/10 W	
RHLdi	Resistor	2.87 kΩ	1%	1/10 W	
CHLbi	Capacitor	3.3 nF	10%	10 V	Not Polarized
CHLdi	Capacitor	0.82 µF	10%	10 V	Ceramic
RMTi	Resistor	3.01 kΩ	1%	1/8 W	
RLGi	Resistor	6.04 kΩ	1%	1/8 W	
RTEST	Resistor	2 kΩ	1%	1 W	Test board
CADi, CBDi [1]	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBATHi, CBATLi, CBATPi	Capacitor	100 nF	20%	100 V	Ceramic
CHPi	Capacitor	22 nF	20%	100 V	Ceramic
CS1i, CS2i[1]	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
CSSi[3]	Capacitor	56 pF	5%	100 V	Ceramic

Note:

1. *Value can be adjusted to suit application.*
2. *Can be looser for relaxed ring-trip requirements.*
3. *Required for metering > 2.2 Vrms, otherwise may be omitted.*

PHYSICAL DIMENSIONS

PL 032



PACKAGE	PL 032	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

Dwg rev AH; 08/00

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"
4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE
5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005".
6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.
7. LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.
8. LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.
9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

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