Application Note
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L8560 Sinusoidal Ringing Generation Using a PWM Input to B1

Introduction

The L8560 generates a trapezoidal waveform by injecting approximately ±29 µA into capacitors FB1 and FB2. When used in this mode, the ramp of the waveform is determined by this current and the size of capacitors FB1 and FB2.

If, instead, the B1 input is pulse-width modulated (PWM) by a sinusoidally modulated signal, the output at tip and ring will be the envelope of the modulation signal which is sinusoidal. Its frequency is the same as the sinusoidal modulation signals.

From the internal scheme of the L8560, shown in Figure 1, the average current delivered to FB1 or FB2 is the following:

$I_{AVG} = 2 \times (PW - 0.5) \times 29\ \mu A$

where PW is the average pulse width, which may vary from zero to one with respect to the center at 0.5.

Thus, the output amplitude at tip/ring is:

$$V_{T/R}\ (\text{tip/ring}) = 4 \times \frac{29\ \mu A}{\omega \times C_{FB}} \times (PW - 0.5)$$

where $V_{T/R}$ = the amplitude at tip/ring,

$\omega = 2 \times \pi \times$ ringing frequency,

$C_{FB} = C_{FB1} = C_{FB2}$,

PW = the amplitude of PWM.

For example, if $C_{FB1} = C_{FB2} = 0.0033\ \mu F$, $(PW - 0.5) = 0.46$ (27% to 73% modulation), $\omega = 2 \times \pi \times 20$ Hz,

then:

$V_{T/R}$ = 128 Vp-p (45 Vrms).

Design Considerations

1. Although the PWM frequency can be over a wide range, e.g., 5 kHz to 100 kHz for a normal 20 Hz ringing frequency, the normal range is expected to be 10 kHz to 20 kHz.
2. A certain design will be useful only for a given frequency. If other ringing frequencies are required, the modulation frequency and the PWM amplitude should be varied to maintain a constant gain.
3. The gain from B1 input to tip/ring output, which will result in amplitude of the voltage at tip/ring, is dependent on the capacitor value and the value of the 29 µA current source. When amplitude of the voltage at tip/ring exceeds $|V_{BAT}| - V_{OH}$, where V_{OH} is the overhead of L8560 at ringing mode (about 2 V), it starts clipping. Small amounts (less than 4 V) of clipping will result in larger (undesirable) total harmonic distortion (THD). To keep THD within a reasonable range, ≤5%, while still approaching a large output voltage at tip/ring, i.e., 45 Vrms or above, the amount of clipping must be limited. As discussed later in this document, one may have to design at the edge of clipping. That means variation may cause clipping. To ensure accuracy and minimize variation of C_{FB1} and C_{FB2} capacitors, tie them ±2%. The internal current source (29 µA) is about ±8% accurate.
4. The accuracy requirement on the capacitors could be reduced by introducing a high-accuracy resistor across FB1 and FB2. But any dc offset, or any pulse-width offset, will result in clipping whenever the amplitude plus the sinewave offset exceed the supply voltage. While in capacitor mode, offset will cause drift from side to side and will not cause clipping until the overall magnitude exceeds the supply voltage. It is recommended that precision capacitors be used for C_{FB1} and C_{FB2} in this application.
5. On the other hand, as long as the THD is still within a good range, we can make use of the clipping to absorb some amount of variations, thus allowing maximum possible voltage out of the SLIC by designing the normal output voltage right at the edge of clipping, rather than designing the minimal output voltage at the edge of clipping (to avoid any clipping).

Design Considerations (continued)

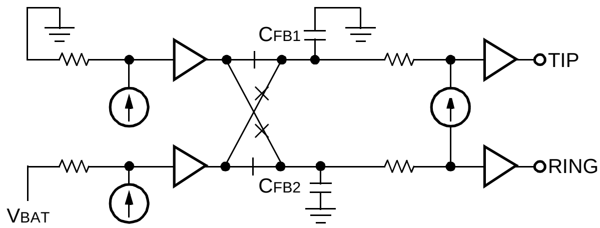

Figure 1. L8560 Internal Scheme

Applications

Figure 2 shows the lab evaluation connections, and Figures 3—6 show the conditions where V_{BAT} = –65.0 V, V_{CC} = –5.0 V, C_{FB1} = C_{FB2} = 0.0033 µF, $V_{T/R}$ = 43.7 Vrms, and T_{HD} = 1.79%. The output from the digital oscillograph in Figure 2 is the source for the data shown in Figures 3—5. The output from the spectrum analyzer shown in Figure 2 is the source for the data shown in Figure 6.

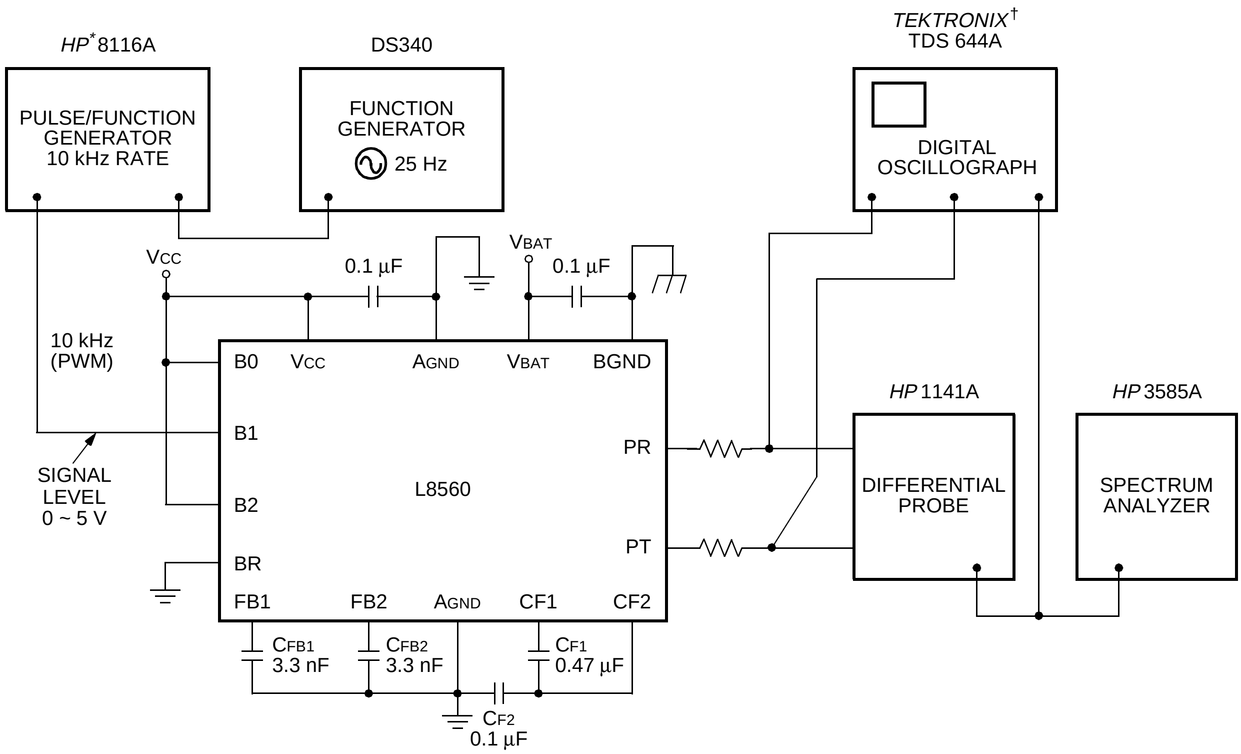

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Figure 2. L8560 Test Connection

Applications (continued)

Figure 3 shows the sinusoidal source output from DS340.

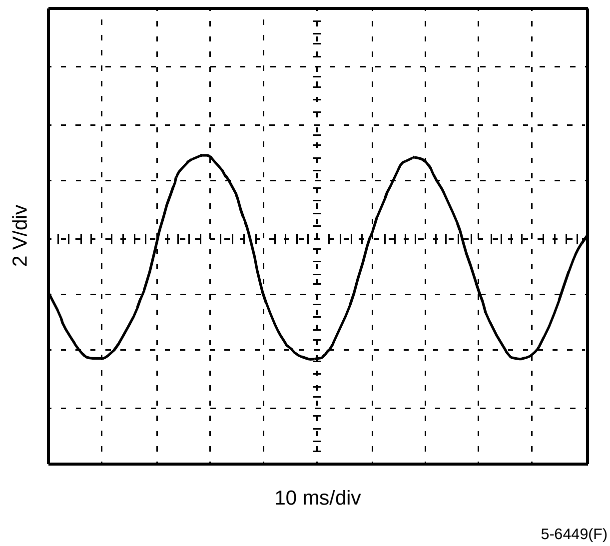

Figure 3. Sinusoidal Source from DS340

Figure 4 shows the output at tip and ring.

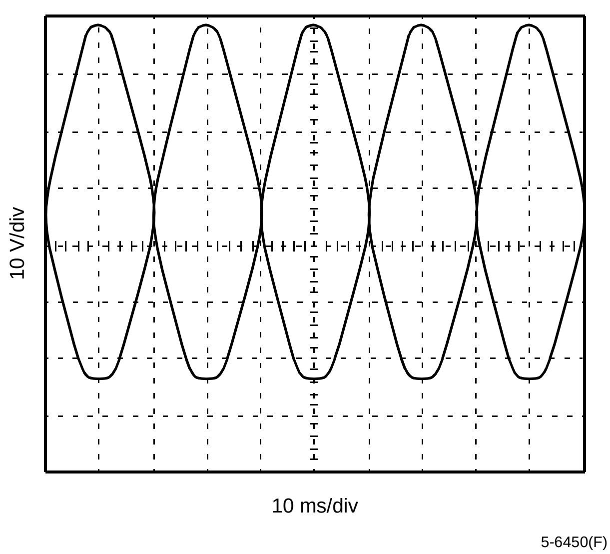

Figure 4. Tip and Ring Output

Figure 5 shows the differential output (attenuated by 100).

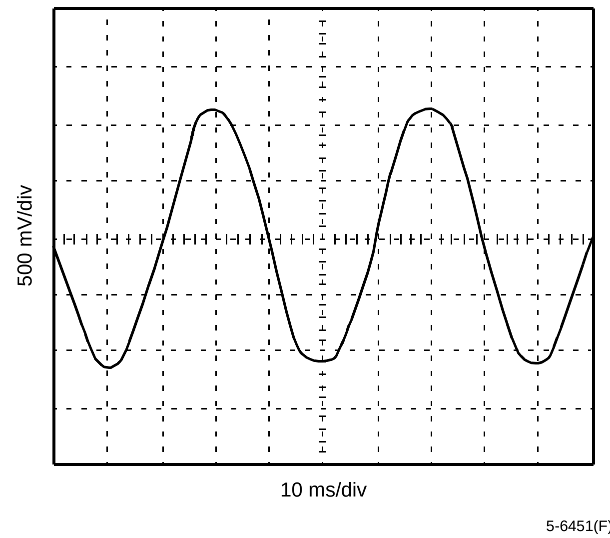

Figure 5. Differential Output (Attenuated by 100)

Figure 6 shows the spectrum of the differential signal.

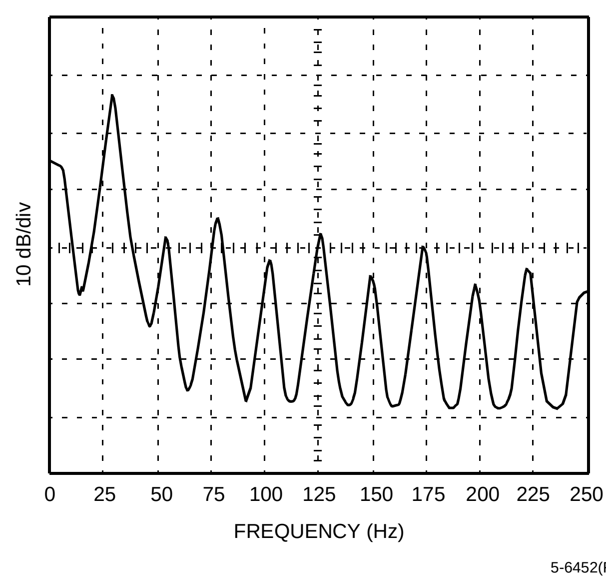

Figure 6. Differential Signal Spectrum

Applications (continued)

Normally, the amplitude of the ringing signal at the handset needs to be 40 Vrms or above. For short loop applications, 45 Vrms is desirable at tip/ring at open loop condition, or about (45 x 1.414 x 2) 126 Vp-p.

Assume that the absolute accuracy of the C_{FB1} and C_{FB2} capacitors is at ±2% accuracy. Since the internal 29 µA current source is at about ±8% accuracy, the combination of the variation can be estimated as:

$$\sqrt{2\%^2 + 8\%^2} = 8.25\%$$

Now the resulting Vp-p at tip/ring needs to be 126 V x 1.0825 = 136 V, and the following equation represents PW.

$$136 = 4 \times \frac{29\ \mu A}{2 \times 3.1415 \times \text{freq (Hz)} \times 3.3\ nF} \times (PW - 0.5)$$

Assume frequency = 25 Hz, (PW – 0.5) = 0.60 (means 20% to 80% modulation).

Lab evaluation experience shows that $V_{BAT(min)}$ = (136/2) 68 V may keep the THD within 5% for the above case.

The maximum possible $V_{BAT(max)}$ = 70 V as the device is rated up to 70 V.

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