Application Note
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microelectronics group

Lucent Technologies
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Switching Behavior of the L9215/16 Ringing SLIC

Contents

Figures

Scope

This application note describes the recommended operation of the Lucent L9215/16 ringing SLICs for switching in and out of the ring mode during both ringing cadence and ring trip. It also discusses forward/reverse battery state transition, state transition in general, and battery switch operation timing. This application note assumes the user has knowledge of the L9215/16 ringing SLIC operation.

Control Signal Timing During Ring Cadence

The L9215/16 can be used in two basic modes of operation to create the power ringing signal. These modes are discussed in detail in the L9215/16 data sheet. In brief, the first mode of operation, the input at $RING_{IN}$ can be a sine wave or a filtered PWM to produce a sine ring signal at tip and ring. The second mode of operation uses a filtered square wave input at $RING_{IN}$. This creates a trapezoidal waveform at tip and ring. In either state of operation, the input at $RING_{IN}$ is amplified to create the power ring signal seen at tip and ring.

Sine Wave Input Mode of Operation

This SLIC creates ringing by amplifying a low-voltage input at a dedicated input ($RING_{IN}$). The ring mode is achieved by toggling a logic bit (BR) low. This turns on the ringing amplifier and puts the amplified ring signal on tip and ring. During nonring modes (BR high), since the state of the SLIC is not affected by $RING_{IN}$, and the ringing amplifier is off the low-voltage sinusoidal waveform input signal can be left on $RING_{IN}$. BR is the controlling bit for ring cadence.

In this mode of operation, there are certain considerations that should be made with respect to false loop supervision glitches seen at NSTAT.

For all results, a 5 REN ringing load of 1386 Ω + 40 μF capacitor was used. No additional loop resistance was added except for 30 Ω protection resistors. The loop supervision threshold was 10 mA.

For the L9215/16 traces, the following is true:

- Channel 1 represents SLIC control signal BR.
- Channel 2 represents SLIC loop supervision output NSTAT.
- Channel 3 represents SLIC output DCOUT.
- Channel 4 represents the ring voltage at PR.

As is seen in Figure 1, under these conditions with a 5 REN load, a glitch at NSTAT is present. The width of this glitch depends on the phase of the sine wave at the time of the state transition. An appropriate software filter is recommended to eliminate this glitch.

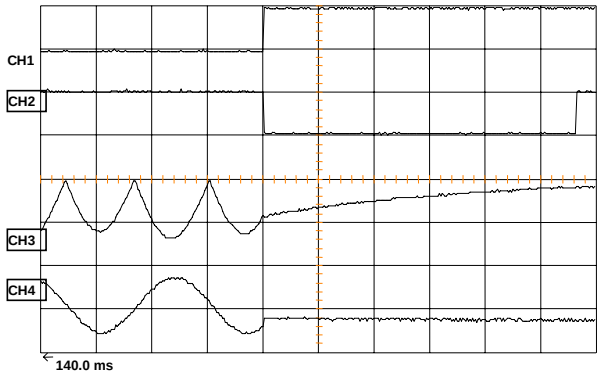

Figure 1. NSTAT Glitch

Control Signal Timing During Ring Cadence (continued)

Square Wave Input Mode of Operation

With the square wave approach, during nonring modes, the square wave input may also be left on at RINGIN. In this case the timing considerations that were discussed with the sine wave input mode of operation will also apply.

However with a square wave input, during nonring modes, the device can be operated by removing the square wave from RINGIN. In this mode of operation, unlike the sine wave case where only BR controls the ring cadence, both BR and the square wave input at RINGIN can be used to control the ringing cadence. This mode of operation has different considerations and advantages with respect to the NSTAT glitch compared to the sine wave approach. These considerations and advantages are discussed below.

For Figure 2:

- Channel 1 represents CMOS input (5 V) at RINGIN.
- Channel 2 represents BR and B0.
- Channel 3 represents NSTAT.

Note: B1 = B2 = 1

- Channel 4 represents ring.

Ring load = 5 REN = 1386 Ω + 40 μF, frequency = 20 Hz, V_{BAT} = –70 V, Vrms = 51 V, Vp-p = 67 V, crest factor = 1.3.

As is seen, when leaving the ring mode, there is a delay in the timing of toggling BR from low to high with respect to the timing of removing the square wave at RINGIN. The square wave at RINGIN is removed and BR is held low for the equivalent of one additional cycle of ringing (50 ms). Using this timing method, a very minimal glitch is seen at NSTAT during the state transition.

The delay method is also used when entering the ring mode. As is seen, the square wave at RINGIN is applied for two cycles of ringing before BR is toggled high to low. This timing eliminates any glitch at the NSTAT. Holding BR high for two cycles is conservative and in many cases 1 cycle may be adequate.

In any case, we do not recommend having no digital filtering of the NSTAT output. The purpose here is to minimize the length of the digital filter to a manageable time.

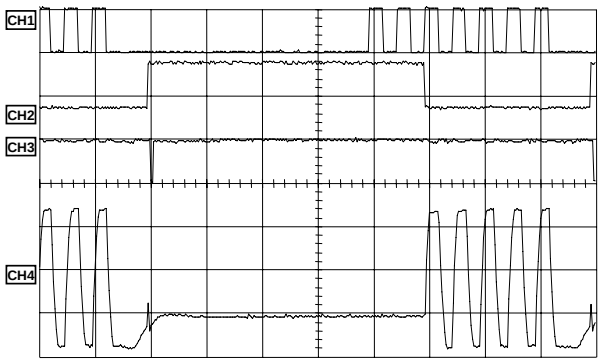

Figure 2. Square Wave Input Mode of Operation

State Transition

The following recommendations describe which state to switch to when switching out of the ring state during ring cadence or ring trip. The recommended operation for forward battery applications and ringing is to go from a forward battery high battery state, such as forward active (with or without PPM, if applicable) or forward scan state, to a forward battery portion of ringing (if possible). The ringing should end on the forward battery portion of the ringing cycle (if possible) and go to a forward active high battery state during the silent portion of ringing, or if a ring trip was detected. Transition to the scan state is also allowed if on-hook transmission is not required.

For reverse battery applications, transitions in and out of ringing should not cause a polarity reversal. It is recommended to transition from reverse battery high battery active to the reverse battery portion of ringing and back to reverse battery high battery active. With any SLIC, if the state transition causes a battery reversal, this will cause dc loop current to flow and cause a false loop status glitch at the loop closure detector. This is illustrated in Figure 3. Figure 3 uses the L8560 SLIC but results apply to any SLIC.

The figure below shows the effect of a simple battery reversal on NSTAT. The load was an 8 µF capacitor.

- Channel 1 represents SLIC control signals BR, B0, and B2.
- Channel 2 represents SLIC control signal B1.
- Channel 3 represents SLIC loop supervision output NSTAT.
- Channel 4 represents DCOUT.

The SLIC is in reverse battery when B1 is low, and is in forward battery when B1 is high. As is seen, a simple state transition from reverse to forward battery can cause a 50 ms glitch with a capacitive load. Conservative design practice will result in an appropriate deglitch at NSTAT after any state transition.

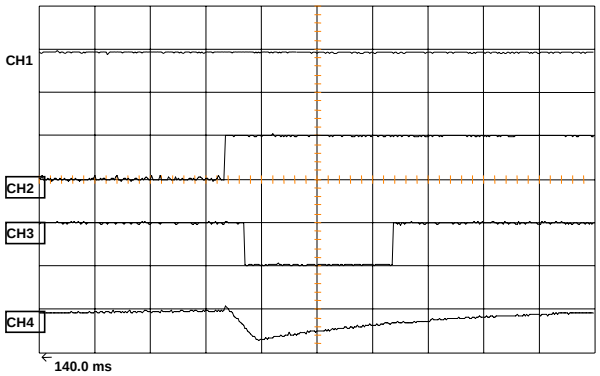

Figure 3. Effect of Battery Reversal on NSTAT

Transition from High Battery Active to Low Battery Active States

During ringing, scanning, or on-hook transmission modes, the SLIC T/R voltage is derived from the higher-voltage battery. Upon a legitimate off-hook condition, to minimize off-hook power, it is typical to use the SLIC battery switch feature to switch to the lower-voltage auxiliary V_{BAT2}. The L9215/16 SLIC has a battery switch that requires a logic control bit to switch from high battery to low battery.

However, if this transition is done in response to a dial pulse string, it can cause noise on adjacent lines due to the switching effect. If the lower-voltage battery has good drive capability, this effect will be minimal. Once a legitimate off-hook is recognized, it is recommended that a 500 ms delay be used prior to switching to low-voltage battery.

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