STANDARD
MICROSYSTEMS
CORPORATION

MIGRATION FROM LAN91C92 TO LAN91C94 (ISA MODE)

The LAN91C94 Ethernet controller chip is pin and register set compatible with the LAN91C92 for both the QFP and TQFP packages. For virtually all cases, the LAN91C94 will be a drop-in replacement for the LAN91C92. The LAN91C94 functions with the same drivers developed for the LAN91C92; however, in order to take advantage of the LAN91C94's Simultasking™ feature, updated drivers (available on SMSC's BBS) must be used.

ROM/PCMCIA* (PIN 95 ON QFP, PIN 93 ON TQFP)
On the LAN91C94, this is an I/O pin with an internal pullup resistor. If this pin is left open, the LAN91C94 will power up in ISA mode. If it is held low at the end of RESET, LAN91C94 will be configured for PCMCIA mode. This pin is an output on the LAN91C92, so it should be kept open for all existing designs.

EARLY TRANSMIT (SIMULTASKING™ FEATURE)
Early transmit allows the LAN91C94 to start transmitting to the network before the LAN91C94 is done writing the entire packet to the Transmit buffer. Setting the ETEN bit of POINTER register will initiate the transmission of the packet. If the TXUNRN bit of the EPH STATUS register is set, an underrun error has occurred. The LAN91C92 does not have an early transmit feature.

EARLY RECEIVE (SIMULTASKING™ FEATURE)
Early receive allows the LAN91C94 to start reading a packet while the packet is being received. The value written to the ERCV THRESHOLD of the EARLY RCV register determines when an ERCVINT interrupt is generated. The ERCV interrupt is generated whenever the number of bytes written in memory for the presently-received packet exceeds the ERCV THRESHOLD (value * 64bytes). In conjunction with early receive, a packet still in the process of being received can be discarded by setting the RCV DISCRD bit of the EARLY RCV register. The LAN91C92 does not have an early receive & discard feature.

MANAGEMENT INTERFACE REGISTER
This is a register that is unique to the LAN91C94. When the LAN91C94 is running with a software driver written for the LAN91C92, this register is not used.

REGISTER DESCRIPTION:

- XENDEC bit reflects the status of XENDEC* pin
- IOS0,IOS1,&IOS2 bits reflects the status of the corresponding pins.
- Setting MDOE low allows the serial interface pins (EEDO,EESK,EECS) to function normally.
  Setting MDOE high changes the function of the serial interface pins. This allows the MANAGEMENT register to drive the MDO & MCLK pins (EEDO & EESK respectively) and set EECS low.

REVISION REGISTER
The contents of the revision register for the LAN91C94 is 70H. This allows the software driver to distinguish the LAN91C94 from the LAN91C92 (which reads 33H) and the LAN91C100 (which reads 71H).

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RESET/PWRDWN

Setting the RESET pin of LAN91C94 will reset the chip regardless of the PWRDWN pin. In comparison, the LAN91C92 will not reset the chip if PWRDWN occurs less than 2usec after RESET.

PLL GAIN (K1 & K0 OF RCR REGISTER)

The PLL GAIN bits which are programmable on the LAN91C92 are low on the LAN91C94.

LNKLED

LNKLED does not turn on during RESET on LAN91C94. In comparison, LNKLED turns on during RESET regardless of LINK on the LAN91C92.

LAN91C94TQFP PACKAGE

The LAN91C94TQFP uses a 100VTQFP package which has a height of 1.0mm, whereas the LAN91C92TQFP uses a regular 100TQFP package which has a height of 1.4mm. All other dimensions of the two packages are the same. The difference in height of the two packages should have no effect on migrating to the 91C94TQFP. The LAN91C94 is a drop in replacement for the LAN91C92 for both the QFP and TQFP packages.