APPLICATION NOTE 8.6

STANDARD
MICROSYSTEMS
CORPORATION

Design Guidelines for the SMSC LAN83C183

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1.0 APPLICATION INFORMATION

80 Arkay Drive
Hauppauge, NY 11788
(516) 435-6000
FAX (516) 273-3123

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SMSC LAN83C183 Design Guidelines

1.0 APPLICATION INFORMATION

1.1 EXAMPLE SCHEMATICS

A typical example schematic of the LAN83C183 used in an adapter card application is shown in Figure 1, a hub application is shown in Figure 2, and an external PHY application is shown in Figure 3.

1.2 TP TRANSMIT INTERFACE

The interface between the Twisted Pair (here on referred to as TP) outputs on TPO± and the twisted pair cable is typically transformer coupled and terminated with the two resistors as shown in Figures 1 through 3. The transformer for the transmitter is recommended to have a winding ratio of 1:1 with a center tap on the primary winding tied to V_{DD}, as shown in Figures 1 through 3. The specifications for such a transformer are shown in Table 1. Sources for the transformer are listed in Table 2.

The transmit output needs to be terminated with two external termination resistors in order to meet the output impedance and return loss requirements of IEEE 802.3. It Is recommended that these two external resistors be connected from V_{DD} to each of the TPO± outputs, and their value should be chosen to provide the correct termination impedance when looking back through the transformer from the twisted pair cable, as shown in Figures 1 through 3. The value of these two external termination resistors depends on the type of cable driven by the device. Refer to the Cable Selection Section for more details on choosing the value of these resistors.

To minimize common mode output noise and to aid in meeting radiated emissions requirements, it may be necessary to add a common mode choke on the transmit outputs as well as add common mode bundle termination. The qualified transformers mentioned in Table 2 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 1 through 3. Common mode bundle termination maybe needed and can be achieved by tying the unused pairs in the RJ45 to chassis ground through 75 Ω resistors and a 0.01 μF capacitor, as shown in Figures 1 through 3.

To minimize noise pickup into the transmit path in a system or on a PCB, the loading on TPO± should be minimized and both outputs should always be loaded equally.

1.3 TP RECEIVE INTERFACE

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with external resistors as shown in Figures 1 through 3.

The transformer for the receiver is recommended to have a winding ration of 1:1, as shown in Figures 1 through 3. The specifications for such a transformer are shown in Table 1. Sources for the transformer are listed in Table 2.

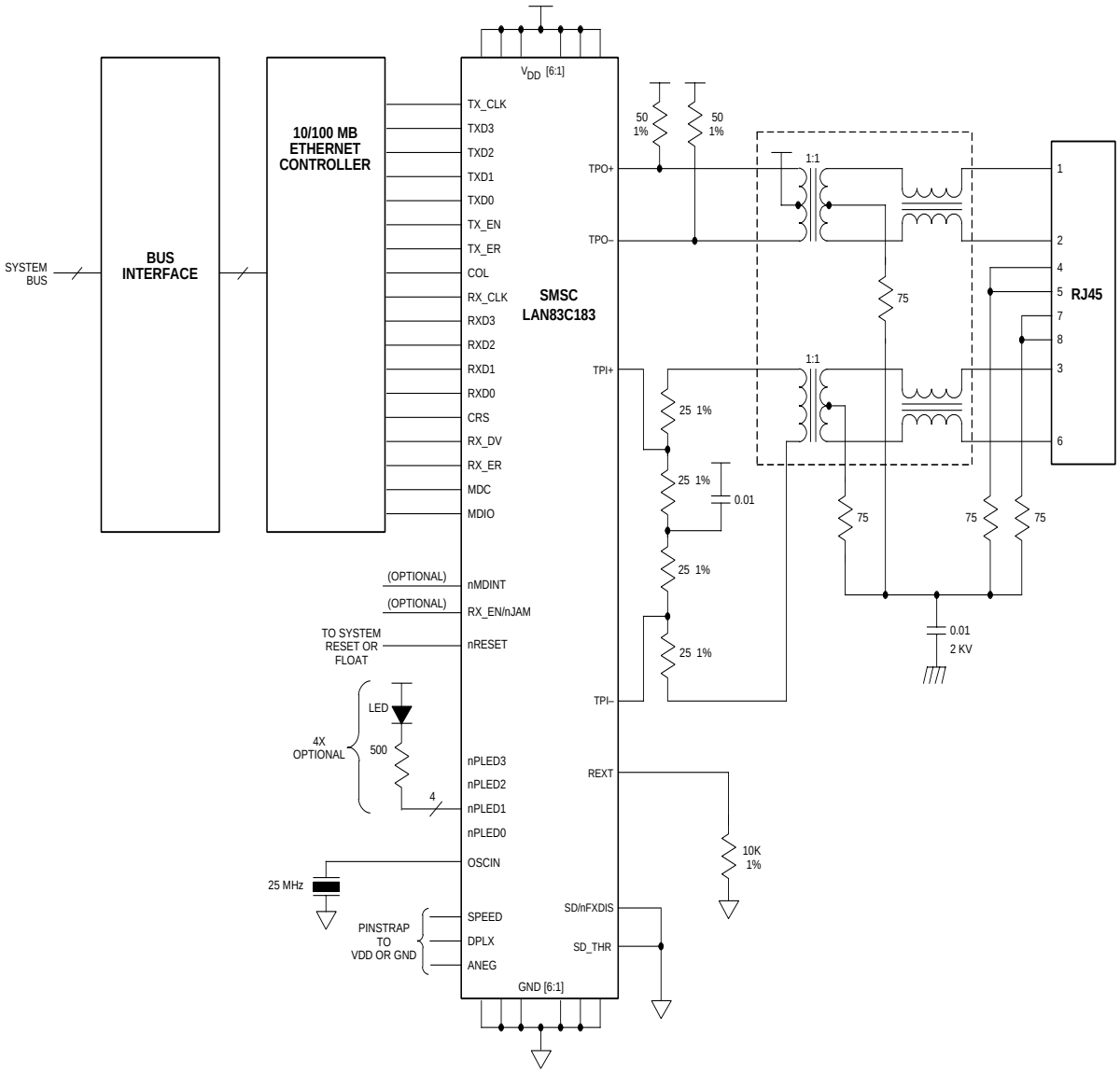

Figure 1. Typical Network Interface Card Schematic

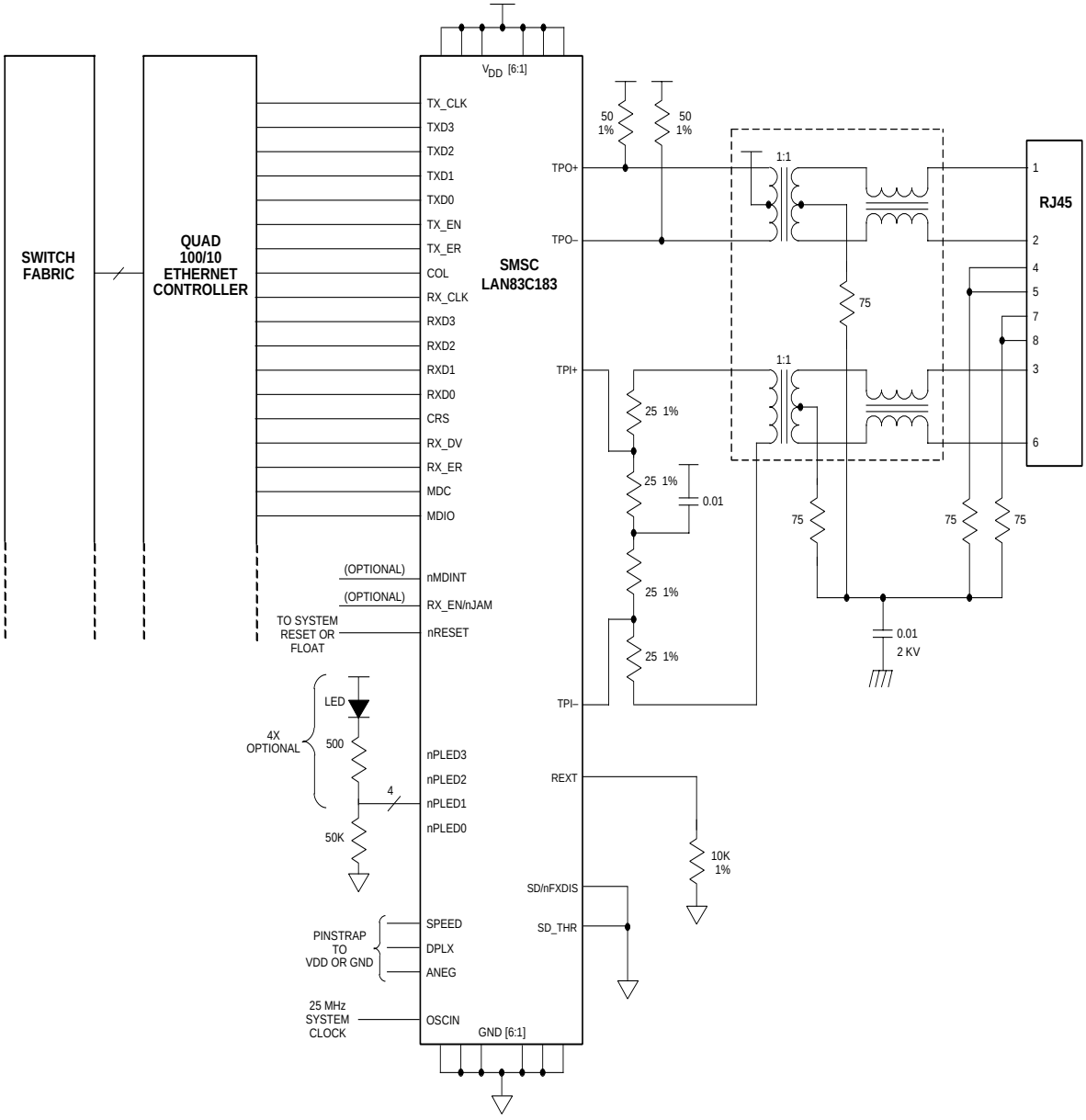

Figure 2. Typical Switching Port Schematic

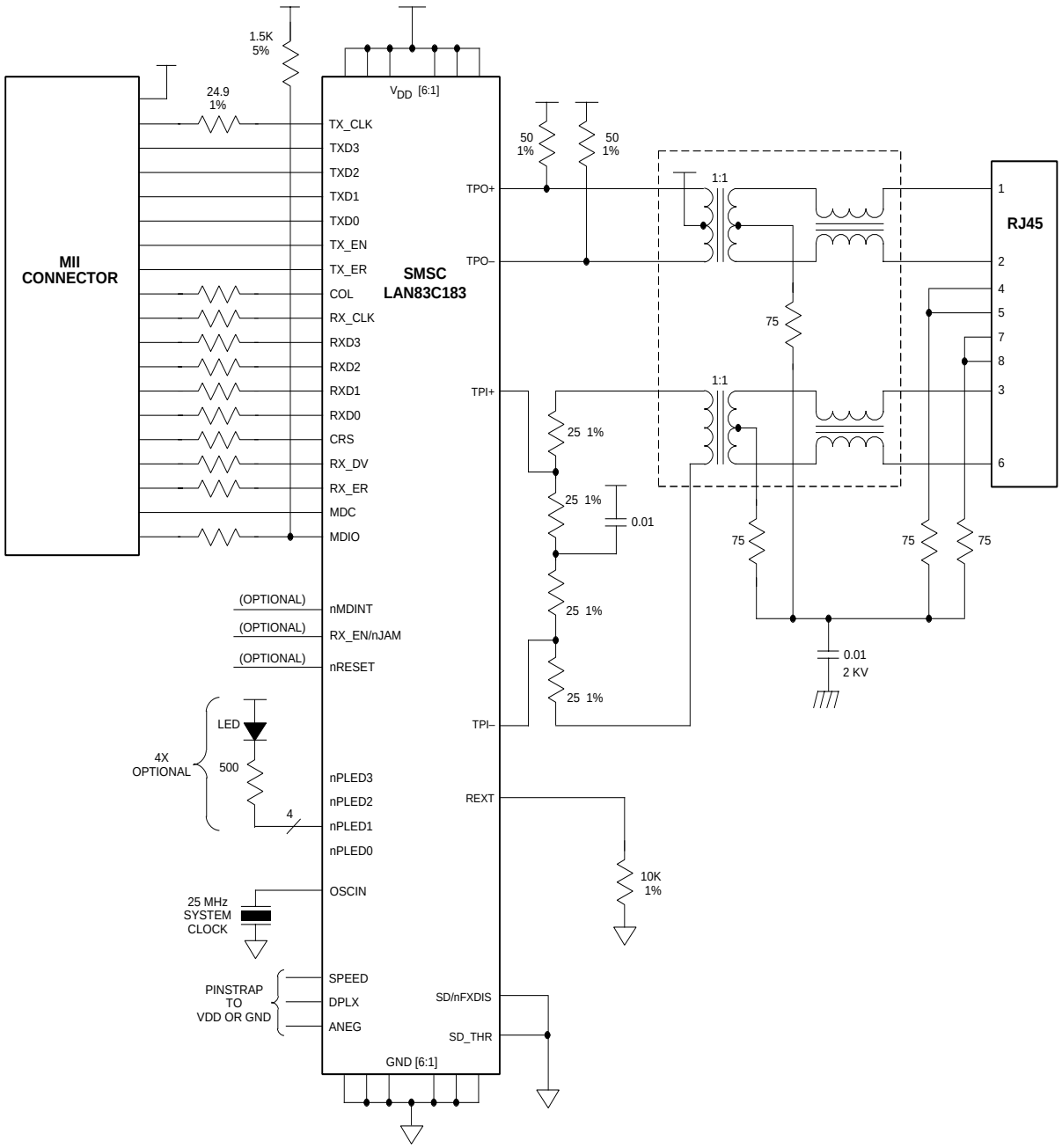

Figure 3. Typical External PHY Schematic

The receive input needs to be terminated with the correct termination impedance to meet the input impedance and return loss requirements of IEEE 802.3. In addition, the receive TP inputs need to be attenuated. It is recommended that both the termination and attenuation be accomplished by placing four external resistors in series across the TPI± inputs as shown in Figures 1 through 3. The resistors should be 25%/25%/25%/25% of the total series resistance, and the total series resistance should be equal to the Characteristic Impedance of the cable (100 Ω for UTP, 15O Ω for STP). It is also recommended that a 0.01 μF capacitor be placed between the center of the series resistor string and V_{DD} in order to provide an AC ground for attenuating common mode signal at the input. This capacitor is also shown in Figures 1 through 3.

To minimize common mode input noise and to aid in meeting susceptibility requirements, it may be necessary to add a common mode choke on the receive input as well as add common mode bundle termination. The qualified transformers mentioned in Table 2 all contain common mode chokes along with the transformers on both the transmit and receive sides, as shown in Figures 1 through 3. Common mode bundle termination may be needed and can be achieved by tying the receive secondary centertap and the unused pairs in the RJ45 to chassis ground through 75 Ω resistors and a 0.01 μF capacitor, as shown in Figures 1 through 3.

In order to minimize noise pickup into the receive path in a system or on a PCB, loading on TPI± should be minimized and both inputs should be loaded equally.

Table 1. TP Transformer Specification

Parameter	Specification	
	Transmit	Receive
Turns Ratio	1:1 CT	1:1
Inductance, (μH Min)	350	350
Leakage Inductance, (μH)	0.05 - 0.15	0.0-0.2
Capacitance (pF Max)	15	15
DC Resistance (Ω Max)	0.40	0.40

Table 2. TP Transformer Sources

Vendor	Part Number
HALO	TG22-3506ND
HALO	TG110-5050N2
BEL	S558-5999-J9
PULSE	H1102
PULSE	H1089

1.4 TP TRANSMIT OUTPUT CURRENT SET

The TPO± output current level is set by an external resistor tied between REXT and GND. This output current is determined by the following equation where R is the value of REXT:

$$I_{out} = (10K/R) \times I_{ref}$$

Where Iref = 40 mA (100 Mbps, UTP)
= 32.6 mA (100 Mbps, STP)
= 100 mA (10 Mbps, UTP)
= 81.6 mA (10 Mbps, STP)

REXT should be typically set to 10K Ω and REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels. Once REXT is set for the 100 Mbps and UTP modes as shown by the equation above, I_{ref} is then automatically changed inside the device when the 10 Mbps mode or UTP120 / STP150 modes are selected.

Keep the REXT resistor as close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Since the TP output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of the output current to compensate for external loading. One way to adjust the TP output level is to change the value of the external resistor tied to REXT. A better way to adjust the TP output level is to use the transmit level adjust register bits accessed through the MI serial port. These four bits can adjust the output level by -14% to +16% in 2% steps as described in Table 3.

1.5 CABLE SELECTION

The LAN83C183 can drive two different cable types (1) 100 Ω unshielded twisted pair, Category 5, or (2) 150 Ω shielded twisted pair.

The LAN83C183 must be properly configured for the type of cable in order to meet the return loss specifications in IEEE 802.3. This configuration requires setting a bit in the serial port and setting the value of some external resistors, as described in Table 3. The Cable Type Select bit in Table 3 is a bit in the MI serial port Configuration 1 register that sets the output current level for the cable type. R_{TERM} in Table 3 is the value of the termination resistors needed to meet the level and return loss requirements. The value for R_{TERM} on the TPO± outputs is for the two external termination resistors connected between V_{DD} to TPO±, the value for R_{TERM} on the TPI± inputs is for the sum of the four series resistors across TPI±, as shown in Figures 1 through 3. These resistors should be 1% tolerance. Also note that some output level adjustment maybe necessary due to parasitics as described in the TP Output Current section.

Table 3. Cable Configuration

Cable Type	Cable Type Select Bit (16.7)	R_{TERM} (Ω)	
		TPO±	**TPI±**
100 Ohm UTP, Cat 5	UTP	R_{TERM1} = 50 Ω R_{TERM2} = 50 Ω	$R_{TERM3} + R_{TERM4} + R_{TERM5} + R_{TERM6}$ = 100 Ω
150 Ohm STP	STP	R_{TERM1} = 75 Ω R_{TERM2} = 75 Ω	$R_{TERM3} + R_{TERM4} + R_{TERM5} + R_{TERM6}$ = 150 Ω

1.6 TRANSMITTER DROOP

The IEEE 802.3 specification has a transmit output droop requirement for 100Base-TX. Since the LAN83C183 TP output is a current source, it has no perceptible droop by itself. However, the inductance of the transformer added to the device transmitter output as shown in Figures 1 through 3 will cause droop to appear at the transmit interface to the TP wire. If the transformer connected to the LAN83C183 outputs meets the requirements in Table 1, the transmit interface to the TP cable will meet the IEEE 802.3 droop requirements.

1.7 FX INTERFACE

1.7.1 General

The FX interface is typically connected to an external fiber optic transceiver. The FX interface inputs are outputs are designed to drive 100 Ω differential loads. The FX interface can be directly coupled to either 3.3V or 5V fiber optic transceivers with minimum external components, as described in the following sections.

1.7.2 Connection to 3.3V Transceivers

The schematic for a typical connection of the LAN83C183 to an external 3.3V fiber transceiver is shown in Figure 4.

The 70 Ω and 173 Ω resistors on FXO± are used for 100 Ω termination and for biasing the LAN83C183 FX0± outputs to match the input range on the 3.3V fiber transceiver inputs. These resistors should be placed as close as possible on the PCB to the fiber optic transceiver inputs. In addition, the parasitic loading on FXO+ and FXO- should be kept to a minimum and matched as well as possible.

The 127 Ω and 83 Ω resistors on FXI± and SD/nFXDIS are used for 100 Ω termination and for biasing the 3.3V fiber transceiver outputs to match the input range on the LAN83C183 FX inputs. These resistors should be placed as close as possible on the PCB to the LAN83C183 fiber inputs. In addition, the parasitic loading on FXI+ and FXI- should be kept to a minimum and matched as well as possible.

In the 3.3V transceiver application, the SD_THR pin needs to be tied to GND, as shown in Figure 14. The SD/nFXDIS ECL trip level is determined by the SD_THR pin. The SD/nFXDIS internal buffer trip level needs to be set to V_{DD}- and must be referenced to the 3.3V supply. Tying SD_THR to GND causes the device to internally set the ECL trip point on the SD/nFXDIS input buffer to V_{DD} -1.3 and references it to the common 3.3 V supply.

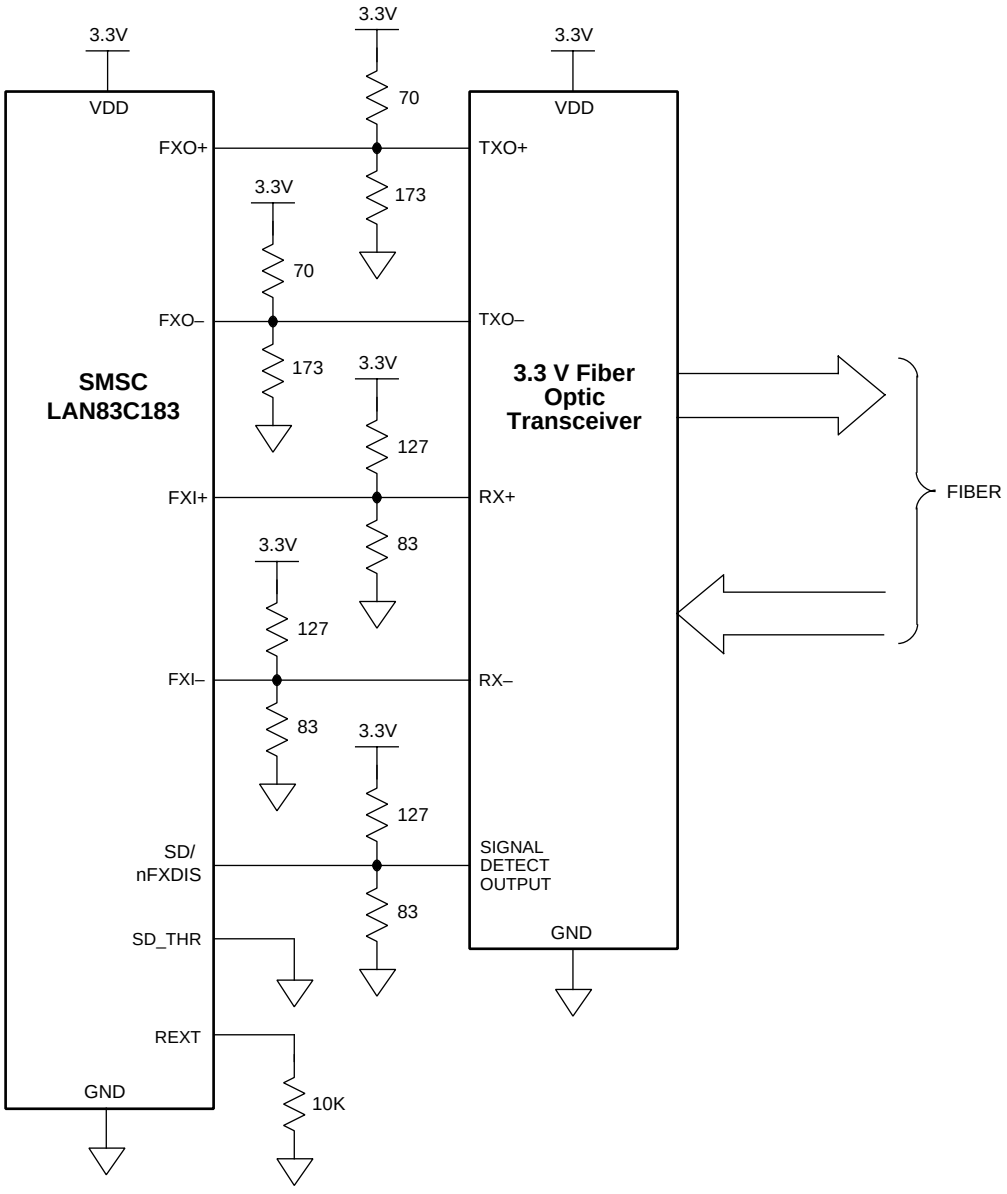

Figure 4. Connection to 3.3 Volt Fiber OpticTransceivers

1.7.3 Connection to 5V Transceivers

The schematic for a typical connection of the LAN83C183 to an external 5V transceiver is shown in Figure 5.

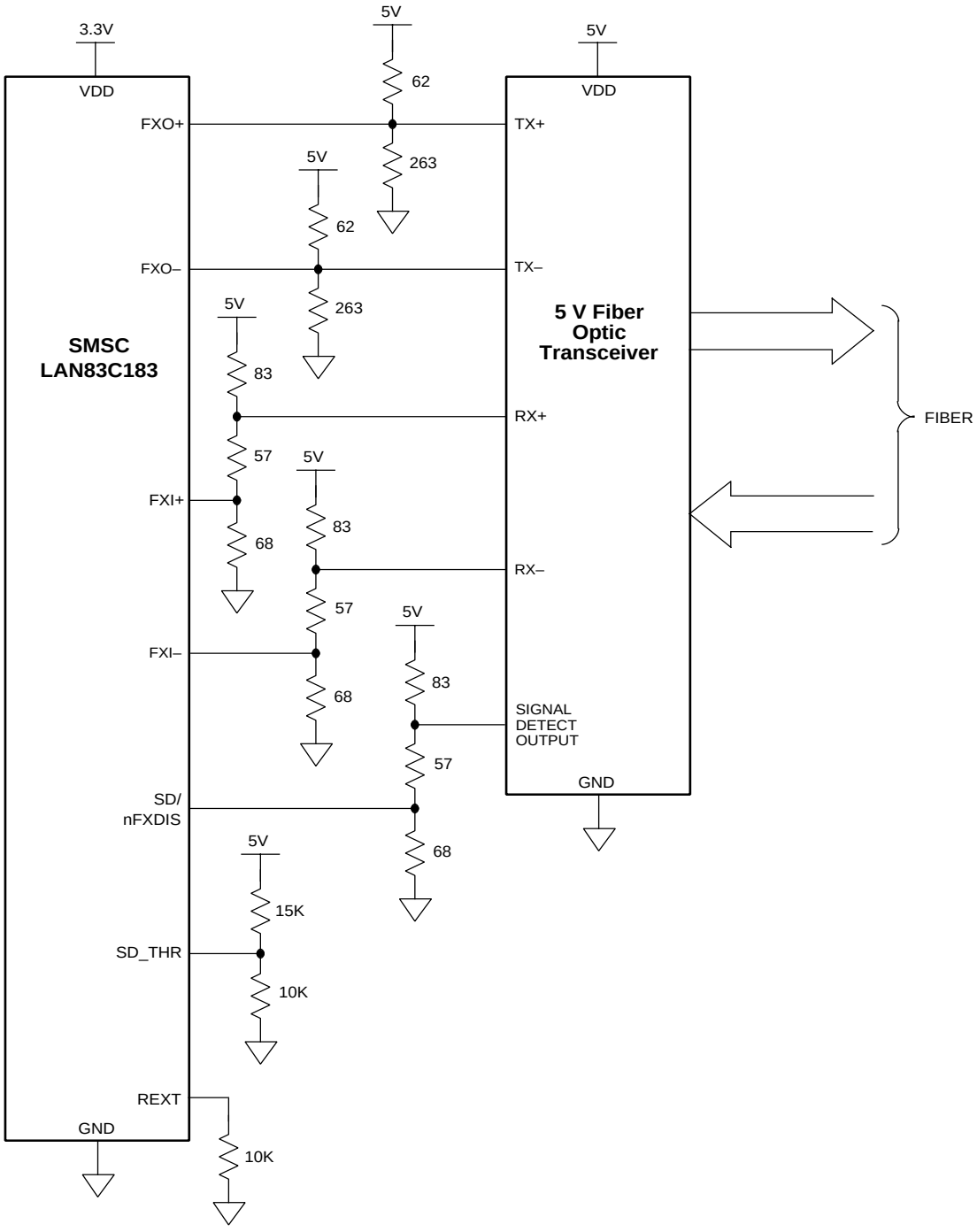

Figure 5. Connection to 5 Volt Fiber Optic Transceivers

The 62 Ω and 263 Ω resistors on FXO± are used for 100 Ω termination and for biasing the 3.3V LAN83C183 FXO± to match the input range on the 5V fiber transceiver inputs. These resistors should be placed as close as possible on the PCB to the fiber optic transceiver inputs. In addition, the parasitic loading on FXO+ and FXO- should be kept to a minimum and matched as well as possible.

The 83 Ω, 57 Ω and 68 Ω resistors on FXI± and SD/nFXDIS are used for 100 Ω termination and for biasing the 5V fiber transceiver outputs to match the input range on the 3.3V LAN83C183 FX inputs. These resistors should be placed as close as possible on the PCB to the LAN83C183 fiber inputs. In addition, the parasitic loading on FXI+ and FXI- should be kept to a minimum and matched as well as possible.

In the 5V transceiver application the SD_THR pin needs to be tied to V_{DD} -1.3V, which can be done with an external resistor divider as shown in Figure 5. The SD/nFXDIS ECL trip level is determined by the voltage on the SD_THR pin. The SD/nFXDIS internal buffer trip level needs to be set to V_{DD} -1.3V and must be referenced to the fiber transceiver 5V supply. Using a resistor divider from the fiber transceiver 5V supply to generate the voltage for the SD_THR pin references the SD/nFXDIS ECL trip level to the transceiver 5V supply. This allows the LAN83C183 SD/nFXDIS ECL trip level to track the supply variations of the fiber transceiver allowing direct connection of the fiber transceiver signal detect output to the LAN83C183 SD/nFXDIS input, as shown in Figure 5.

1.7.4 Disabling the FX Interface

The FX interface can be disabled by tying the SD/nFXDIS pin to GND, as shown in Figures 1 through 3. When the FX Interface is disabled, the TP interface is enabled, and vice versa.

1.8 MII CONTROLLER INTERFACE

1.8.1 General

The MII controller interface allows the LAN83C183 to connect to any external Ethernet controller without any glue logic provided that the external Ethernet controller has a MII interface that complies with IEEE 802.3, as shown in Figures 1 and 2.

1.8.2 Clocks

Standard Ethernet controllers with a MII use TX_CLK to clock data in on TXD[3:0]. TX_CLK is specified in IEEE 802.3 and on the LAN83C183 to be an output. If a nonstandard controller or other digital device is used to interface to the LAN83C183, there might be a need to clock TXD[3:0] into the LAN83C183 on the edges of an external master clock. The master clock, in this case, would be an input to the LAN83C183. This can be done by using OSCIN as the master clock input; since OSCIN generates TX_CLK inside the LAN83C183, data on TXD[3:O] can be clocked into the LAN83C183 on edges of output clock TX_CLK or input clock OSCIN. In the case where OSCIN is used as the input clock, a crystal is no longer needed on OSCIN, and TX_CLK can be left open or used for some other purpose.

1.8.3 Output Drive

The digital outputs on the LAN83C183 controller signals meet the MII driver characteristics specified in IEEE 802.3 and shown in Figure 6 if external 24.9 Ω, 1% termination resistors are added. These termination resistors are only needed if the outputs have to drive a MII cable or other transmission line type load, such as in the external PHY application shown in Figure 3. If the LAN83C183 is used in embedded applications, such as adapter cards and switching hubs shown in Figures 1 and 2, then these terminations resistors are not needed.

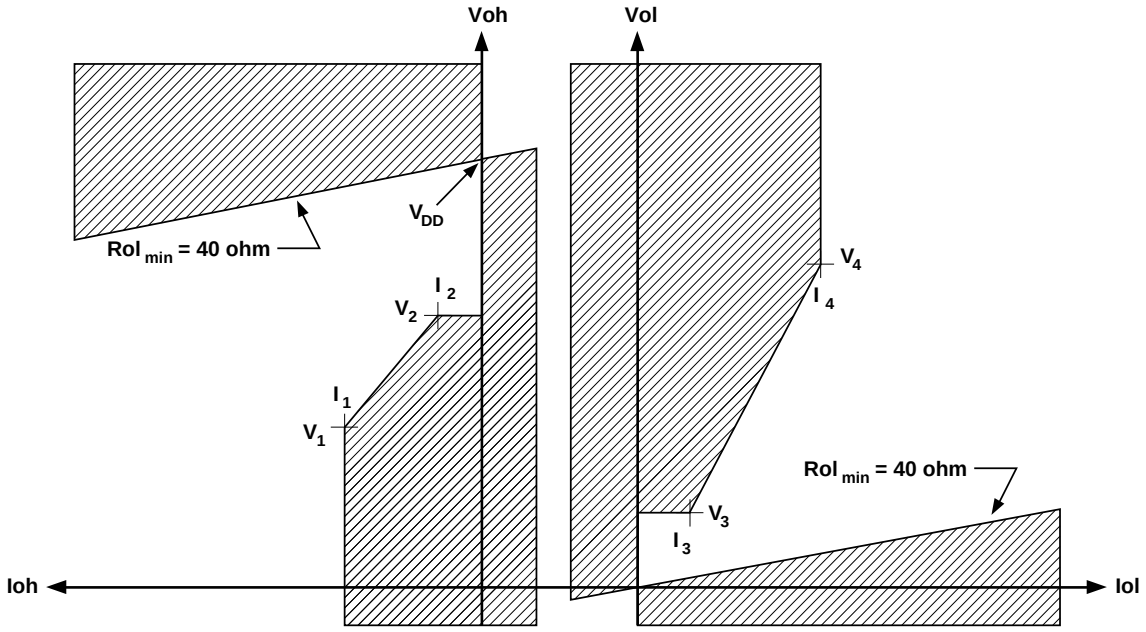

Figure 6. MII Output Drive

1.8.4 MII Disable

The MII outputs can be placed in the high impedance state and inputs disabled by setting the MII disable bit in the MI serial port Control register. When this bit is set to the disable state, the TP outputs are also disabled and transmission is inhibited. The default value of this bit when the device powers up or is reset is dependent on the physical device address. If the device address latched into MDA[4:0] at reset is 11111, it is assumed that the device is being used in applications where there maybe more than one device sharing the MII bus, like external PHY's or adapter cards, so the device powers up with the MII Interface disabled. If the device address latched into MDA[4:0] at reset is not 11111, it is assumed that the device is being used in an application where it is the only device on the MII bus, like hubs, so the device powers up with the MII interface enabled.

1.8.5 Receive Output Enable

The receive output enable pin, RX_EN, forces the receive and collision MII/FBI outputs into the high impedance state. More specifically, when RX_EN is deasserted, RX_CL K, RXD[3:0], RX_DV, RX_ER and COL are placed in high impedance.

RX_EN can be used to "wire OR" the outputs of many LAN83C183 devices in Multiport applications where only one device may be receiving at a time, like a repeater. By monitoring CRS from each individual port, the repeater can assert only the one RX_EN to that LAN83C183 device which is receiving data. The method will reduce, by 8 per device, the number of pins and PCB traces required by a repeater core IC.

The RX_EN function can be enabled by appropriately setting the R/J Configuration select bit in the MI serial port Configuration 2 register. When this bit is set, the RX_EN/nJAM pin becomes RX_EN.

1.9 FBI CONTROLLER INTERFACE

The FBI (Five Bit Interface) controller interface has the same characteristics of the Mll except that the data path is five bits wide, instead of 4 bits wide per the MII. The five bit wide data path is automatically enabled when the 4B5B encoder is bypassed. Because of this encoder/decoder bypass, the FBI is used primarily for repeaters or other applications where the full PHY is not needed. For more details about the FBI, see the Repeater Applications section.

1.10 REPEATER APPLICATIONS

1.10.1 MII Based Repeaters

The LAN83C183 can be used as the physical interface for MII based repeaters by using the standard Mll as the interface to the repeater core.

For most repeaters, it is necessary to disable the internal CRS loopback. This can be done be setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

For some particular types of repeaters, it maybe desirable to either enable or disable AutoNegotiation, force Half Duplex operation, and enable either 100 Mbps or 10 Mbps operation. All of these modes can be configured by setting the appropriate bits in the MI serial port Control register.

The LAN83C183 has a RPTR pin which will automatically configure the device for one common type of repeater application. When the RPTR pin is asserted (1) TX_EN to CRS loopback is disabled, (2) AutoNegotiation is disabled, (3) Half Duplex operation is selected, and (4) 100 Mbps operation is selected.

The MII requires 16 signals between the LAN83C183 and a repeater core, the MII signal count to a repeater core will be 16 multiplied by the number of ports, which can be quite large. The signal count between the LAN83C183 and repeater core can be reduced by 8 per device by sharing the receive output pins and using RX_EN to enable only that port where CRS is asserted. Refer to the Controller Interface section within the Applications section for more details about RX_EN.

1.10.2 Non-MII Based Repeaters

The FBI Interface available on the LAN83C183 can be used to connect to non-Mll based repeaters that employ the industry popular five bit wide interface.

Since the FBI is a 5 bit wide interface, it requires that the 4B5B encoder/decoder be bypassed. The FBI is automatically selected on the LAN83C183 when the 4B58 encoder decoder is bypassed. The 4B5B encoder/decoder can be bypassed by setting the bypass encoder/decoder select bit in the MI serial port Configuration 1 register. Some applications may also require the scrambler / descrambler to be bypassed. This can be done by setting the bypass scrambler / descrambler select bit in the MI serial port Configuration 1 register.

For most repeaters, it is necessary to disable the internal CRS loopback. This can be done be setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

For some particular types of repeaters, it may be desirable to either enable or disable AutoNegotiation, force Half Duplex operation, and enable either 100 Mbps or 10 Mbps operation. All of these modes can be configured by setting the appropriate bits in the MI serial port Control register.

The FBI requires 16 signals between the LAN83C183 and a repeater core. The FBl signal count to a repeater core will be 16 multiplied by the number of ports, which can be quite large. The signal count between the LAN83C183 and repeater core can be reduced by 8 per device by sharing the receive output pins and using RX_EN to enable only that port where CRS is asserted. Refer to the Controller Interface section within the Applications section for more details on RX_EN.

1.10.3 Clocks

Normally, transmit data over the MII/FBI is clocked into the LAN83C183 with edges from the output clock TX_CLK. It may be desirable or necessary in some repeater applications to clock in the transmit data from a master clock from the repeater core. This would require that transmit data be clocked in on edges of an input clock. An input clock is available for clocking in data on TXD with the OSCIN pin. Notice from the timing diagrams that OSCIN generates TX_CLK, and TXD data is clocked in on TX_CLK edges. This means that TXD data is also clocked in on OSCIN edges as well. Thus, an external clock driving the OSCIN input can also be used as the clock for TXD.

1.11 SERIAL PORT

1.11.1 General

The LAN83C183 has a MI serial port to access the devices's configuration inputs and readout the status outputs. Any external device that has an IEEE 802.3 compliant MII Interface can connect directly to the LAN83C183 without any glue logic, as shown in Figures 1 through 3.

As described earlier, the MI serial port consists of 8 lines: MDC, MDIO, nMDINT, and nMDA[4:0]. However, only 2 lines, MDC and MDI0, are needed to shift data in and out; nMD_INT and nMDA[4:0] are not needed but are provided for convenience only.

Note that the nMDA[4:0] addresses are inverted inside the LAN83C183 before going to the MII serial port block. This means that the nMDA[4:0] pins would have to be pin strapped to 11111

externally in order to successfully match the MI physical address of 00000 on the PHYAD[4:0] bits internally.

1.11.2 Polling vs. Interrupt

The status output bits can be monitored by either polling the serial port or with interrupt.

If polling is used, the registers can be read at regular intervals and the status bits can be checked against their previous values to determine any changes. To make polling simpler, all the registers can be accessed in a single read or write cycle by setting the register address bits REGAD[4:0] to 11111 and adding enough clocks to readout out all the bits, provided the multiple register access feature has been enabled.

The interrupt feature offers the ability to detect changes in the status output bits without register polling. Assertion of interrupt indicates that one or more of the status output bits has changed since the last read cycle. There are three interrupt output indicators on the LAN83C183: (1) nMDINTpin, (2) INT bit in the MI serial port Status Output register, and (3) Interrupt pulse on MDIO. These interrupt signals can be used by an external device to initiate a read cycle. Then when an interrupt is detected, the individual registers (or multiple registers) can be read out and the status bits compared against their previous values to determine any changes. After the interrupts have been read out, the interrupt signals are automatically deasserted. A mask register bit exists for every status output bit in the Mask register so that the interrupt bits can be individually programmed for each application.

1.11.3 Multiple Register Access

If the MI serial port needs to be constantly polled in order to monitor changes in status output bits, or if it is desired that all registers be read or written in a single serial port access cycle, multiple register access mode can be used. Multiple register access allows access to all registers in a single MI serial port access cycle. When multiple register access is enabled, then all the registers are read/written when the register address REGAD[4:0] = 11111. This eliminates the need to read or write registers individually. Multiple register access mode is normally disabled but it can be enabled by setting the multiple register access enable bit in the MI serial port Configuration 2 register.

1.11.4 Serial Port Addressing

The device address for the MI serial port are selected by tying the nMDA[4.-0] pins to the desired value. nMDA[4:0] share the same pins as the nMDINT and nPLED[3:0] outputs, respectively, as shown Figure 7a. On powerup or at reset, the output drivers are tri-stated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port address. The LED outputs are open drain with internal resistor pullup to V_{DD}.

If an LED is desired on the LED outputs, then an LED and resistor are tied to V_{DD} as shown in Figures 7b. If a high address is desired, then the LED to V_{DD} automatically makes the latched address value a high. If a low value for the address is desired, then a 50K Ω resistor to GND must be added as shown in Figure 7b.

If no LED's are needed on the LED outputs, the selection of addresses can be done as shown in Figure 7c. If a high address is desired, the pin should be left floating and the internal pullup will pull the pin high during power-on reset time and latch in a high address value. If a low address is desired, then the nMDINT and nPLED[3:0] output pins should be tied either directly to GND or through an optional 50K Ω resistor to GND. nPLED3 should always be tied through a 50K Ω resistor to GND since it has both pull up and pulldown capability. The optional 50K Ω resistor also allows the nMDINT and nPLED[2:0] pins to be used as digital outputs under normal conditions.

Note that the nMDA[4:0] addresses are inverted inside the LAN83C183 before going to the MI serial port block. This means that the nMDA[4:0] pins would have to be pin strapped to 11111 externally in order to successfully match the MI physical address bits PHYAD[4:0] = 00000 internally.

1.12 LONG CABLE

IEEE 802.3 specifies that 10Base-T and 100Base-TX operate over twisted pair cable lengths of between 0 - 100 meters. The squelch levels can be reduced by 4.5 dB if the receive level adjust bit is appropriately set in the MI serial port Configuration 1 register, which will allow the LAN83C183 to operate with up to 150 meters of twisted pair cable. The equalizer is already designed to accommodate between 0 - 125 meters of cable.

1.13 AUTOMATIC JAM

The LAN83C183 has an automatic nJAM generation feature which automatically transmits a nJAM packet when receive activity is detected. This feature is primarily designed to give the user a means to easily implement half duplex flow control. In a typical application a watermark signal from a system FIFO or memory would be tied directly to the nJAM pin. When the system FIFO is nearly full and more data is incoming from the receiver, the device will automatically transmit a nJAM packet and create a collision which will cause the far end device to backoff allowing time for the system FIFO to empty itself.

The nJAM generation feature requires that the RX EN/nJAM pin be programmed for nJAM. This can be done by appropriately setting the R/J configuration select bit in the MI serial port Configuration 2 register.

1.14 OSCILLATOR

The LAN83C183 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency can be generated by either connecting an external 25Mhz crystal between OSCIN and GND or by applying an external 25 Mhz clock to OSCIN. If the crystal oscillator is used, it needs only a crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 4. The crystal must be placed as close as possible to OSCIN and GND pins so that parasitics on OSCIN are kept to a minimum.

Table 4. Crystal Specifications

Parameter	Specification
Type	Parallel Resonant
Frequency	25 Mhz +/- 0.01 %
Equivalent Series Resistance	25 Ω max
Load Capacitance	18 ρF typical
Case Capacitance	7 ρF max
Power Dissipation	1 mW max

1.15 PROGRAMMABLE LED DRIVERS

The nPLED[5:0] outputs can all drive LED's tied to V_{DD} as shown in Figures 1 through 3. In addition, nPLED1 and nPLEDO can drive an LED tied to GND as well as V_{DD}. The nPLED[3:0] outputs can be programmed through the MI serial port to do 4 different functions (1) Normal Function (2) On, (3) Off, and (4) Blink.

nPLED[3:0] can be programmed to indicate 4 different sets of events with the LED Normal Function select bits in the Ml serial port Configuration 2 register. In addition, nPLED[3:0] can be user controlled by appropriately setting the LED output select bits in the MI serial port Configuration 2 register. When nPLED[3:0] is programmed for its Normal function, these outputs indicate the specific functions described in Table 5 and determined by the LED Normal Function select bits. When nPLED[3:0] is programmed to be On, the LED output driver go low, thus turning on the LED under user control. When nPLED[3:0] Is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control. When nPLED[3 0] is programmed to Blink, the LED outout driver will continuously blink at a rate of 100 mS on, 100 mS off.

The On and Off functions allow the LED driver to be controlled directly through the Ml serial port to indicate any function that is desired under external control. The Blink function allows the same external control of the LED driver and also offers the provision to blink the LED without the need for any external timers.

Table 5. LED Normal Function Definition

Bit 17.7	Bit 17.6	nPLED5	nPLED4	nPLED3	nPLED2	nPLED1	nPLED0
1	1	Rcv Act	Xmt Act	Link	Col	Full Dplx	10/100
1	0	Rcv Act	Xmt Act	Link	Act	Full Dplx	10/100
0	1	Rcv Act	Xmt Act	Link and Act	Col	Full Dplx	10/100
0	0	Rcv Act	Xmt Act	Link 100	Act	Full Dplx	Link 10

The nPLED[5:0] puts can also drive other digital inputs. Thus, nPLED[5:0] can also be used as digital outputs whose function can be user defined and controlled through the MI serial port.

Note that nPLED1 and nPLED0 pins have both pullup and pulldown transistors. This allows these pins to drive an LED from V_{DD} or to GND. When nPLED0 is programmed to be a 10/100 Mbps select, two LED's can be connected to this pin, one to V_{DD} to indicate that 100 Mbps mode is enabled, the other to GND to indicate that 10 Mbps mode is enabled. Similarly, when nPLED 1 is programmed to be a Half/Full Duplex Mode indication, two LED's can be connected to this pin, one to V_{DD} to indicate Full Duplex Mode is enabled, the other to GND to indicate Half Duplex Mode is enabled.

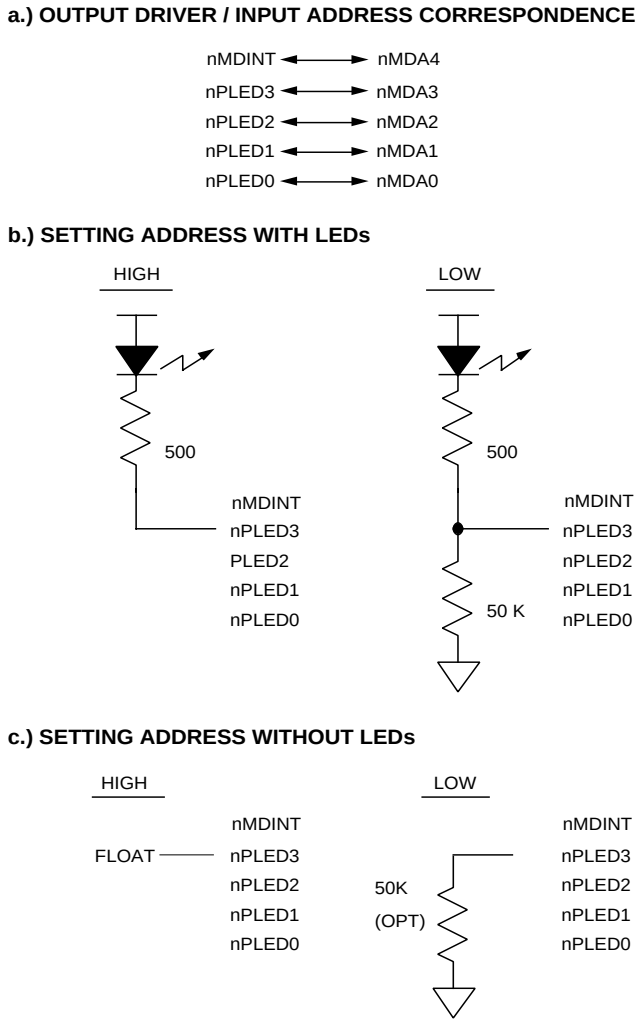

Figure 7. Configurable LEDs

1.16 POWER SUPPLY DECOUPLING

There are six V_{DD}s on the LAN83C183 (V_{DD}[6:1]) and six GND's (GND[6:1]). All six V_{DD}'s should be connected together as close as possible to the device with a large V_{DD} plane. If the V_{DD}s vary in potential by even a small amount, noise and latchup can result. The V_{DD}s should be kept to within 50 mV of each other.

All six GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result. The GNDs should be kept to within 50 mV of each other.

A 0.01 μF - 0.1 μF decoupling capacitor should be connected between each V_{DD} / GND set as close as possible to the device pins, preferably within 0.050". The value should be chosen on whether the noise from V_{DD} - GND is high or low frequency. A conservative approach would be to use two decoupling capacitors on each V_{DD} / GND set, one 0.1 μF for low frequency and one 0.001 μf for high frequency noise on the power supply.

The V_{DD} connection to the transmit transformer center tap shown in Figures 1 through 3 has to be well decoupled in order to minimize common mode noise injection from the supply into the twisted pair cable. And is recommended that a 0.01 μF decoupling capacitor be placed between the center tap V_{DD} to the S004 GND plane. This decoupling capacitor should be physically placed as close as possible to the transformer center tap, preferably within 0.20”.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to achieve the following when measured at the device: (1) The resultant AC noise voltage measured across each V_{DD} / GND set should be less than 100 mV pp, (2) All V_{DD}s should be within 50 mV pp of each other, and (3) All GND's should be within 50 mV pp of each other.