STANDARD
MICROSYSTEMS
CORPORATION

**APPLICATION NOTE 7.15**

# ACCESSING THE LAN83C171 (EPIC/XF) AND LAN83C175 (EPIC/C) CORRECTLY

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The EPIC controllers require the internal clock sources to be set correctly for the chip to function properly. The software drivers need to write to a test bit to set the internal clock source following power up and the following resets:

1) PCI or CardBus reset pin asserted while bit 17 of the General Control Register is clear(0).
2) Bit 0 of the General Control Register is set by the software driver.

If the clock source is not set correctly for the 33MHz bus operation, the EPIC controllers may be given a command yet no appropriate reaction may be noticed. With the incorrect clock setting, the controllers may miss host write attempts to the chip control registers. The mis-configuration is most easily noticed while attempting to transmit an Ethernet data packet.

The controller permits changing the source of the internal clocks. This is accomplished by writing one(1) to bit-3 (CLOCK TEST) of the Test register at offset 1Ch of the register space. All other bits of the Test register must be written as zero (0) during the CLOCK TEST write.

In order to set the CLOCK TEST bit in the Test register, perform the following:

- Write 0x0008 to the test register at least sixteen consecutive times.

The CLOCK TEST bit is write-only and cannot be read back for verification. Writing it several times consecutively insures a successful write to the bit. Once write command is executed to write to the CLOCK TEST bit sixteen times consecutively, the chip starts executing write commands always on the first time the host attempts. Writing to this bit can be made part of the chip initialization routine and only needs to be written after power up and resets.

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