Product Brief
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Lucent Technologies
Bell Labs Innovations

LU3X54FT
QUAD-FET for 10Base-T/100Base-TX/FX

Features

10 Mbits/s Transceiver

- Compatible with *IEEE* * 802.3 10Base-T standard for twisted-pair cable
- Autopolarity detection and correction
- Adjustable squelch level for extended line length capability (two levels)
- Interfaces with *IEEE* 802.3u media independent interface (MII) or a serial 10 Mbits/s 7-pin interface
- On-chip filtering eliminates the need for external filters
- Half- and full-duplex operations

100 Mbits/s TX Transceiver

- Compatible with *IEEE* 802.3u MII (clause 22), PCS (clause 23), PMA (clause 24), autonegotiation (clause 28), and PMD (clause 25) specifications
- Scrambler/descrambler bypass
- Encoder/decoder bypass
- 3-statable MII in 100 Mbits/s mode
- Selectable carrier sense signal generation (CRS) asserted during either transmission or reception in half duplex (CRS asserted during reception only in full duplex)
- Selectable MII or 5-bit code group interface
- Full- or half-duplex operations
- Optional carrier integrity monitor (CIM)
- On-chip filtering and adaptive equalization that eliminates the need for external filters

100 Mbits/s FX Transceiver

- Compatible with *IEEE* 802.3U 100Base-FX standard
- Reuses existing twisted-pair I/O pins for compatible fiber-optic transceiver pseudo-ECL (PECL) data:
  - — No additional data pins required
  - — Reuses existing LU3X54FT pins for fiber-optic signal detect (FOSD) inputs
- Fiber mode automatically configures port:
  - — Disables autonegotiation
  - — Disables 10Base-T
  - — Enables 100Base-FX remote fault signaling
  - — Disables MLT-3 encoder/decoder
  - — Disables scrambler/descrambler
- FX mode enable is pin- or register-selectable on an individual per-port basis.

General

- Autonegotiation (*IEEE* 802.3u, clause 28):
  - — Fast link pulse (FLP) burst generator
  - — Arbitration function
- Bused interfaces:
  - — Supports either separate 10 Mbits/s and 100 Mbits/s multiport repeaters (100 Mbits/s MII and 10 Mbits/s serial data stream), or single-chip multispeed repeaters
  - — Connects ports to either the 10 Mbits/s or 100 Mbits/s buses controlled by autonegotiation
  - — Separate TX_EN, RX_EN, CRS, and COL pins for each port
  - — Drivers on bused signal can drive up to eight LU3X54FTs (32 ports)

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

Features (continued)

General (continued)

- Supports the station management protocol and frame format (clause 22):
  - — Basic and extended registers
  - — Supports next-page function
  - — Operates up to 12.5 MHz
  - — Accepts preamble suppression
  - — Maskable status interrupts
- Supports the following management functions via pins if MII station management is unavailable:
  - — Speed select
  - — Carrier integrity enable
  - — Encoder/decoder bypass
  - — Scrambler/descrambler bypass
  - — Full duplex
  - — No link pulse mode
  - — Carrier sense select
  - — Autonegotiation
  - — 10 Mbits/s repeater reference select
  - — Internal 20 MHz clock synthesizer
  - — FX mode select
- Single 25 MHz crystal input or 25 MHz clock input, optional 20 MHz clock input
- Supports half- and full-duplex operations
- Provides six status signals:
  - — Receive activity
  - — Transmit activity
  - — Full duplex
  - — Collision/jabber
  - — Link integrity
  - — Speed indication
- Optional LED pulse stretching
- Per-channel powerdown mode for 10 Mbits/s and 100 Mbits/s operation
- Loopback for 10 Mbits/s and 100 Mbits/s operation
- Internal pull-up or pull-down resistors to set default powerup mode
- 0.35 μm low-power CMOS technology
- 208-pin SQFP
- Single 5 V power supply

Description

Configuration

The LU3X54FT is a four-channel, single-chip complete transceiver designed specifically for dual-speed 10Base-T, 100Base-TX, and 100Base-FX repeaters and switches. It supports simultaneous operation in three separate *IEEE* standard modes: 10Base-T, 100Base-TX, and 100Base-FX.

Each channel implements:

- 10Base-T transceiver function of *IEEE* 802.3.
- Physical coding sublayer (PCS) of *IEEE* 802.3u.
- Physical medium attachment (PMA) of *IEEE* 802.3u.
- Autonegotiation of *IEEE* 802.3u.
- MII management of *IEEE* 802.3u.
- Physical medium dependent (PMD) of *IEEE* 802.3.

The LU3X54FT supports operations over two pairs of unshielded twisted-pair (UTP) cable (10Base-T and 100Base-TX), and over fiber-optic cable (100Base-FX).

It has been designed with a flexible system interface that allows configuration for optimum performance and effortless design. The individual per-port interface can be configured as 100 Mbits/s MII, 10 Mbits/s MII, 7-pin 10 Mbits/s serial, or bused mode.

Bused MII Mode

The LU3X54FT has been designed for operation in two basic system interface modes of operation:

- **Normal MII Mode (Four Separate MII Ports).** The separate mode provides four independent RJ-45 to MII ports and is similar to having four independent 10/100 transceivers.
- **Bused MII Mode.** This mode is designed specifically for repeater applications to save pins. In bused mode:
  - — Data from all of the ports operating at 100 Mbits/s will be internally bused to system interface port A (100 Mbits/s MII interface).
  - — Data from all of the ports operating at 10 Mbits/s will be internally bused to system interface port B (7-pin 10 Mbits/s serial interface).

The LU3X54FT will automatically detect the speed of each port (10 Mbits/s or 100 Mbits/s) and route the data to the appropriate port.

Description (continued)

Bused MII Mode (continued)

The bused mode has two additional submodes of operation:

- **Seperate Bused MII Mode**. This mode is designed to operate with two independent repeater ICs, one repeater operating at 100Mbits/s and the other operating at 10 Mbits/s
- **Smart Bused MII Mode.** This mode is used when the LU3X54FT is communicating with a single (smart) 10/100 Mbits/s repeater IC, and allows the use of the security feature.

The bused interface allows each of the four transceivers to be connected to one of two system interfaces:

- Port A: 100 Mbits/s MII interface.
- Port B: 7-pin 10 Mbits/s serial interface.

This configuration allows 10/100 Mbits/s segment segregation or port switching with conventional multiport shared-media repeaters.

The port speed configuration and connection to the appropriate bused output is done automatically and is controlled by autonegotiation.

Figure 1 gives a functional overview of the LU3X54FT.

Clocking

The LU3X54FT requires an internal 25 MHz clock and a 20 MHz clock to run the 100Base-TX transceiver and 10Base-T transceiver.

These clocks can be supplied as follows:

- As separate clock inputs: 25 MHz and 20 MHz.
- The 20 MHz clock can be internally synthesized from the 25 MHz clock.
- The 25 MHz clock can also be internally generated by an on-chip oscillator if an external crystal is supplied.

The LU3X54FT will automatically detect if a 25 MHz clock is supplied, or if a crystal is being used to generate the 25 MHz clock.

Either the on-chip 20 MHz clock synthesizer (default clock) can be used, or H-DUPLED[A]/CLK20_SEL (pin 198) can be pulled high (sensed on powerup and reset) to select the external 20 MHz clock input.

FX Mode

Each individual port of the LU3X54FT can be operated in 100Base-FX mode by selecting it through the pin program option (RXLED[D:A]/FX_MODE_EN[D:A], or through the register bit (register 29, bit 0).

When operating in FX mode, the twisted-pair I/O pins are reused as the fiber-optic transceiver I/O data pins, and the fiber-optic signal detect (FOSD) inputs are enabled.

When a port is placed in FX mode, it will automatically configure the port for 100Base-FX operation (and the register bit control will be ignored) such that:

- The far-end fault signaling option will be enabled.
- The MLT-3 encoding/decoding will be disabled.
- Scrambler/descrambler will be disabled.
- Autonegotiation will be disabled.
- The signal detect inputs will be activated.
- 10Base-T will be disabled.

“Notes”

Description (continued)

Functional Block Diagrams

Device Overview

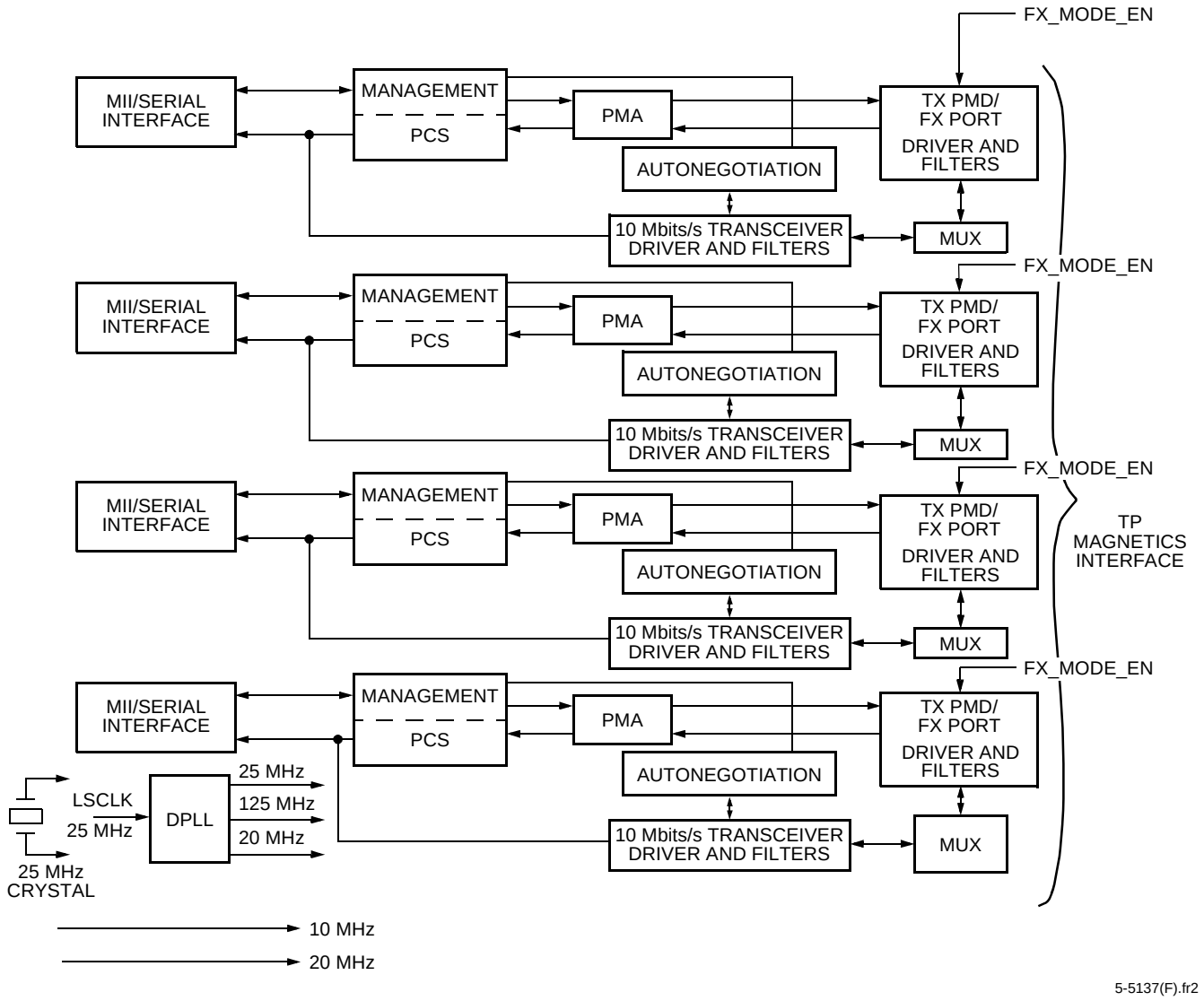

Figure 1. LU3X54FT Device Overview

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 316**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1189 324 299**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Bracknell),

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