LF3312
12-Mbit Frame Buffer / FIFO

Advance Information

FEATURES

- ❑ 12,441,600-bit Frame Memory
- ❑ May be Organized Into the Following Configurations:
  - 1,555,200 x 8-bit (single channel)
  - 1,244,160 x 10-bit (single channel)
  - 1,036,800 x 12-bit (single channel)
  - 777,600 x 16-bit (single channel)
  - 622,080 x 20-bit (single channel)
  - 518,400 x 24-bit (single channel)
  - 777,600 x 8-bit (each of two parallel channels)
  - 622,080 x 10-bit (each of two parallel channels)
  - 518,400 x 12-bit (each of two parallel channels)
- ❑ Eight Operating Modes:
  - One-Channel Synchronous Shift Register (Single Clock Source)
  - One-Channel Framestore With Sequential Write and Random Access Read
  - One-Channel Framestore With Random Access Write and Sequential Read
  - One-Channel FIFO With Asynchronous I/O
  - Two-Channel Synchronous Shift Register (Single Clock Source)
  - FIFO + shift register; Channel B Synchronized to Channel A
  - Shift register + FIFO; Channel A Synchronized to Channel B
  - Two-Channel FIFO; Both Channels Sychronized to External Signal (a)

(a) power-up default mode

- ❑ Features in the Four Modes With Asynchronous FIFOs:
  - Near-Full/Empty Flags With Programmable Thresholds
- ❑ Features in the Six Purely Sequential (FIFO, shift register) Modes:
  - Up to 100 MHz Continuous Data Throughput Rate
- ❑ Features in the Two Random Access (non-FIFO) Modes:
  - Up to 27 MHz Data Rate
- ❑ LF3312s may be connected in parallel for HDTV, multiframe SDTV, etc.
- ❑ Built-in ITUR-656 TRS detection and synchronization
- ❑ User-Resettable Read and Write Pointers
- ❑ Choice of Control Interfaces
  - Two-wire Serial Microprocessor Interface
  - Eight-Wire Parallel Microprocessor Bus
- ❑ 100-lead PQFP
- ❑ Single 3.3V power supply, 5V-tolerant I/O

APPLICATIONS

- ❑ Field-Based or Frame-Based Comb Filtering
- ❑ Image or Data Sequence Capture
- ❑ Resynchronization of Data Streams
- ❑ Video Special Effects (Rotation, Zoom, Picture-in-Picture)
- ❑ Test Pattern Generation
- ❑ Motion Detection or Frame-to-Frame Correlation
- ❑ Closed Circuit or Security Camera Systems

DESCRIPTION

The LF3312 is a 12,441,600-bit memory chip which can be configured by the user into either a two-data-port single-channel or a four-data-port dual-channel architecture. The input data ports may be clocked simultaneously or asynchronously with one another and with the output ports. Although dynamic memory cells are employed, a built-in automatic self-refresh circuit makes the device appear fully static to the user. Since all internal pointers and registers are fully static, read and write operations can be interrupted for indefinite periods of time without loss of data, as long as a memory core clock signal (internally derived from the signal applied to the RCLK pin) of 6MHz to 50MHz is continuously provided, for refresh purposes. Using the four 12-bit data ports provided, the user can operate the chip as one or two 8-, 10-, or 12-bit channels or as a single 16-, 20-, or 24-bit channel, without wasting any memory resources. Since reads are non-destructive (in fact, self-refreshing), a given data value, once written into the memory core, may be read as many times as desired. A user requiring more storage can cascade up to ten LF3312s into a larger array. The device is controlled by sixteen instruction words of eight bits each, which may be programmed or verified via a standard 2-wire serial or 8-wire parallel microprocessor interface.

The 3-bit OPMODE control selects one of the chip's eight distinct operating modes, each of which has versatile submode options:

- 0) One-Channel Synchronous Shift Register (Single Clock; User-set Latency)
- 1) One-Channel Framestore With Sequential Write and Random Access Read
- 2) One-Channel Framestore With Random Access Write and Sequential Read
- 3) One-Channel FIFO With Asynchronous I/O
- 4) Two-Channel Synchronous Shift Register (Single Clock; User-set Latencies)
- 5) Two-Channel FIFO; Channel B Synchronized to Channel A
- 6) Two-Channel FIFO; Channel A Synchronized to Channel B
- 7) Two-Channel FIFO; Both Channels Sychronized to External Signal

In all modes, incoming data on AIN[11:0] are accepted on each rising edge of AWCLK for which $\overline{\text{AWEN}}$ is active (LOW). In two-channel modes (OPMODE = 4 - 7), incoming data on BIN[11:0] are accepted on each rising edge of BWCLK for which $\overline{\text{BWEN}}$ is LOW. Likewise, in all modes, data in the output register driving AOUT[11:0] are updated 2 RCLK cycles following each rising edge of RCLK for which $\overline{\text{AREN}}$ is LOW. In two-channel modes, data in the output register driving BOUT[11:0] are likewise updated 2 RCLK cycles following each rising edge of RCLK for which $\overline{\text{BREN}}$ is LOW. The user may independently tristate output ports AOUT[11:0] and BOUT[11:0] by bringing $\overline{\text{AOEA}}$ and $\overline{\text{BOE}}$, respectively, HIGH.

In the synchronous shift register modes (OPMODE = 0, 4, 5 (channel A only), or 6 (channel B only)), the user provides a single clock for both the input and output data and specifies a desired input-to-output data path latency (ALAT, BLAT) via the control interface. In the dual-channel modes (OPMODE = 4 - 7), the two channels' latencies need not be identical. When OPMODE = 0 or 4, AWCLK, BWCLK, and RCLK must be tied together, as should $\overline{\text{AWEN}}$, $\overline{\text{BWEN}}$, $\overline{\text{AREN}}$, and $\overline{\text{BREN}}$. When OPMODE = 5, AWCLK and RCLK must be tied together, as should $\overline{\text{AWEN}}$, $\overline{\text{AREN}}$, and $\overline{\text{BREN}}$. When OPMODE = 6, BWCLK and RCLK must be tied together, as should $\overline{\text{BWEN}}$, $\overline{\text{AREN}}$, and $\overline{\text{BREN}}$. When OPMODE = 7, $\overline{\text{AREN}}$ and $\overline{\text{BREN}}$ must be tied together if the user wishes to maintain output synchronicity.

DESCRIPTION Cont'd

In random access write mode (OPMODE = 2, $\overline{\text{ASET}}$ = 0, $\overline{\text{BSET}}$ = 1), on each active write clock cycle (rising edge of AWCLK = BWCLK for which $\overline{\text{AWEN}}$ = $\overline{\text{BWEN}}$ is LOW), the user directs the write pointer to any desired memory location, using what are otherwise the second channel data input and output ports. In this application, BOUT[11:0] denotes the vertical component, and BIN[11:0], the horizontal component, of a Cartesian set, or, if desired, the concatenation of BOUT[11:0] in front of BIN[11:0] represents a single 24-bit linear address. Offset circuitry within the LF3312 permits the user to gang several chips in parallel and to use them collectively as a single large memory. Data are read out sequentially by rising edges of RCLK, under the control of AREN (read enable), $\overline{\text{RSET}}$ (read pointer force to constant), and $\overline{\text{RCLR}}$ (read pointer clear to 0). Holding $\overline{\text{ASET}}$ LOW keeps the chip continuously in random access write mode. In single-chip mode (CASCADE=0), releasing $\overline{\text{ASET}}$ to its HIGH state causes the chip to continue to write sequentially from the last-loaded address, albeit still at the random access rate of up to 27MHz. (The chip's maximum data throughput rate in Random Access Write or Random Access Read mode is approximately 1/4 of that in the other modes.)

In random access read mode (OPMODE = 1, $\overline{\text{RSET}}$ = 0, $\overline{\text{BCLR}}$ = 1, MARK_SEL = 0), the user likewise controls the read pointer over ports BIN and BOUT. In this case, (single-address) writing is sequential and under the control of $\overline{\text{ACLR}}$, $\overline{\text{ASET}}$, and $\overline{\text{AWEN}}$. As in random access write mode, BOUT[11:0] represents the upper bits or the vertical address, whereas BIN[11:0] represents the lower bits or the horizontal address. In single-chip mode, releasing $\overline{\text{RSET}}$ HIGH causes the read address pointer to increment from its last randomly-assigned location.

In asynchronous single-channel FIFO mode (OPMODE = 3), the device can retime a data stream according to a read sync signal ($\overline{\text{RSET}}$ or $\overline{\text{RCLR}}$) and either ITU-R656 Timing Reference Signals (TRS) embedded within the incoming (video) data or the falling edge of a write sync signal applied to $\overline{\text{ACLR}}$, $\overline{\text{ASET}}$, or $\overline{\text{AMARK}}$. The input (write) and output (read) clocks need not be synchronous with one another, and the memory core will eventually fill or empty if they differ in average frequency. As it "fills," the host will begin to lose prestored data by writing over it before it has been read. If the memory core "empties," the host will begin to read a stored data sequence for a second time. In either case, when the read and write addresses reach equality, the "COLLIDE" flag will go high, to alert the host. The almost-full and almost-empty flags provide advance warning of these conditions whenever user-selected "fullness" or "emptiness" thresholds, expressed in approximate thirty-fourths of the memory core size, are exceeded. For example, if the 1/34 and 33/34 thresholds are enabled, flag APE will go HIGH whenever the read pointer lags behind the write pointer by less than 1/34 of the memory space, and flag APF will go HIGH whenever the read pointer leads the write pointer by this amount. (Calculations are performed modulo the total address space.) The data input and output are sequential and the timing between write and read sync signals dynamically determines the effective delay (depth) of the FIFO.

In dual-channel synchronous shift register mode (OPMODE = 4), the user supplies a single clock to AWCLK, BWCLK, and RCLK and loads the respective desired constant latency for each channel via the microprocessor bus. In this mode, $\overline{\text{AWEN}}$ and $\overline{\text{AREN}}$ must be tied together, as must $\overline{\text{BWEN}}$ and $\overline{\text{BREN}}$.

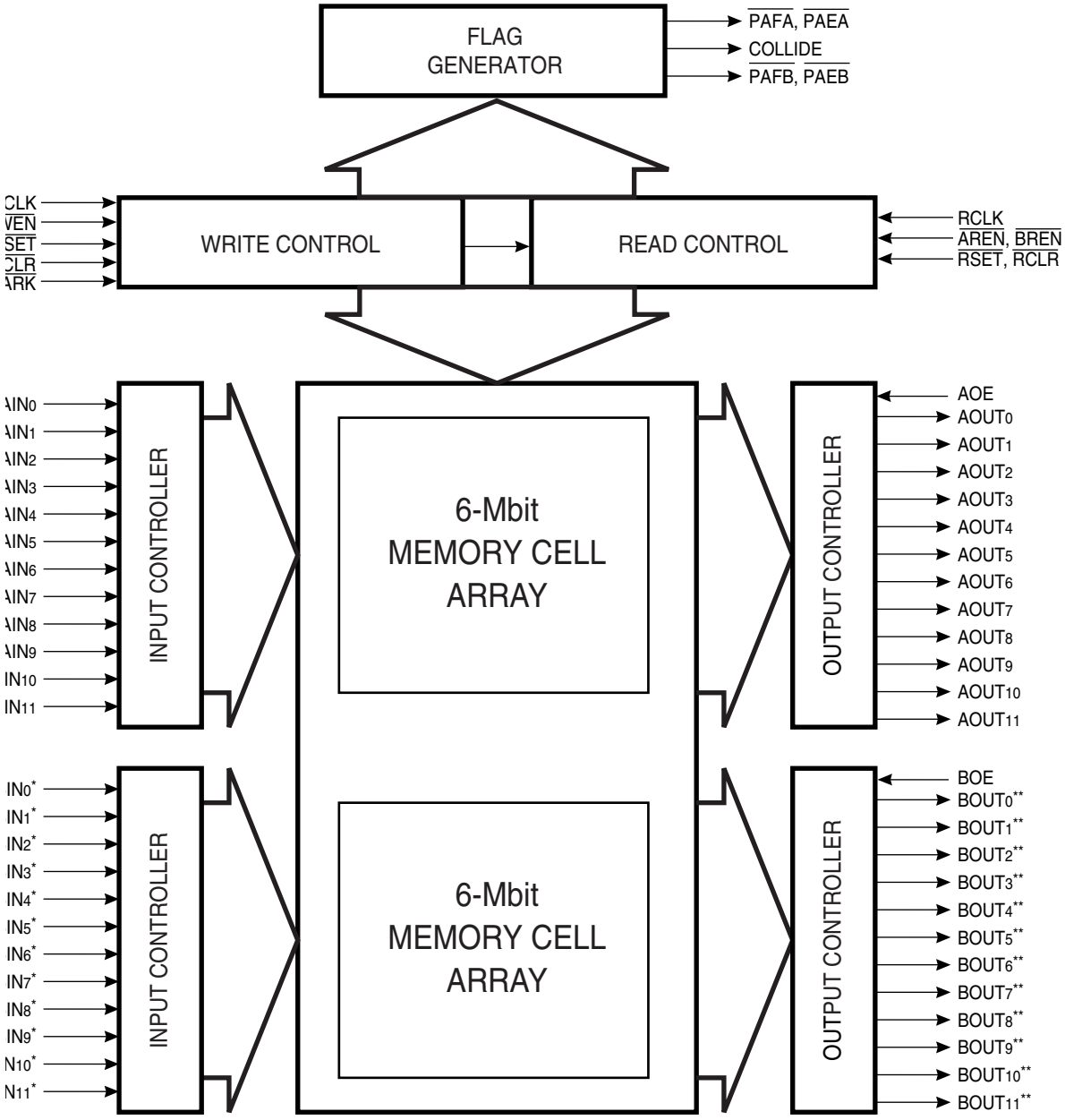
DESCRIPTION

In dual-channel master/slave mode (OPMODE = 5), channel A operates as a fully synchronous master shift register, to which the data in asynchronous FIFO channel B is retimed. The user drives AWCLK and RCLK from the incoming AIN data stream's sample clock, and BWCLK from the BIN data stream's clock. The user also specifies whether sync timing will be derived from TRS words embedded within the incoming data streams or from signals applied to AWACLR and WASETCLR or to AMARK and BMARK. AWEN and AREN must be tied together to maintain constant reference latency through channel A.

Dual-channel slave/master mode (OPMODE = 6) is identical, except that channel A is the slave FIFO and channel B is the master shift register, and RCLK needs to be tied to BWCLK, and BWEN needs to be tied to BREN.

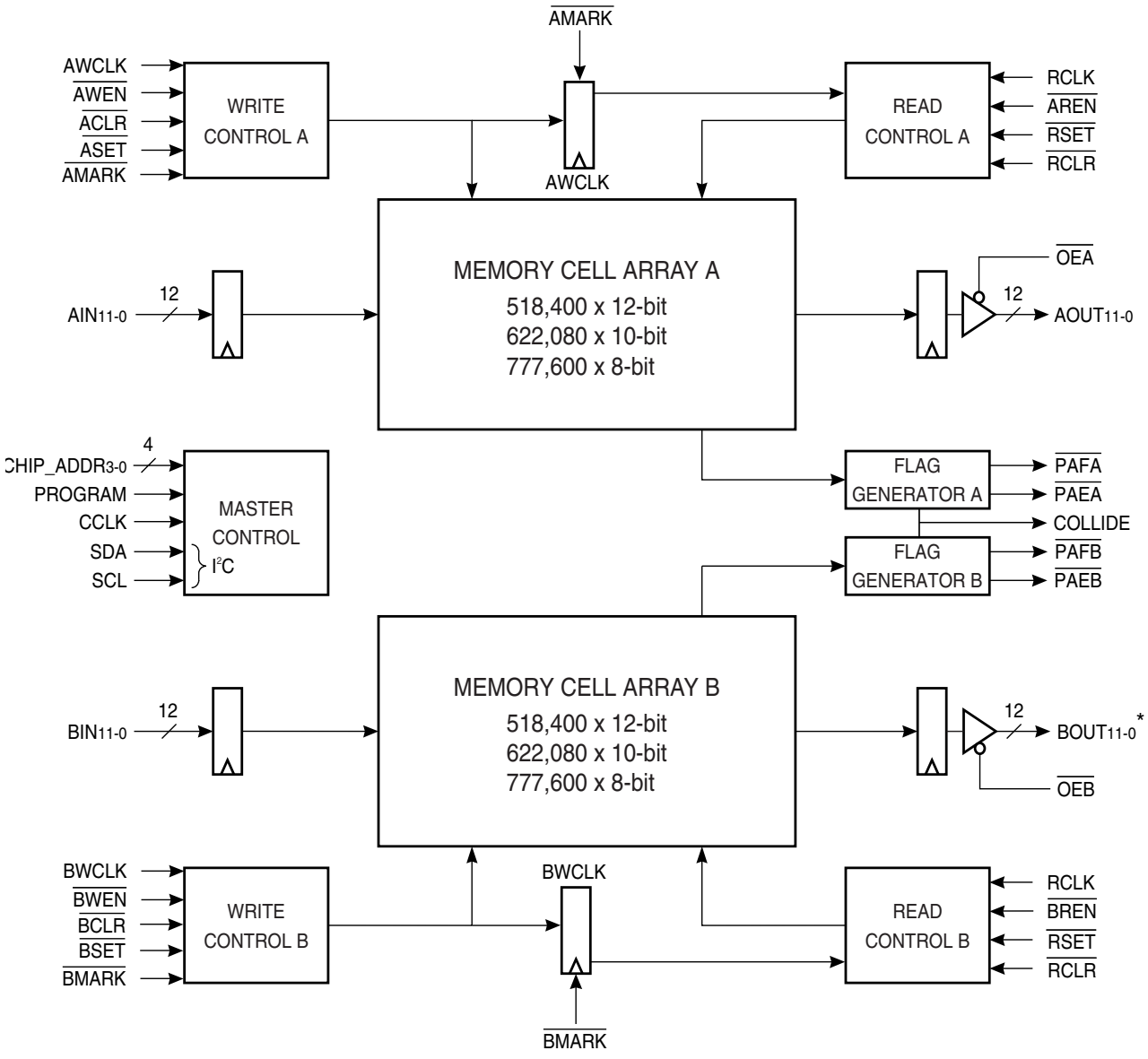
In dual-channel asynchronous FIFO mode (OPMODE = 7; power-on default), the device can accept two asynchronous data streams and automatically adjust the latency of each to bring it into alignment with an output sync signal applied to RSET or RCLR. Again, the user may reference input synchronization either to ACLR, ASET, BCLR, and BSET, to AMARK and BMARK, or to embedded TRS. The data read/output clock need not be synchronous with either of the two input clocks, which likewise need not be synchronous with one another.

LF3312 Functional Block Diagram



Doubles as lower portion of random address input
Doubles as upper portion of random address input or as parallel microprocessor port

Figure 1. Dual Channel FIFO Mode Functional Block Diagram



* PROGRAM pin must be LOW to enable BOUT as a data bus.

Figure 2. Single Channel FIFO Mode Functional Block Diagram

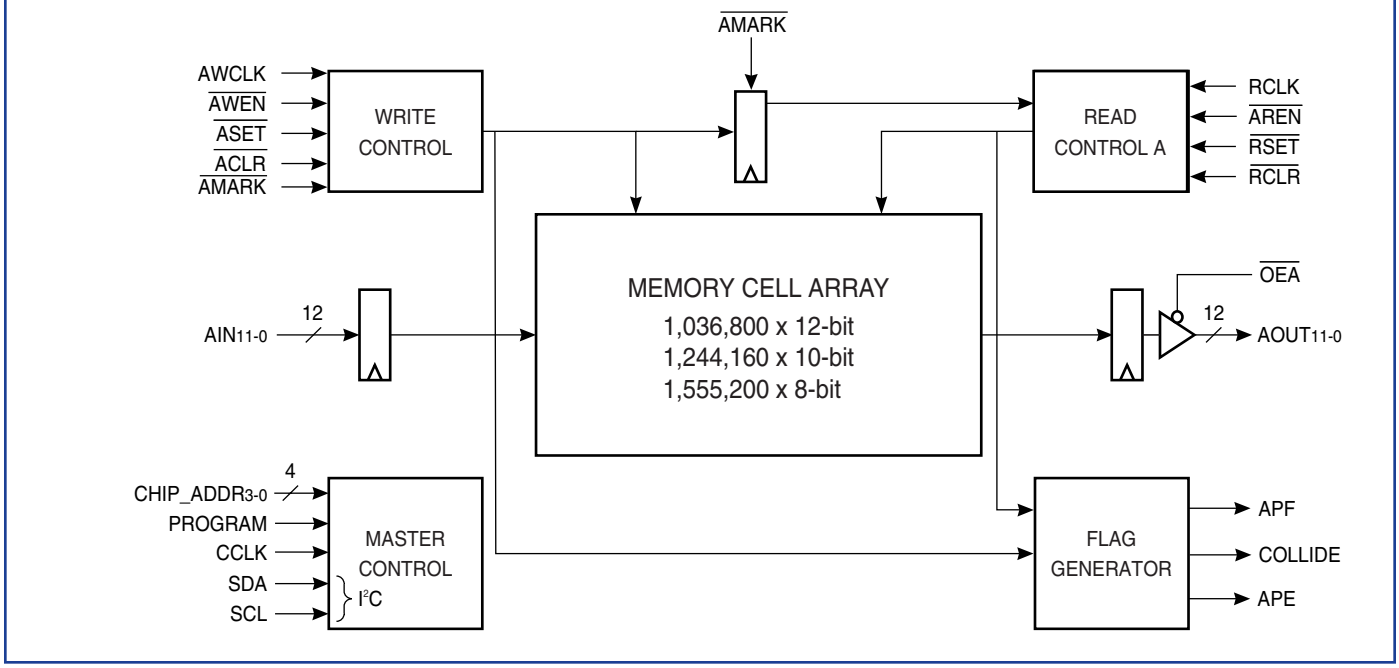
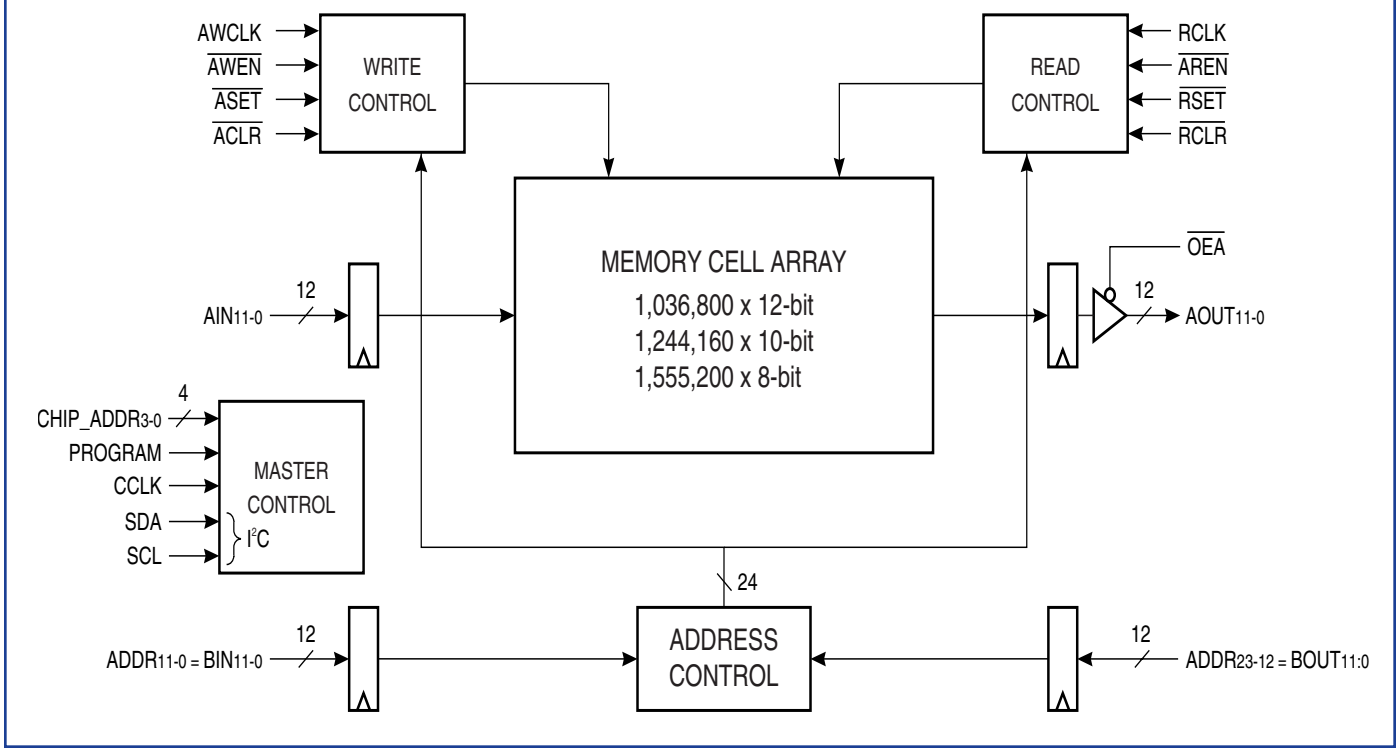


Figure 3. Random Access Mode Functional Block Diagram



FIFO Mode Signal Definition

Power

VCC and GND
+3.3V power supply. All pins must be connected.

Clocks

AWCLK - Write Clock A
Data present on AIN11-0 is written into the LF3312 on the rising edge of AWCLK when $\overline{\text{AWEN}}$ is LOW.

RCLK
Data is read from the LF3312 and presented on the output port (AOUT11-0) after a rising edge of RCLK while $\overline{\text{AREN}}$ and $\overline{\text{AOE}}$ are LOW. In two-channel mode, data is read from the LF3312 and presented on the output port (BOUT11-0) after a rising edge of RCLK while $\overline{\text{BREN}}$ and $\overline{\text{BOE}}$ are LOW.

BWCLK - Write Clock B
In two-channel mode, data present on BIN11-0 is written into the LF3312 on the rising edge of BWCLK when $\overline{\text{BWEN}}$ is LOW. In one-channel mode, BWCLK must be tied to AWCLK.

Inputs

AIN11-0 - Data Input A
AIN11-0 is the 12-bit registered data input port. Bit 11 is the MSB in all modes. AIN1-0 are ignored in 10-bit mode and AIN3-0 are ignored in 8-bit mode. Any such unused inputs should either be tied to ground or driven to proper logic levels by external logic.

BIN11-0 - Data Input B
BIN11-0 is the 12-bit registered data input port in all dual channel FIFO modes. Bit 11 is the MSB in all modes. BIN1-0 are ignored in 10-bit mode and BIN3-0 are ignored in 8-bit mode. Unused inputs should be tied off to ground or driven to proper logic levels by external logic.

$\overline{\text{ACLR}}$ - Channel A Write Pointer Clear
When $\overline{\text{ACLR}}$ is brought LOW, the next rising edge of AWCLK will bring the current value on AIN[11:0] into memory Channel A, address 0. Whenever $\overline{\text{ACLR}}$ is HIGH, the destination for AIN[11:0] will be controlled by $\overline{\text{ASET}}$. The user may program $\overline{\text{ACLR}}$ such that either its falling edge or its LOW state is active. If its LOW state is active, holding this pin LOW will hold the write address in its zero position continuously. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{BCLR}}$ - Channel B Write Pointer Clear / Channel A Write Random Select
In dual-channel modes (OPMODE = 4-7), this pin clears the Channel B Write Pointer, in the same manner that $\overline{\text{ACLR}}$ clears the Channel A Write Pointer, and the user may program it to be falling edge or LOW state active. In single-channel modes (OPMODE = 0-3), this pin and control MARKSEL govern the action of $\overline{\text{RSET}}$. In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

FIFO Mode Signal Definition

Inputs Cont'd

$\overline{\text{ASET}}$ - Channel A Write Pointer Set
This control is active only when $\overline{\text{ACLR}}$ is HIGH. Bringing $\overline{\text{ASET}}$ LOW will cause the next rising edge of AWCLK to bring the current value on AIN[11:0] into memory A, at the address specified by ALAT, or if OPMODE = 0-3 and $\overline{\text{BSET}}$ = 1, at the address whose Cartesian coordinates are present on BOUT and BIN. Whenever $\overline{\text{ASET}}$ and $\overline{\text{ACLR}}$ are HIGH, the next rising edge of AWCLK will bring the current AIN[11:0] data value into the next-higher address in sequence. $\overline{\text{ASET}}$ may be programmed to be either edge-triggered, in which case it affects the write pointer for only one clock cycle following a negedge, after which incrementing resumes, or level-triggered, in which case it affects the write pointer until it is brought HIGH. For continuous random access write operation, holding $\overline{\text{ASET}}$ LOW and programming it to be level-triggered will provide the needed continuous write pointer override. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{AMARK}}$ - Channel A Write Address Pointer Mark
In single-channel mode, bringing this bit LOW will cause an internal register to store a copy the current value of the write address pointer, for subsequent use in synchronizing the corresponding read address pointer to the same location. Unlike $\overline{\text{ACLR}}$ and $\overline{\text{ASET}}$, this control does not affect the write pointer value itself. The system must use $\overline{\text{AMARK}}$ instead of $\overline{\text{ACLR}}$ if the entire memory core can be filled between sequential falling edges of the sync reference signal. In contrast, the system must use $\overline{\text{ACLR}}$ or $\overline{\text{ASET}}$ to establish a definite relationship between the internal address and the data stream, as in random access read mode.

$\overline{\text{BSET}}$ - Channel B Write Pointer Set
In two-channel modes (OPMODE = 4-7), this pin's impact on the B write pointer is analogous to that of $\overline{\text{ASET}}$ on the A write pointer, and the user may program the pin's action to be either edge- or level-triggering. In one-channel modes, $\overline{\text{BSET}}$ determines whether $\overline{\text{ASET}}$ forces the write address pointer to ALAT ($\overline{\text{BSET}}$ = 0) or to BOUT,BIN ($\overline{\text{BSET}}$ = 1). In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

$\overline{\text{BMARK}}$ - Channel B Write Address Pointer Mark
(active in dual channel modes, OPMODE = 4-7) Bringing this bit LOW will cause an internal register to store a copy the current value of the Channel B write address pointer, for use in synchronizing the corresponding read address pointer to the same location. This signal does not affect the value of the memory B write address pointer itself.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. With this chip, it functions as a dedicated input, since this part cannot be the master on an two-wire serial microprocessor interface.

CHIP_ADDR3-0 - Chip Address
CHIP_ADDR3-0 determines the LF3312's address on the two-wire microprocessor bus. Each LF3312 chip's 7-bit two-wire serial microprocessor interface address is 1, 1, 0, CHIP_ADDR3, CHIP_ADDR2, CHIP_ADDR1, CHIP_ADDR0, where CHIP_ADDRx is "1" if that pin is pulled high, or a "0" if that pin is pulled low.

FIFO Mode Signal Definition

Inputs Cont'd

$\overline{RSET}$ - Read Address Pointer Set
In dual-channel modes (OPMODE = 4-7), if $\overline{AREN}$ is LOW, bringing $\overline{RSET}$ LOW will force read address pointer A to ALAT (MARKSEL HIGH) or to the value most recently captured by $\overline{AMARK}$ (MARKSEL LOW). If $\overline{BREN}$ is LOW, bringing $\overline{RSET}$ LOW will force read address pointer B to BLAT (MARKSEL HIGH) or to the value most recently captured by $\overline{BMARK}$(MARKSEL LOW). In single-channel modes (OPMODE = 0-3), if $\overline{AREN}$ is LOW, bringing $\overline{RESET}$ LOW will force the read address to the most recently marked value (MARKSEL LOW), to BLAT (MARKSEL HIGH and $\overline{BCLR}$ LOW), or to BOUT,BIN (MARKSEL HIGH and $\overline{BCLR}$ HIGH). This pin may be programmed to be either falling edge or level LOW active.

$\overline{RCLR}$ - Read Address Pointer Clear
Bringing $\overline{RCLR}$ LOW causes the next rising edge of RCLK to force the read address pointer (OPMODE 0-3) or pointers (OPMODE 4-7) to zero. This pin may be programmed to be active on its falling edge or in its LOW state. In single-channel mode, it can reset the read pointer only when $\overline{AREN}$ is LOW. In dual-channel mode, it can reset read pointer A only if $\overline{AREN}$ is LOW, and read pointer B only if $\overline{BREN}$ is LOW.

Input/Output

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire two-wire serial microprocessor interface.

Controls

$\overline{AWEN}$ - Write Enable A
If $\overline{AWEN}$ is LOW, data on AIN11-0 is written to the device on the rising edge of AWCLK. When $\overline{AWEN}$ is HIGH, the device ignores data on AIN.

$\overline{BWEN}$ - Write Enable B
If $\overline{BWEN}$ is LOW, data on BIN11-0 is written to the device on the rising edge of BWCLK. When $\overline{BWEN}$ is HIGH, the device ignores data on BIN.

$\overline{AREN}$ - Read Enable A
If $\overline{AREN}$ is LOW and the output port is enabled, data from Channel A is read and presented on AOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{AREN}$ goes HIGH, the last value loaded into Channel A output register will remain unchanged.

$\overline{BREN}$ - Read Enable B
If $\overline{BREN}$ is LOW and the output port is enabled, data from Channel B is read and presented on BOUT11-0 after tD has elapsed from the rising edge of RCLK. If $\overline{BREN}$ goes HIGH, the last value loaded into Channel B output register will remain unchanged.

PROGRAM -– Mode Override for Port BOUT
When PROGRAM is LOW, the contents of BOUT[11:0] are treated as signal sample data output (dual-channel modes, OPMODE = 4-7), or as data memory address inputs (single-channel modes). When PROGRAM is HIGH, the chip treats BOUT as a standard 8-bit parallel microprocessor interface, instead, irrespective of operating mode. In this mode, bits BOUT[11:4] are conditionally tristated by the parallel bus logic, whereas bits BOUT[3:0] are unconditionally tristated, to allow them to serve as dedicated microprocessor interface inputs.

FIFO Mode Signal Definition

LOAD – Instruction Load
Bringing asynchronous control LOAD LOW updates the working instruction latches to match the current contents of the instruction preload latches. Holding it LOW causes the working latches to reflect all ongoing instruction preloads. Holding it HIGH permits the user to preset the instruction preload latches to any desired configuration without disturbing the work in progress.

RESET - Global Reset
Bringing asynchronous control RESET LOW forces all state machines to 0 and holds them there until it is released HIGH. It also forces the control preload latch into a default single-channel FIFO state, if and only if LOAD is also LOW. To operate the chip in any other mode, the user may then preprogram the control registers via either the serial or the parallel microprocessor port. A followup LOAD command is then needed to cause the preprogramming to take effect. Pulsing RESET HIGH-LOW-HIGH while holding LOAD HIGH will reset the state machines, but will not change either the preload or the working latches.

Outputs

AOE - Output Enable A
When AOE is LOW, AOUT11-0 is enabled for output. When AOE is HIGH, AOUT11-0 is placed in a high-impedence state. In 10-bit modes, AOUT1-0 are unconditionally tristated. In 8-bit modes, AOUT3-0 are tristated. The flag outputs are not affected by AOE.

BOE - Output Enable B
In any dual-channel mode, when BOE is LOW, BOUT11-0 is enabled for output. When BOE is HIGH, or in any single-channel mode, BOUT11-0 is placed in a high-impedence state. In 10-bit modes, BOUT1-0 are tristated. In 8-bit modes, BOUT3-0 are tristated. The flag outputs are not affected by BOE. If PROGRAM is HIGH, BOUT becomes a standard 8-bit parallel microprocessor interface.

AOUT11-0 - Data Output A
AOUT11-0 is the 12-bit registered data output port. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when AREN is LOW.

BOUT11-0 - Data Output B
BOUT11-0 is the 12-bit registered data output port. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when BREN is LOW.

PAFA - Programmable Almost Full Flag A
PAFA goes low when the write pointer is (Full - N) locations ahead of the read pointer. N is the value stored in the PAFA register and has no default value. PAFA is synchronized to the rising edge of AWCLK.

PAFB - Programmable Almost Full Flag B
PAFB goes low when the write pointer is (Full - N) locations ahead of the read pointer. N is the value stored in the PAFB register and has no default value. PAFB is synchronized to the rising edge of BWCLK.

FIFO Mode Signal Definition

Output Cont'd

$\overline{PAEA}$ - Programmable Almost Empty Flag A
PAEA goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the $\overline{PAEA}$ register and has no default value. $\overline{PAEA}$ is synchronized to the rising edge of RCLK.

$\overline{PAEB}$ - Programmable Almost Empty Flag B
PAEB goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the PAEB register and has no default value. PAEB is synchronized to the rising edge of RCLK.

COLLIDE - Memory Read/Write Pointer Collision Flag
This flag goes high whenever the read and write addresses to the memory core (OPMODE 0-3) or within either of the two memory cores (OPMODE 4-7) are the same. By monitoring the partial full/empty flags, the user can ascertain the direction of approach, i.e., read pointer catching up with write (FIFO empty) or write pointer catching up with read (FIFO full).

Random Access Mode Signal Definition

Power

VCC and GND
+3.3V power supply. All pins must be connected.

Clocks

AWCLK - Write Clock A
Data present on AIN11-0 is written into the LF3312 (or the location addressed by ADDR23-0 in Random Write mode) on the rising edge of AWCLK when $\overline{AWEN}$ is LOW.

RCLK - Read Clock A
Data is read from the LF3312 (or the location addressed by ADDR23-0 in Random Read mode) and presented on the output port (AOUT11-0) after a rising edge of RCLK while $\overline{AREN}$ and AOE are LOW.

CCLK - Memory Test Clock
This pin may be used as an input to strobe the internal memory core.

Inputs

AIN11-0 - Data Input A
AIN11-0 is the 12-bit registered data input port. Bit 11 is the MSB in all modes. AIN1-0 is ignored in 10-bit mode and AIN3-0 is ignored in 8-bit mode. Any such unused inputs should be either tief off to ground or driven to proper logic levels by external logic.

ADDR23-0 - Memory Address
ADDR23-0 is the 24-bit read or write memory address. When the device is configured for Random Write, ADDR23-0 acts as the 24-bit write address. When the device is in Random Read, ADDR23-0 acts as the 24-bit read address.

SCL - Serial Clock Input
SCL is a standard two-wire serial microprocessor interface clock pin. With this chip, it functions as a dedicated input, since this part cannot be the master on an two-wire serial microprocessor interface.

Random Access Mode Signal Definition

Inputs Cont'd

CHIP_ADDR3-0 - Chip Address
CHIP_ADDR3-0 determines both the LF3312's address on the two-wire microprocessor bus and the base address of its internal memory core, in Random Access Modes.

Input/Output

SDA - Serial Data I/O
SDA is the standard bidirectional data pin of a two-wire serial microprocessor interface.

Controls

$\overline{\text{ACLR}}$ - Channel A Write Pointer Clear
When $\overline{\text{ACLR}}$ is brought LOW, the next rising edge of AWCLK will bring the current value on AIN[11:0] into memory Channel A, address 0. Whenever $\overline{\text{ACLR}}$ is HIGH, the destination for AIN[11:0] will be controlled by $\overline{\text{ASET}}$. The user may program $\overline{\text{ACLR}}$ such that either its falling edge or its LOW state is active. If its LOW state is active, holding this pin LOW will hold the write address in its zero position continuously. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{BCLR}}$ - Channel B Write Pointer Clear / Channel A Write Random Select
In dual-channel modes (OPMODE = 4-7), this pin clears the Channel B Write Pointer, in the same manner that $\overline{\text{ACLR}}$ clears the Channel A Write Pointer, and the user may program it to be falling edge or LOW state active. In single-channel modes (OPMODE = 0-3), this pin and control MARKSEL govern the action of $\overline{\text{RSET}}$. In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

$\overline{\text{ASET}}$ - Channel A Write Pointer Set
This control is active only when $\overline{\text{ACLR}}$ is HIGH. Bringing $\overline{\text{ASET}}$ LOW will cause the next rising edge of AWCLK to bring the current value on AIN[11:0] into memory A, at the address specified by ALAT, or if OPMODE = 0-3 and $\overline{\text{BSET}}$ = 1, at the address whose Cartesian coordinates are present on BOUT and BIN. Whenever $\overline{\text{ASET}}$ and $\overline{\text{ACLR}}$ are HIGH, the next rising edge of AWCLK will bring the current AIN[11:0] data value into the next-higher address in sequence. $\overline{\text{ASET}}$ may be programmed to be either edge-triggered, in which case it affects the write pointer for only one clock cycle following a negedge, after which incrementing resumes, or level-triggered, in which case it affects the write pointer until it is brought HIGH. For continuous random access write operation, holding $\overline{\text{ASET}}$ LOW and programming it to be level-triggered will provide the needed continuous write pointer override. This control takes effect only when $\overline{\text{AWEN}}$ is LOW.

$\overline{\text{BSET}}$ - Channel B Write Pointer Set
In two-channel modes (OPMODE = 4-7), this pin's impact on the B write pointer is analogous to that of $\overline{\text{ASET}}$ on the A write pointer, and the user may program the pin's action to be either edge- or level-triggering. In one-channel modes, $\overline{\text{BSET}}$ determines whether $\overline{\text{ASET}}$ forces the write address pointer to ALAT ($\overline{\text{BSET}}$ = 0) or to BOUT,BIN ($\overline{\text{BSET}}$ = 1). In OPMODES 4-7, this control takes effect only when $\overline{\text{BWEN}}$ is LOW.

$\overline{\text{AMARK}}$ - Channel A Write Address Pointer Mark
In single-channel mode, bringing this bit LOW will cause an internal register to store a copy the current value of the write address pointer, for subsequent use in synchronizing the corresponding read address pointer to the same location. Unlike $\overline{\text{ACLR}}$ and $\overline{\text{ASET}}$, this control does not affect the write pointer value itself. The system must use $\overline{\text{AMARK}}$ instead of $\overline{\text{ACLR}}$ if the entire memory core can be filled between sequential falling edges of the sync reference signal. In contrast, the system must use $\overline{\text{ACLR}}$ or $\overline{\text{ASET}}$ to establish a definite relationship between the internal address and the data stream, as in random access read mode.

Random Access Mode Signal Definition

Controls Cont'd

$\overline{AWEN}$ - Write Enable A
If $\overline{AWEN}$ is LOW, data on AIN11-0 is written to the device on the rising edge of AWCLK. When $\overline{AWEN}$ is HIGH, the device is not enabled for writing.

$\overline{AREN}$ - Read Enable A
If $\overline{AREN}$ is LOW and the output port is enabled, data from the Memory Cell Array is read and presented on AOUT11-0 after t_d has elapsed from the rising edge of RCLK. If $\overline{AREN}$ goes HIGH, the last value loaded into Channel A output register will remain unchanged.

PROGRAM - B Channel I/O Mode
During Random Access operation, PROGRAM must be set LOW, to treat the contents of BIN11-0 port and BOUT11-0 port as a 24-bit address. Bringing PROGRAM HIGH allows the user to program the chip.

$\overline{LOAD}$ – Instruction Load
Bringing asynchronous control $\overline{LOAD}$ LOW updates the working instruction latches to match the current contents of the instruction preload latches. Holding it LOW causes the working latches to reflect all ongoing instruction preloads. Holding it HIGH permits the user to preset the instruction preload lathes to any desired configuration without disturbing the work in progress.

$\overline{RESET}$ - Global Reset
Bringing asynchronous control $\overline{RESET}$ LOW forces all state machines to 0 and holds them there until it is released HIGH. It also forces the control preload latch into a default single-channel FIFO state, if and only if $\overline{LOAD}$ is also LOW. To operate the chip in any other mode, the user may then preprogram the control registers via either the serial or the parallel microprocessor port. A followup $\overline{LOAD}$ command is then needed to cause the preprogramming to take effect. Pulsing $\overline{RESET}$ HIGH-LOW-HIGH while holding $\overline{LOAD}$ HIGH will reset the state machines, but will not change either the preload or the working latches.

$\overline{AOE}$ - Output Enable A
When $\overline{AOE}$ is LOW, AOUT11-0 is enabled for output. When $\overline{AOE}$ is HIGH, AOUT11-0 placed in a high-impedence state. In 8-bit modes, AOUT11-8 is tristated. In 10-bit modes, AOUT11-10 is tristated. The flag outputs are not affected by $\overline{AOE}$.

Outputs

$\overline{RSET}$ - Read Address Pointer Set
In dual-channel modes (OPMODE = 4-7), if $\overline{AREN}$ is LOW, bringing $\overline{RSET}$ LOW will force read address pointer A to ALAT (MARKSEL HIGH) or to the value most recently captured by $\overline{AMARK}$ (MARKSEL LOW). If $\overline{BREN}$ is LOW, bringing $\overline{RSET}$ LOW will force read address pointer B to BLAT (MARKSEL HIGH) or to the value most recently captured by $\overline{BMARK}$ (MARKSEL LOW). In single-channel modes (OPMODE = 0-3), if $\overline{AREN}$ is LOW, bringing $\overline{RESET}$ LOW will force the read address to the most recently marked value (MARKSEL LOW), to BLAT (MARKSEL HIGH and $\overline{BCLR}$ LOW), or to BOUT,BIN (MARKSEL HIGH and $\overline{BCLR}$ HIGH). This pin may be programmed to be either falling edge or level LOW active.

Random Access Mode Signal Definition

Outputs Cont'd

$\overline{RCLR}$ - Read Address Pointer Clear

Bringing RCLR LOW causes the next rising edge of RCLK to force the read address pointer (OPMODE 0-3) or pointers (OPMODE 4-7) to zero. This pin may be programmed to be active on its falling edge or in its LOW state. In single-channel mode, it can reset the read pointer only when $\overline{AREN}$ is LOW. In dual-channel mode, it can reset read pointer A only if $\overline{AREN}$ is LOW, and read pointer B only if $\overline{BREN}$ is LOW.

AOUT11-0 - Data Output A

AOUT11-0 is the 12-bit registered data output port. In 10-bit mode, bits 1 and 0 are tristated. In 8-bit mode, bits 3-0 are tristated. All active bits are updated on each rising edge of RCLK when $\overline{AREN}$ is LOW.

Control Register Map

The various 8-bit control registers may be preprogrammed either through the BOUT port, with PROGRAM = 1, or through the serial microprocessor interface bus. Changes in preprogramming begin to affect the data path when $\overline{\text{LOAD}}$ is brought LOW. In each instance, the value in parens () is the state following assertion of $\overline{\text{RESET}}$ while $\overline{\text{LOAD}}$ = 0.

Instruction Register 0 (dflt = 10_00_0_111)

7:6 = WIDTH[1:0]	(10: 10 bits)
5:4 = MCLK_RATE	(00: memory clock = RCLK)
3 = CCLK_enable	(0: CCLK pin driver is tristated)
2:0 = OPMODE	(111: two-channel asynchronous FIFO)

Instruction Register 1 (dflt = 00000000)

7:0 = reserved	(0)

Instruction register 2 (dflt = 00_000_000)

7:6 = TRS_SYNC[1:0]	(00: ignore embedded TRS)
5 = B_FLD	(0: frame sync from TRS)
4 = A_FLD	(0: frame sync from TRS)
3 = MARK_SEL	(0: use marked address)
2:0 = FLAG_SET	(000: trigger empty, full on 1/34, 33/34)

Instruction register 3 (dflt = 00000000)

7 = BSET_catch	(0: ignore BSET & TRS to force read pointer)
6 = ASET_catch	(0: ignore ASET & TRS to force read pointer)
5 = RSET_b_sel	(0: falling edge one shot RSET_b)
4 = RCLR_b_sel	(0: falling edge one shot RCLR_b)
3 = BSET_b_sel	(0: falling edge one shot BSET_b)
2 = BCLR_b_sel	(0: falling edge one shot BCLR_b)
1 = ASET_b_sel	(0: falling edge one shot ASET_b)

Control Register Map

Instruction register 4 (dflt = 0000_0000)

7, 3 = reserved	(0, 0)
6:4 = BFLAG_CTL	(00: BPE, BPF are part-empty, -full)
2:0 = AFLAG_CTL	(00: APE, APF are part-empty, -full)

Instruction register 5 (dflt = 0000_0000)

7:4 = BASE_ADDR	(0000: lowest-address chip in a sequence)
3:0 = CASCADE	(0000: sequence comprises a single chip)

Instruction register 6 (dflt = 0000_0000)

7:6 = ALATENCY[25:24]	(00)
5:4 = BLATENCY[25:24]	(00)
3:0 =ROW_LENGTH[11:8]	(0000: 24-bit linear map; see reg 7)

Instruction register 7 (dflt = 00000000)

7:0 =ROW_LENGTH[7:0]	(00000000: 24-bit linear map; see reg 6)

Instruction register 8 (dflt = 00001000)

7:0 = ALATENCY[23:16]	(00000000: default = 0; see reg 9, a)

Instruction register 9 (dflt = 00000000)

7:0 = ALATENCY[15:8]	(00000000: default = 0; see reg 8, a)

Instruction register a (dflt = 00000000)

7:0 = ALATENCY[7:0]	(00000000: default = 0; see reg 8, 9)

Instruction register b (dflt = 00000000)

7:0 = BLATENCY[23:16]	(00000000)

Control Register Map

Instruction register c (dflt = 00000000)

7:0 = BLATENCY[15:8]	(00000000)

Instruction register d (dflt = 00000000)

7:0 = BLATENCY[7:0]	(00000000)

Instruction register e (dflt = 00000000)

7 = MEMORY_TEST	{0 - memory error correction enabled/normal}
6 = MEMORY_FAST	(0 - memory read error correction for write)

Instruction register f (dflt = 00000000)

4:0 = TSADRtest site address	

Instruction register 10 (0)

7:0 = TSBUS	

Detailed Signal Definitions

R0[7:6] WIDTH[1:0] - data word size at input/output ports

0x	8 bits	[11:4]	xOUT[3:0] tristated
10	10 bits	[11:2] (dflt)	xOUT[1:0] tristated
11	12 bits	[11:0]	

R0[5:4] MCLK_RATE[1:0] frequency ratio: memory clock / RCLK

00, 11	1 (dflt)	6MHz < RCLK < 50MHz
01	1/2	12MHz < RCLK < 100MHz
10	2	3MHz < RCLK < 27MHz (a)

(a) Random access modes (OPMODE = 1 or 2) require MCLK_RATE = 10.

Detailed Signal Definitions

RO[3] CCLK_enable makes memory core clock visible on CCLK test pin

0	disable (tristate) (dflt)
1	enable

RO[2:0] OPMODE[2:0] - operating mode

000	1 chnl	synchronous shift register (fix delay, 1 clock)
001	1 chnl	random access read
010	1 chnl	random access write
011	1 chnl	asynchronous (slave) FIFO
100	2 chnl	synchronous shift reg. (2 fix delays, 1 clock)
101	2 chnl	FIFO, B slaved to A
110	2 chnl	FIFO, A slaved to B
111	2 chnl	asynchronous (slave) FIFO (dflt)

R2[7:6] TRS_SYNC[1:0] - response to embedded TRS EAV (a)

00	disable TRS sync detection (dflt)
01	F-bit of embedded TRS EAV marks current write pointer.
10	F-bit of embedded TRS EAV sets current write pointer to value set by BOUT/BIN (1-chnl.modes) or ALAT & BLAT (2-chnl. modes, respectively).
11	F-bit of embedded TRS EAV clears current write pointer. (a) If B_FLD = 0 (frame-based sync), action is on each B-channel EAV with F = 0 for which the preceding EAV had F = 1. If B_FLD = 1 (field-based sync), action is on each B-chan EAV whose F differs from that of the preceding EAV. A_FLD affects the A-channel operation in the same fashion.

Detailed Signal Definitions

R2[5] B_FLD frame/field sync select, chnl B

0	use only falling F-bit in EAV; ignore rising (dflt)
1	use both rising and falling F-bit in EAV

R2[4] A_FLD frame/field sync select, chnl A same logic as B_FLD

R2[3] MARK_SEL: when RSET_b goes to 0:

0	force read pointer(s) to marked address(es) (dflt)
1	force read pointer(s) as shown:

OPMODE	BCLR_b	Read Pointer
0-3	1	remap address
0-3	0	BLAT
4-7	x	A=ALAT, B=BLAT

R2[2:0] FLAG_SET[2:0] - sets fractional "fullness" and "emptiness" thresholds in memory core. Full flag goes HIGH when and only when the memory is at least TH full. Empty flag goes HIGH when and only when the memory is less than TL full.

000	TH = 33/34	TL = 1/34 (dflt)
001	TH = 32/34	TL = 2/34
010	TH = 31/34	TL = 3/34
011	TH = 30/34	TL = 4/34
100	TH = 29/34	TL = 5/34
101	TH = 28/34	TL = 6/34
110	TH = 27/34	TL = 7/34
111	TH = 26/34	TL = 8/34

Detailed Signal Definitions

R3[7] BSET_catch (OPMODES 4-7 only)

0:	setting write pointer B does not mark its new value (dflt)
1:	setting write pointer B automatically marks its new value

R3[6] ASET_catch (all OPMODES) logic same as for BSET_catch

R3[5:0] Control action.

R3[5]	BSET_b_sel
R3[4]	BCLR_b_sel
R3[3]	ASET_b_sel
R3[2]	ACLR_b_sel
R3[1]	RSET_b_sel
R3[0]	RCLR_b_sel
0:	Each falling edge on the corresponding control pin overrides a memory address counter for exactly one clock cycle, after which normal memory address incrementing immediately resumes. (dflt)
1:	The corresponding pin continuously overrides the memory address counter as long as it is held LOW. Memory address incrementing resumes when the pin is returned HIGH.

R4[6:4] BFLAG_CTL[2:0] for pins BPE and BPF

BFLAG_CTL	BPE	BPF
000	chnl B empty	chnl B full (dflt)
001	read B = mark B	read A = mark A
010	AIN f	AIN v
011	AOUT f	AOUT
100	AIN f	AIN h
101	AOUT f	AOUT h
110	BIN f	BIN h
111	BOUT f	BOUT h

Detailed Signal Definitions

AIN f, v, h are the TRS bits embedded in the incoming A channel TRS signals. AOUT f, v, h are the TRS bits embedded in the emerging A channel TRS signals. BIN f, v, h and BOUT f, v, h are the analogous B channel values. Read A(B) is the read address pointer value for channel A(B).

R4[2:0] AFLAG_CTL[2:0] for pins APE and APF

AFLAG_CTL	APE	APF
000	chnl A empty	chnl A full (dflt)
001	read B = mark B	read A = mark A
010	BIN f	BIN v
011	BOUT f	BOUT v
100	BIN f	BIN h
101	BOUT f	BOUT h
110	AIN f	AIN h
111	AOUT f	AOUT h

R5[7:4] BASE_ADDR[3:0] position of chip in cascade series; 0000 = lowest; BASE_ADDR[3:0] must not exceed CASCADE[3:0]

R5[3:0] CASCADE[3:0] number of chips in a system with concatenated address spaces.

0000:	single chip operation; (dflt) sequential R, W memcore addresses modulo 103,680
0001: modulo 207,360	two chip cascade; sequential R, W addresses
	...
1111:	sixteen chip cascade; (a) sequential R, W addresses modulo 1,658,880 (a) Note limits, related to WIDTH control: 0- 9 always accepted (WIDTH = xx) 10-12 useful for 10 or 12 bit (WIDTH = 1x) 13-15 useful for 12 bits only (WIDTH = 11)

Detailed Signal Definitions

R6[3:0], R7[7:0] ROW_LENGTH[11:0] - for Cartesian-to-linear address map in 1-chnl modes

This control governs the remapping of Cartesian coordinates arriving on BIN (horizontal component) and BOUT (vertical component) into a linear address, for use by the chip's internal address generator. Setting ROW_LENGTH to 0 causes the incoming address to be interpreted directly as a linear address (or equivalently, a Cartesian address with 4096 pixels per line), with the 12 bits of BOUT concatenated with the 12 bits of BIN.

ALATENCY[25:0] Total wait latency, channel A

In single-channel synchronous shift register mode (OPMODE = 0), the 21 LSBs, ALATENCY[20:0], determine the effective shift register depth, i.e., such that the chip's input-to-out latency = TBD + ALATENCY clock cycles. In dual-channel modes with synchronous A channel (OPMODE = 4, 5), these bits set the A channel delay only. For OPMODE = 0, 4, or 5, a falling edge on pin AMARK_b marks the current write pointer and starts a countdown timer, which forces the read pointer to this marked position ALATENCY clock cycles later.

In addition to this function, in all OPMODES, bringing ASET_b low forces the A (OPMODE 4-7) or single overall (OPMODE 0-3) memory write pointer to:

ALATENCY[25:22]	chip address	1 out of CASCADE+1
ALATENCY[21:12]	core address	1 out of 544
ALATENCY[11:8]	bank number	1 out of 12
ALATENCY[7:5]	section number	1 out of 8
ALATENCY[4]	channel number	A side or B side; OPMODE 0-3
ALATENCY[3:0]	parse number	WIDTH selects among 10, 12, 15

Thus, when ALATENCY is used to establish a time delay, its 21 lowest bits are interpreted as an ordinary unsigned binary number. In contrast, when it is used to override an address pointer, its 26 bits are parsed into the six fields indicated above.

BLATENCY[25:0] - shift register depth, channel B (two-channel synchronous shift register modes 4 and 6, only). In these modes, this control impacts channel B exactly as ALATENCY did channel A in modes 4 and 5.

Total Channel B data latency = TBD + LATENCY_B clock cycles. This sets a binary wait count from BMARK_b falling edge.

Detailed Signal Definitions

In OPMODES 0-3, falling RSET_b forces the memory read pointer to:

BLATENCY[25:22]	chip address	1 out of CASCADE+1
BLATENCY[21:12]	core address	1 out of 544
BLATENCY[11:8]	bank number	1 out of 12
BLATENCY[7:5]	section number	1 out of 8
BLATENCY[4]	channel number	A side or B side; OPMODE 0-3
BLATENCY[3:0]	parse number	WIDTH selects among 10, 12, 15

In OPMODES 4-7, falling BSET_b forces the B memory write pointer to the values indicated in this table, except BLATENCY[4], which is ignored.

MEMORY_TEST - For factory test purposes only, turns off error correction.

0:	normal operation (dflt)
1:	memory error correction disabled

MEMORY_FAST - For factory test purposes only

0:	“before-and-after” error correction during write mode (dflt)
1:	“before” error correction disabled during write mode

TSADR[4:0]	**test site address (active only if MPU pointer = 10000)**
00	input FIFO read and write pointers [7:6] B write; [5:4] B read [3:2] A write; [1:0] A read
01	output FIFO read and write pointers same pattern as for input

FIFOs

02	input FIFO parse addresses [7:4] chan B; [3:0] chan A
03	output FIFO parse address [7:4] chan B; [3:0] chan A

Detailed Signal Definitions

FIFOs--Continued

04	FIFO read/write controls
	[7] in B write enable [6] in B read enable [5] in A write enable [4] in A read enable [3] out B write enable [2] out B read enable [1] out A write enable [0] out A read enable
05	front fifo full/empty flags [7] front FIFO B full [6] front FIFO B empty [5] front FIFO A full [4] front FIFO A empty
06	Memory A refresh addr[9:2]
07	{Memory A refresh addr[1:0], bank_adr[3:0], Memory A read/write control}
08	Memory B refresh addr[9:2]
09	{BMemory refresh addr[1:0], bank_adr[3:0], Memory B read/write control}
0a	Memory A read addr[9:2]
ob	Memory A read addr[1:0], Bank_adr[3:0]
oc	Memory B read addr[9:2]
od	Memory B read addr[1:0], Bank_adr[3:0]
oe	Memory A write addr[9:2] to FIFO
of	Memory A write addr[1:0], Bank_adr[3:0]
10	Memory B write addr[9:2] to FIFO
11	Memory B write addr[1:0], Bank_adr[3:0]

Detailed Signal Definitions

TSBUS[7:0] Test site bus, if this address is set, the mpu interface reads out the contents of the data bus selected by TSADR

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
VCC supply voltage with respect to ground	–0.5V to +4.5V
Input signal with respect to ground	–0.5V t o 5.5V
Signal applied to high impedance output	–0.5V to 5.5V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commerical	0°C to +70°C	–3.00V ≤ Vcc ≤ 3.60V

Electrical Characteristics *Over Operating Conditions (Note 4)*

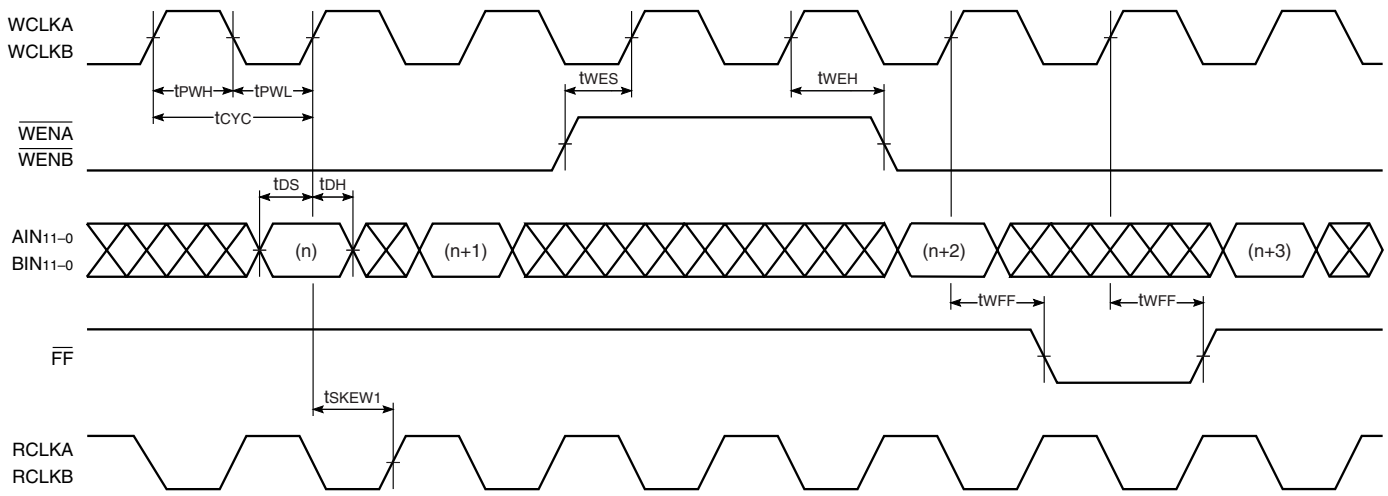
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		5.5	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{Ix}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Note 5,6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

Switching Characteristics

Commercial Operating Range (0°C to +70°C) Notes 9, 10 (ns)

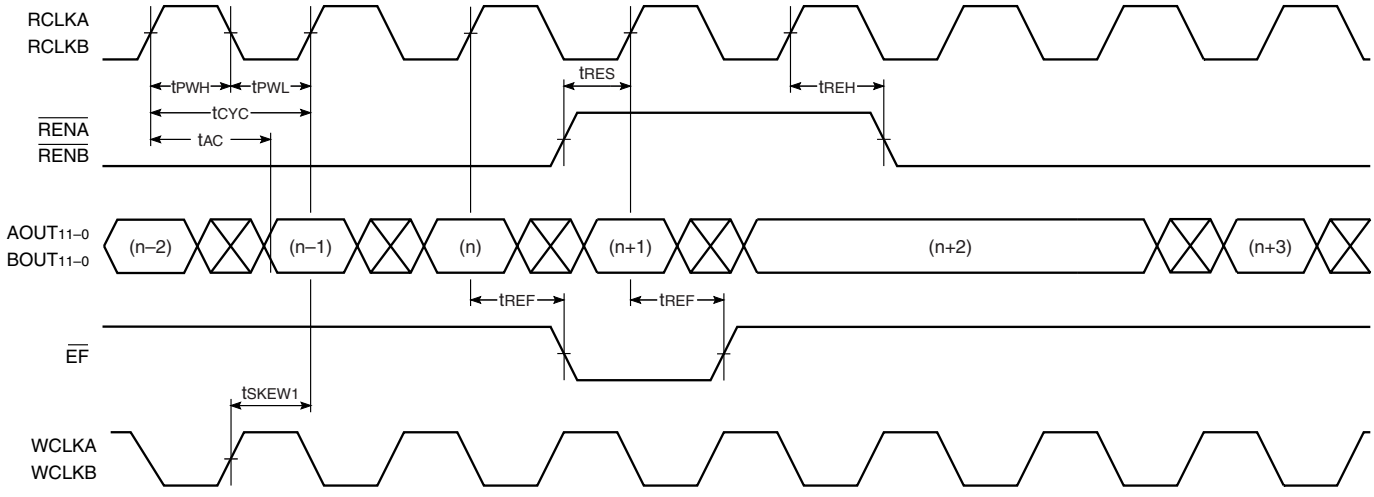
		LF3312QC10			
		10			
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	10			
t_{PWH}	Clock Pulse Width High	3			
t_{PWL}	Clock Pulse Width Low	3			
t_{DS}	Setup Time, All Inputs	4			
t_{DH}	Hold Time, All Inputs	0			
t_{WES}	Write Enable Setup Time	4			
t_{WEH}	Write Enable Hold Time	0			
t_{RES}	Read Enable Setup Time	4			
t_{REH}	Read Enable Hold Time	0			
t_{LDS}	Load Setup Time	4			
t_{LDH}	Load Hold Time	0			
t_{RS}	Read/Write Reset Setup Time	4			
t_{RH}	Read/Write Reset Hold Time	0			
t_{AC}	Access Time		6		
t_{WFF}	Write Clock to Full Flag		6		
t_{REF}	Read Clock to Empty Flag		6		
t_{PAF}	Write Clock to Programmable Almost-Full Flag		6		
t_{PAE}	Read Clock to Programmable Almost-Empty Flag		6		
t_{OHZ}	Output Enable to Output in Low Impedance		6		
t_{OLZ}	Output Enable to Output in High Impedance		6		
t_{SKEW1}	Skew Time Between Read and Write Clocks for $\overline{EF}$ and $\overline{FF}$		4		
t_{SKEW2}	Skew Time Between Read and Write Clocks for $\overline{PAEx}$ and $\overline{PAFx}$		4		

Write Cycle Timing



RWA = RWB = HIGH

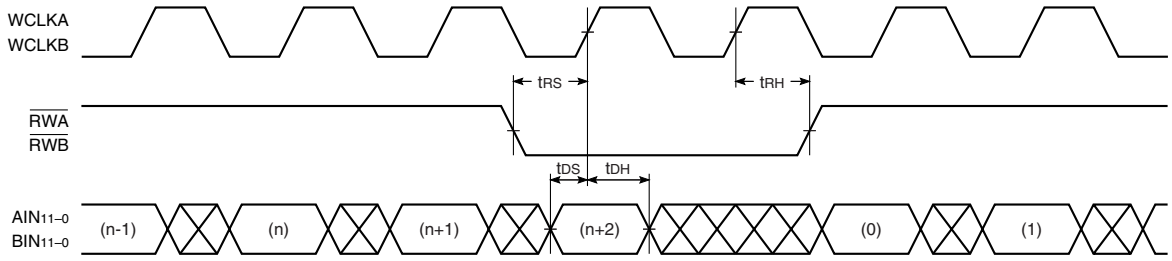
Read Cycle Timing



RRA = RRB = HIGH

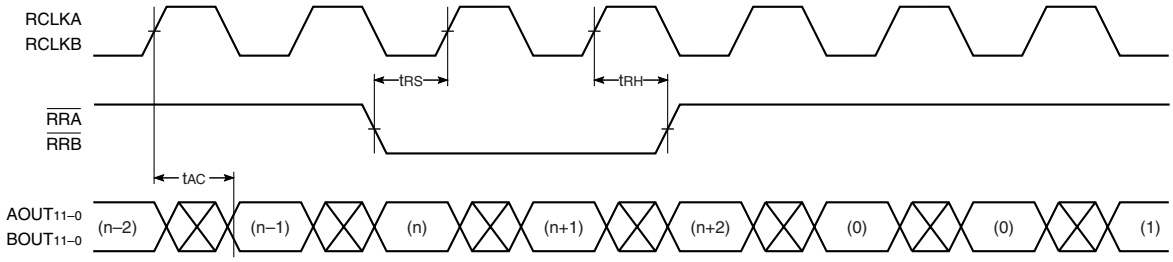
OEA = OEB = LOW

Write Reset Timing



$\overline{WENA}$ = $\overline{WENB}$ = LOW

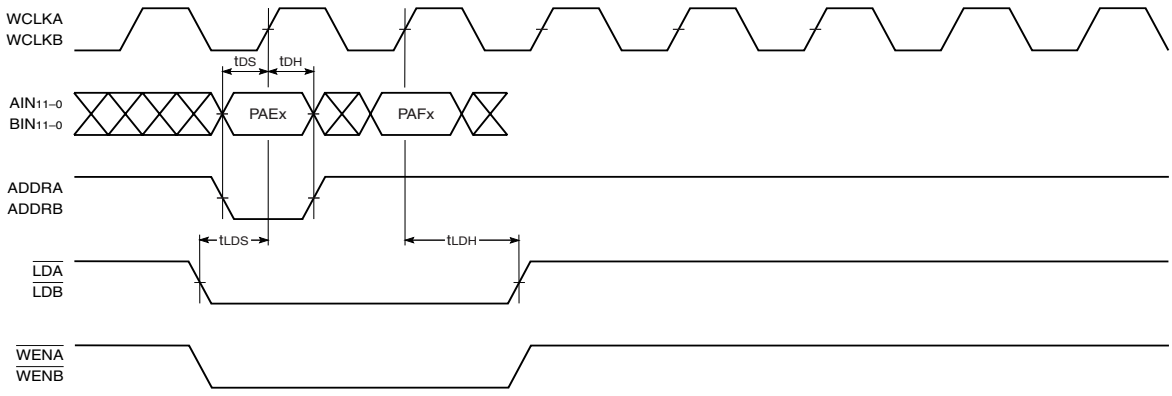
Read Reset Timing



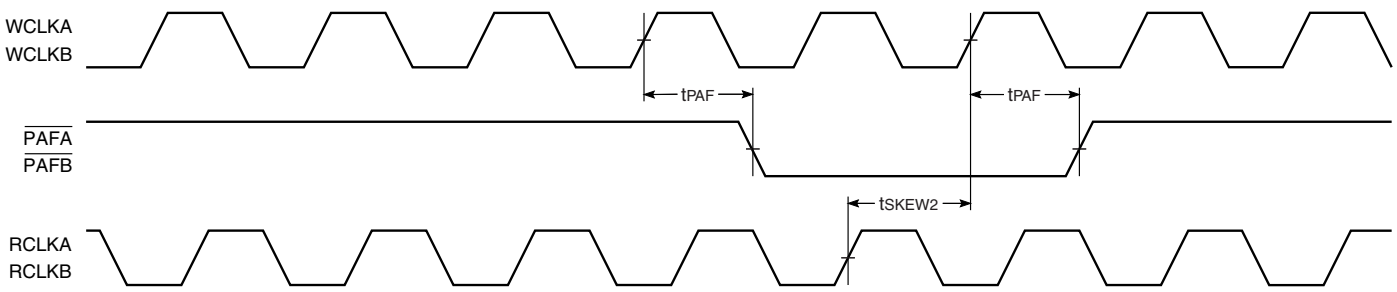
$\overline{RENA}$ = $\overline{RENB}$ = LOW

$\overline{OEA}$ = $\overline{OEB}$ = LOW

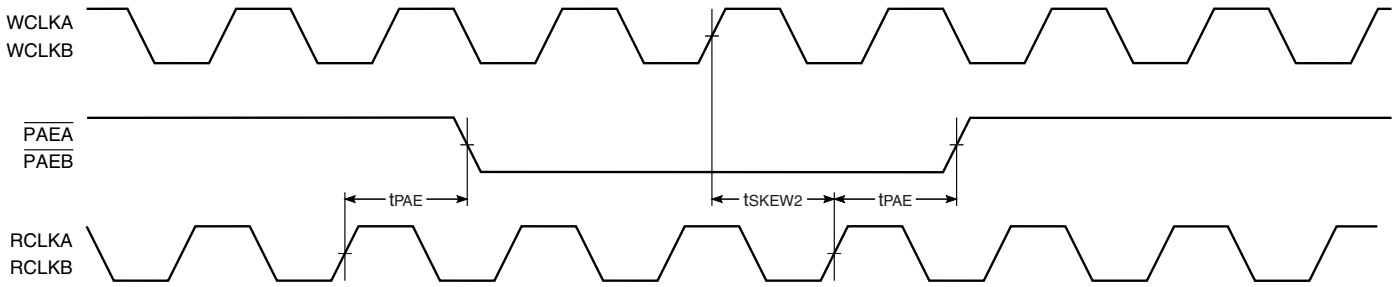
Programmable Flag Load Timing



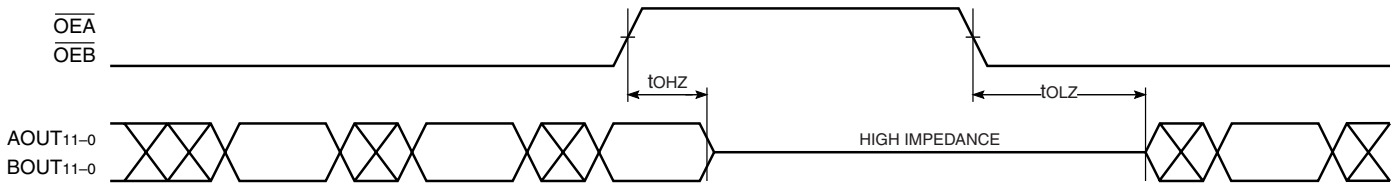
Programmable Almost Full Flag



Programmable Almost Empty Flag



Output Enable and Disable



Notes

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides h clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6V. The device can withstand operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels may be in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be approximated by:

where $\frac{NCV^2F}{2}$

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 50 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, and no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{dis} test), and input levels of nominally 0 to 3.0V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current change pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the device as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the device reads.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required input levels relative to the device ground pin.

Notes

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ena} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{dis} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{th}, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Figure A. Output Loading Circuit

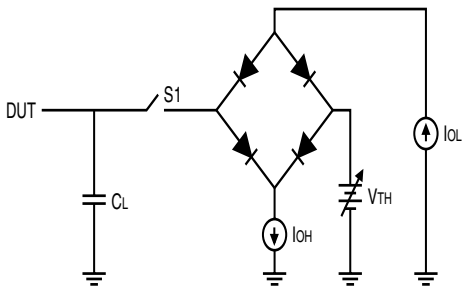
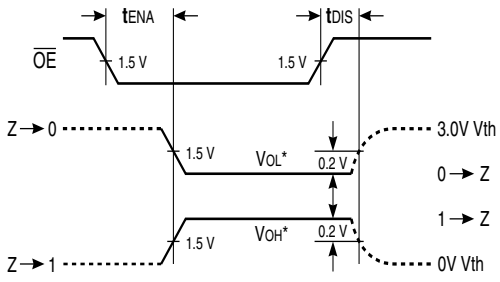


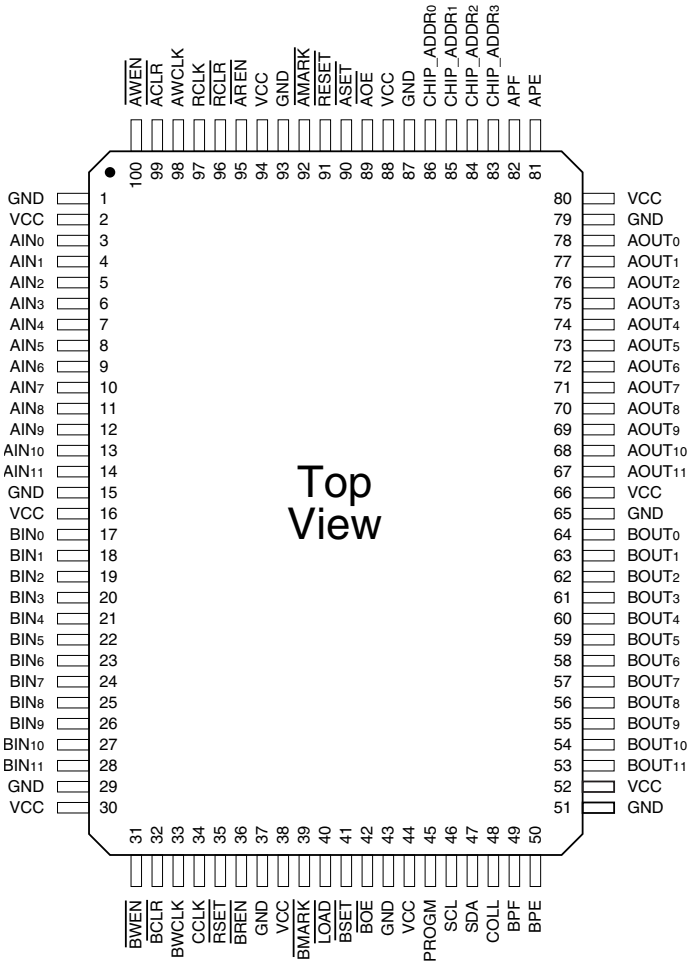
Figure B. Threshold Levels



VOL* Measured VOL with IOH = –10mA and IOL = 10mA
VOH* Measured VOH with IOH = –10mA and IOL = 10mA

Package and Ordering Information

100-Pin
PQFP



Speed	**Plastic Quad Flatpack (Q2)**
	0°C to 70°C--Commercial Screening
10 ns	LF3312QC10