PC Card/Compact Flash Interface to StrongARM SA-1100 and SA-1110 CPUs

FEATURES

- Single Slot PC Card/Compact Flash interface (software configurable)
- Glue-less interface to SA-1100 / 1110
- Support of both 3V and 5V cards
- Single PC Card interface
  - ⇒ Allows hot insertion
  - ⇒ Reduces power dissipation
  - ⇒ Reduces board real estate
- Control for external Power Switch for 3V, 5V and Vpp
- Supports second PC Card/Compact Flash slot by using another L1110 chip
- Level shifting buffers on chip to support dual power supply
- Ultra low power CMOS design
- 144 pin TQFP package

OVERVIEW

The L1110 is designed to provide a glue-less interface between Intel's StrongARM™ SA-1100 and SA-1110 integrated processors and a PC Card or Compact Flash socket. The L1110 does the 3V to 5V and 5V to 3V conversion resulting in a clean interface between the processor and the PC Card socket. This results in a much smaller board area requirement and lower power. In addition, the L1110 allows hot insertion of a PC Card and provides control signals to drive Maxim/Temic/T.I. power switches to switch the 3V, 5V and Vpp power to the socket. Two L1110 devices may reside in a system for the support of two PC Cards or Compact Flash cards. The L1110 is fabricated in a 0.6-micron CMOS technology.

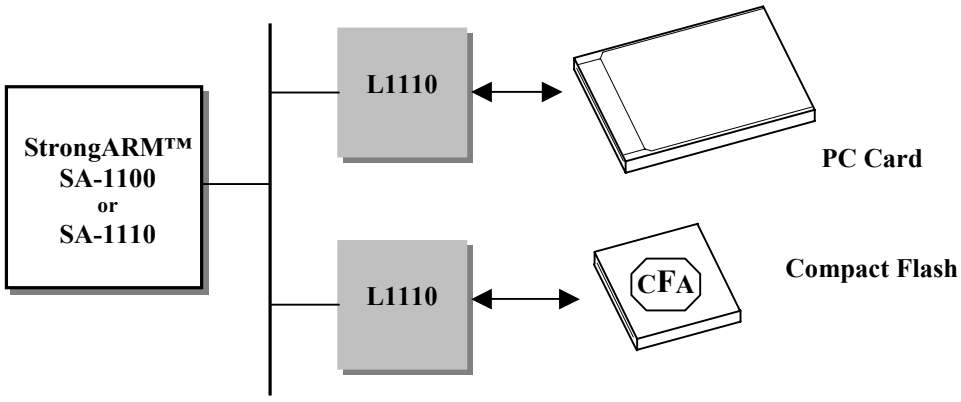
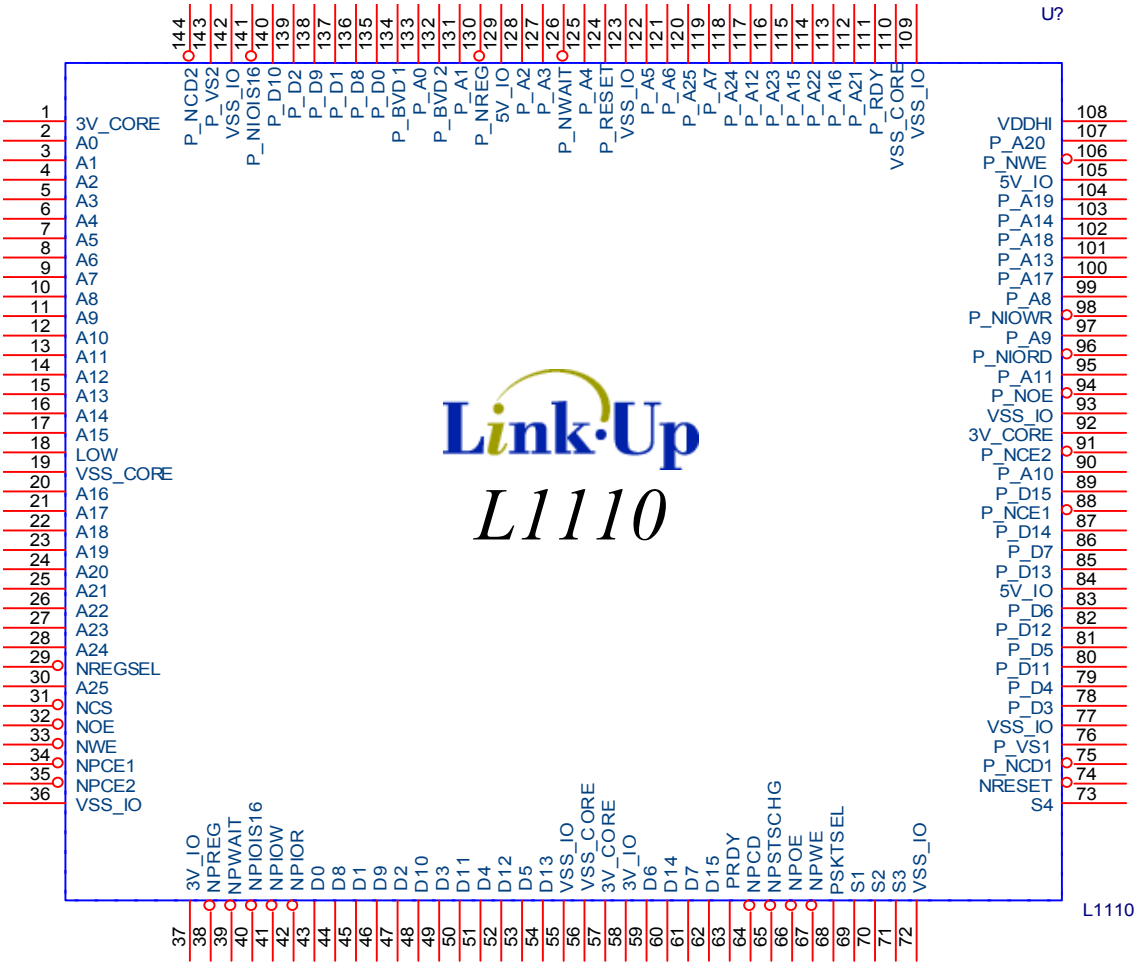


Figure 1. Typical Application

Pin Information

Figure 2. Pin Diagram

The pin assignment is optimized for interfacing to a SA-1100 or SA-1110 and PC Card socket. No vias are required on any of the socket signals. Routing can be done on two layers with power and ground on separate planes.



Pin Description

Table 1. Pin Description

Pin Name	Description
CPU Interface Pins. All signals are CMOS level.	
A[25:0]	**CPU Address Inputs:** This bus connects to the SA-1100 / 1110 address bus.
D[15:0]	**CPU Bi-directional Data Bus:** This bus is driven by the L1110 when PSKTSEL, nPCE[2:1], nPIOR and nPOE are asserted. For the on chip PC Card register access nCS, nREGSEL and nOE have to be active.
nCS	**Chip Select:** This signal is used with nOE, nREGSEL and nWE to read and write the on chip PC Card register.
nREGSEL	**Register Select:** This signal is used to access the on chip PC Card register. It has to be tied low in a one slot system and tied to an address pin (A24/A25) in a two slot system.
nOE	**Output Enable:** Input from CPU Output Enable signal. This signal is used with nCS and nREGSEL to read the on chip PC Card register.
nWE	**Write Enable:** This signal is used with nCS and nREGSEL to write to the on chip PC Card register.
LOW	Spare pin should be tied to Vss.
System Reset	
nRESET	**Reset Input**: Input from system reset. All output signals on the PC Card bus are tri-stated when nRESET is asserted. The PR Command register will be reset if nRESET is asserted thus, S[4:1] outputs are low.
PC Card Signals: For a detailed description on the following signals see SA-1100 / 1110 data sheet. All signals are CMOS level.	
nPCE[2:1]	**Card Enable:** Input from CPU nPCE[2:1] signals.
nPIOIS16	**IO is 16 bit:** Output to CPU nPIOIS16 signal. Open Drain output. This signal has to be wired OR with the equivalent output from the second slot controller. It must be pulled up with a resistor.
nPIOR	**IO Read:** Input from CPU nPIOR signal.
nPIOW	**IO Write:** Input from CPU nPIOW signal.
nPOE	**Output Enable:** Input from CPU nPOE signal.
nPREG	**REG Select:** Input from CPU nPREG signal.
nPWAIT	**Wait:** Output to CPU nPWAIT signal. Open Drain output. This signal has to be wired OR with the equivalent output from a second L1110. It must be pulled up with a resistor.
PRDY	**Ready:** This is the RDY/nIRQ signal of the PC Card bus. Open Drain output. Connect to the equivalent signal of the second L1110. It must be pulled up with a resistor.This signal may be used to generate an interrupt to the CPU.
nPWE	**Write Enable:** Input from CPU nPWE signal.
nPSTSCHG	**Status Change:** Output to CPU GPIO signal. Open Drain output. Connect to the equivalent signal of the second L1110. This signal is derived from the P_BVD[1] signal of the PC Card socket signal. It may be used to generate an interrupt to the system. It must be pulled up with a resistor.
nPCD	**Card Detect:** Output to CPU GPIO signal. Open Drain output. Connect to the equivalent signal of the second L1110. This output is driven low when both P_nCD[2] and P_nCD[1] are low otherwise it is high. It indicates that a card is inserted. The status of these pins can also be read in the PR Status Register.
PSKTSEL	**Socket Select:** This pin when active will enable the L1110 and allow access to the PC Card. PSKSEL polarity is programmed by the state of bit 8 in the PR Command register. It is active low if bit 8 is reset (for slot 0) and it is high active when this bit

	is set 1. The PC Card register is accessible irrespective of the state of this pin.
PC Card Socket Signals: All signals are CMOS level.	
P_RESET	**Reset:** This signal can be asserted by writing a '1' to bit 4 of the PC Card Command register. A pull-up resistor is required to assure that the card is reset while nRESET is active.
P_A[25:0]	**Address Bus:** PC Card address bus. The bus will be tri-stated when one of the P_nCD[2:1] signals is high or if PRC[7] is '0'. If Compact Flash bit PR[6] is set A[25:11] are always high.
P_D[15:0]	**Data Bus:** PC Card bi-directional data bus. Data is transferred from the PC Card socket to the CPU through this 16-bit bus. Only byte and 16 bit operations are supported. This bus will be driven by the L1110 only when: nCE1,2 is asserted and nPIOR and nPOE is not asserted. PSKTSEL is active low for slot 0 and active high for slot 1 access and PC Card register bit 7 is set to '1' and P_nCD[2:1] are both low. In all other cases this bus is tri-state. The inputs are protected from drwaing current in case no card is attached.
P_nREG	**nREG:** Output to PC Card socket nREG signal. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low.
P_nCE[2:1]	**Card Enable:** Output to PC Card socket nCE[2:1] signals. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low.
P_nOE	**Output Enable:** Output to PC Card socket nOE signal. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low. This signal is high when PSKTSEL is inactive.
P_nWE	**Write Enable:** Output to PC Card socket nWE signal. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low. This signal is high when PSKTSEL is inactive.
P_nIOR	**IO Read:** Output to PC Card socket nIOR signal. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low. This signal is high when PSKTSEL is inactive.
P_nIOW	**IO Write:** Output to PC Card socket nPIOW signal. This output is tri-stated if one of the P_nCD[2:1] signals is high or PRC[7] is low. This signal is high when PSKTSEL is inactive.
P_nWAIT	**Wait Signal:** Input from PC Card Socket nWAIT. A weak pull-up resistor to 5V_IO is on-chip.
P_nIOIS16	**IO is 16 bit:** Input from PC Card Socket nIOIS16. A weak pull-up resistor to 5V_IO is on-chip.
P_RDY	**Ready/Interrupt Request:** Input from PC Card Socket RDY/nIRQ signal. A weak pull-up resistor to 5V_IO is on-chip.
P_BVD[2:1]	**Battery Voltage Detect:** Input from PC Card Socket Battery Voltage Detect signals BVD[2:1]. A weak pull-up resistor to 5V_IO is on-chip.
P_VS[2:1]	**Voltage Sense:** Input from PC Card Socket Voltage Sense signals VS[2:1]. A weak pull-up resistor to 3V_IO is on-chip.
P_nCD[2:1]	**Card Detect:** Input from PC Card Socket Card Detect signals nCD[2:1]. If one of the P_nCD[2:1] signals is deasserted all PC Card outputs are tri-stated. A weak pull-up to 3V_IO is on-chip.
S[4:1]	**Power Control Signals:** Output control signals to the power switch (e.g. Temic Si9712). S[4:1] are low when nRESET is asserted. These signals are unaffected by the state of P_RESET. They reflect the state of bits PR[3:0] of the PC Card register. These outputs are CMOS level. If automatic power off is programmed and either P_nCD1 or P_nCD2 is inactive, S4:1 will be set to '0'.

Power Supply	
3V_CORE	VDD for Core Power.
3V_IO	VDD for IO Power.
5V_IO	PC Card Power. May be 0, 3.3V or 5V and is connected to the PC Cards power.
VDDHI	This pin has to be at the highest voltage of 3V or 5V.
VSS_CORE	VSS Core Power.
VSS_IO	VSS IO Power.

Figure 3. Block Diagram using one L1110 in a SA-1100 / 1110 system.

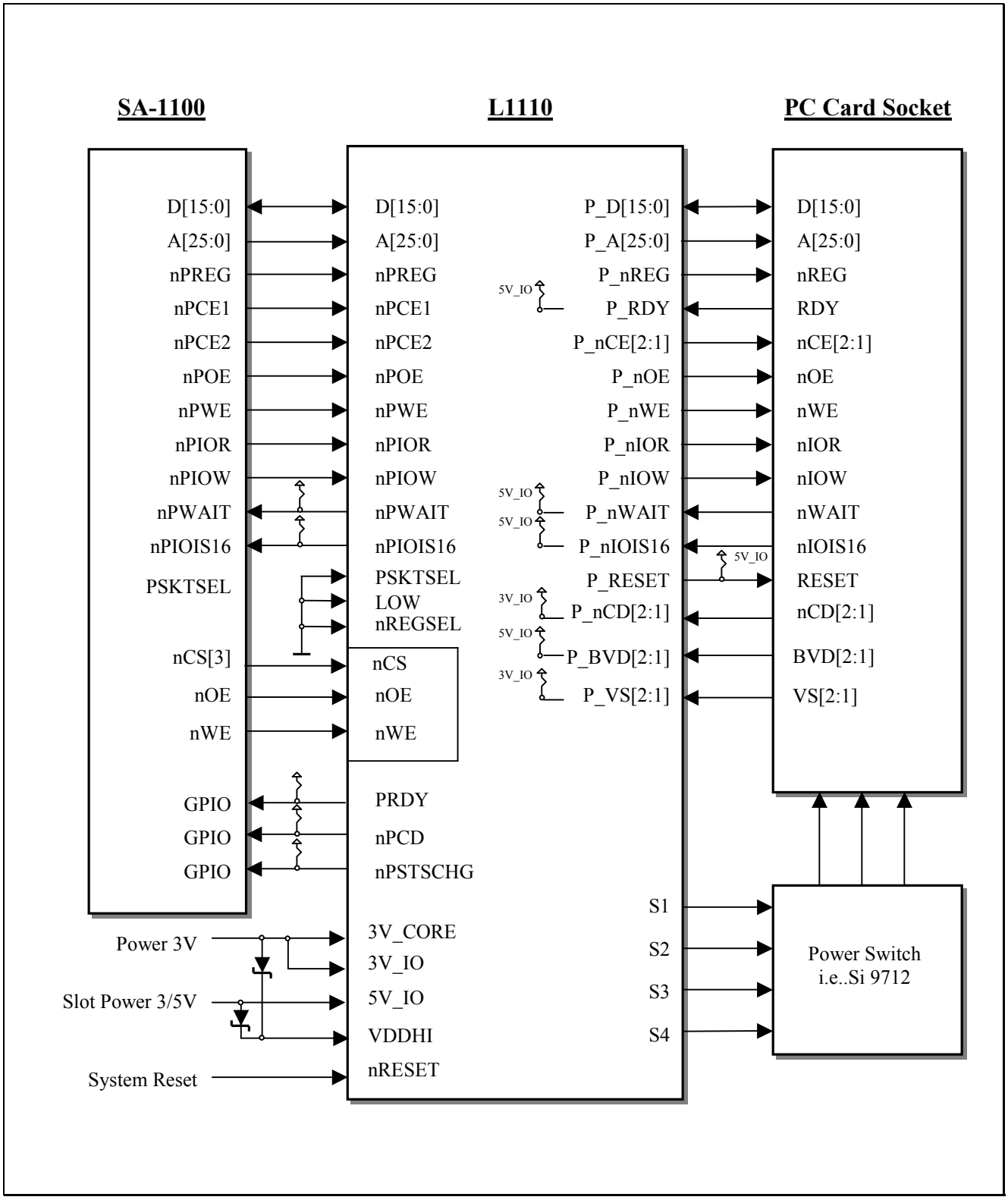
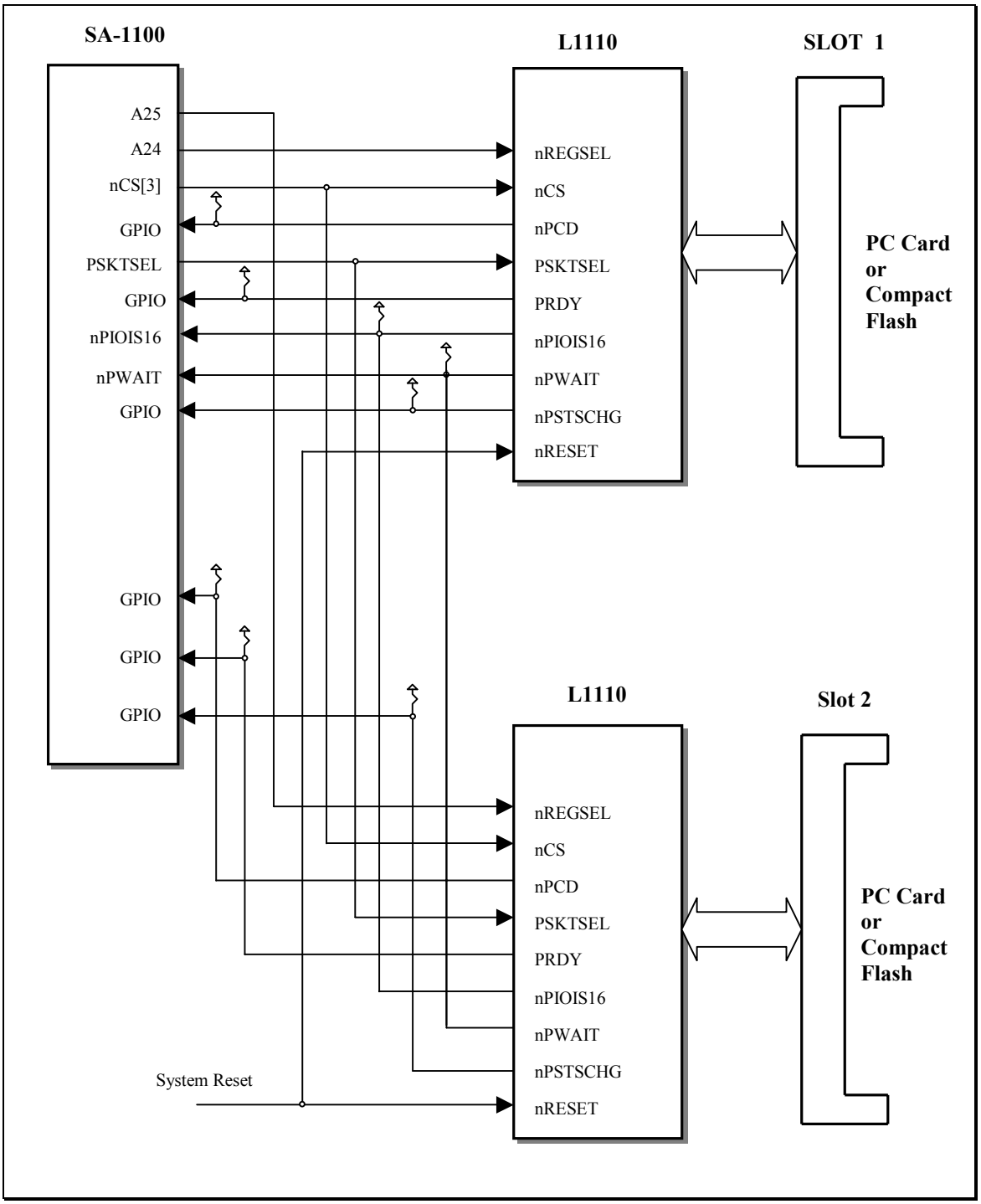


Figure 4. Block Diagram using two L1110 in a SA-1100 system.
Note: All signals not shown are identical to the one slot diagram in Figure 3.



Functional Description

PC Card Register (PR)

The PC Card register is composed of two 16-bit registers. The PR Status (PRS) and the PR Command (PRC). These registers can be read when nREGSEL, nCS and nOE signals are active. They can be written to by asserting nREGSEL, nCS and nWE.

PR Status (PRS)

Bit	Function	Description
3:0	S4:S1	These 4 bits reflect the current status of the Voltage Control Pins S4 down to S1.
4	BVD1	Battery Voltage Detect 1 status. This bit reflects the status of P_BVD[1] pin.
5	BVD2	Battery Voltage Detect 2 status. This bit reflects the status of P_BVD[2] pin.
6	VS1	Voltage Sense 1 status. This bit reflects the status of P_VS[1] pin.
7	VS2	Voltage Sense 2 status. This bit reflects the status of P_VS[2] pin.
8	RDY	P_RDY status. This bit reflects the status of P_RDY pin.
9	CD1	Card Detect 1: P_nCD[1] status. This bit reflects the status of P_nCD[1] pin.
10	CD2	Card Detect 2: P_nCD[2] status. This bit reflects the status of P_nCD[2] pin.
11	Reserved	
15:12	ID	Chip ID: This ID is for LinkUp Systems Corporation internal use only.

PR Command (PRC)

The command register is a 16 bit register. This register is cleared after power up or when nRESET is active.

Bit	Function	Description
0	S1	Voltage Control 1
1	S2	Voltage Control 2
2	S3	Voltage Control 3
3	S4	Voltage Control 4
4	RESET	Software Reset, this bit drives the P_RESET output. If set to high the P_RESET output is high.
5	APOE	Automatic power off enable: When this bit is set, S[4:1] will be cleared when P_nCD1 or P_nCD2 is high effectively turning off the power to the slot. S[4:1] will not regain the state if P_nCD1 and P_nCD2 should become active but have to be set under software control.
6	CFE	Compact Flash enable: If this bit is set the device is in Compact Flash mode. Addressing is limited to the space A[10:0] as defined by Compact Flash standard. A[25:11] are driven high.
7	SOE	PC Card socket signal output driver enable. The socket signals cannot be driven active unless this bit is set.
8	SSP	Socket Select Polarity: This bit has to be programmed in a two-slot system. If this bit is ‘0’ the device will respond when PSKTSEL is ‘0’. If this bit is ‘1’ the device will respond when PSKTSEL is ‘1’.
15	TST	Test bit: This bit should be set to 0 at all times.

ABSOLUTE MAXIMUM RATINGS

Absolute Temperature under Bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (10 seconds)	+275°C
Supply voltage to Ground	-0.5V to +7.0V
DC Input Voltage	- 0.5 to 5.5V Max
DC Output Current	± 10mA
DC Input Current	–10mA to 10mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)	0°C to +70°C
Supply Voltage (V_{CC})	3.3V ± 10%
Maximum input voltage (Vin)	5.25V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

Conditions: $V_{3VCore,}$ V_{3VIO} = 3.3V ± 10%; $V_{5VIO=}$ 5V± 5%; V_{SS} = 0V; Ambient Temperature T_A = 0°C to 70°C.

Table 2. DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
Vihc	Input high voltage CMOS	0.7 x Vcc	Vcc + 0.3V	V	
Vilc	Input low voltage CMOS	-0.3V	0.2 x Vcc	V	
Vohc	Output high voltage CMOS	Vcc – 1.0		V	Ioh = -1mA
Volc	Output low voltage CMOS		0.4	V	Iol = 2mA
Viht	Input high voltage TTL	2.0	Vcc + 0.3V	V	
Vilt	Input low voltage TTL		0.8	V	
Voht	Output high voltage TTL	2.4		V	Ioh = -2mA
Volt	Output low voltage TTL		0.4	V	Iol = 2mA
Iin	Input Leakage Current	-10	+10	uA	Vin = Vcc or Vss
Ioh	Output High Current	-2		mA	Respective Slot Vcc = 3.0V
Ioz	Output Tristate Leakage Current	-10	+10	uA	Vout = Vcc or Vss
Cin	Input Capacitance		10	pF	
Cout	Output Capacitance		10	pF	
I_{3Vcore} + I_{3VIO}	Operating Current		5	mA	No loads
I_{5VIO}	Operating Current		5	mA	No loads
I_{VDDHI}	Operating Current		2	mA	No loads
I_{PU}	Pullup Current		50	µA	5V_IO=5.25V
Icc stby	Standby Current		10	µA	on any supply total

AC Characteristics

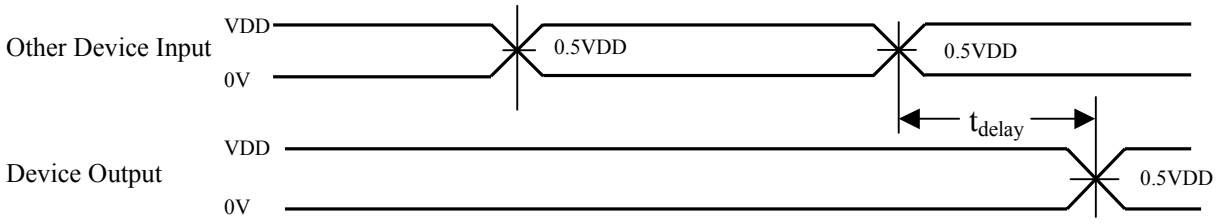
Operating Conditions: $V_{3VCore,}$ V_{3VIO} = 3.3V ± 10%; $V_{5VIO=}$ 5V± 5%; T_A= 0°C to 70°C.

Table 3. AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
t_{prop}	Prop Delay		18	ns	Any input to output, 5V_IO=3.0V
t_{rise}	Rise Time		20	ns	Any socket signal at 50pF load
t_{fall}	Fall Time		15	ns	Any socket signal at 50pF load
t_{setup}	Data Setup time to nWE high	10		ns	PR register write
t_{hold}	Data Hold time from nWE high	2		ns	PR register write
t_{Enable}	Output enable		15		Any socket output active from enable

Switching Test Waveform

All timings are measured at 0.5VDD (VDD may be 5V_IO, 3V-Core or 3V_IO). For additional capacitive loading add 0.2ns for every pF.



Pin Characteristics

This section describes each of the L1110 pins and its use. The table is in addition to the Pin Description with an emphasis on the electrical characteristics. Following symbols are used:

Type

n	Active low signal
I/O	bi-directional
I/OZC	I/O with output tri-stateable, CMOS
I/OZT	I/O with output tri-stateable, TTL
IC	Input CMOS
IS	Input with Schmitt Trigger
IT	Input TTL
OD	Open Drain Output
OC	Output CMOS
OZT	Output tri-stateable, TTL
PU	Pull up resistor on chip

5V Tolerance

All PC Card inputs are 5V tolerant. These inputs will tolerate 5V input levels provided L1110 5V_IO voltage on these pins is 5V. The current flow to the power plane under this condition is very low. VDDHI must be at the highest voltage of either 3V or 5V. Use two Schottky diodes as shown in the schematics.

Power Planes

The L1110 device has three power planes as defined below:

S	3.3V supply; same as the CPU input output plane	3V_IO
P	PC Card slot power, either 3.3V or 5V or off	5V_IO
C	Core Voltage, this plane drives the on chip logic	3V_CORE

Table 4. Pin Function

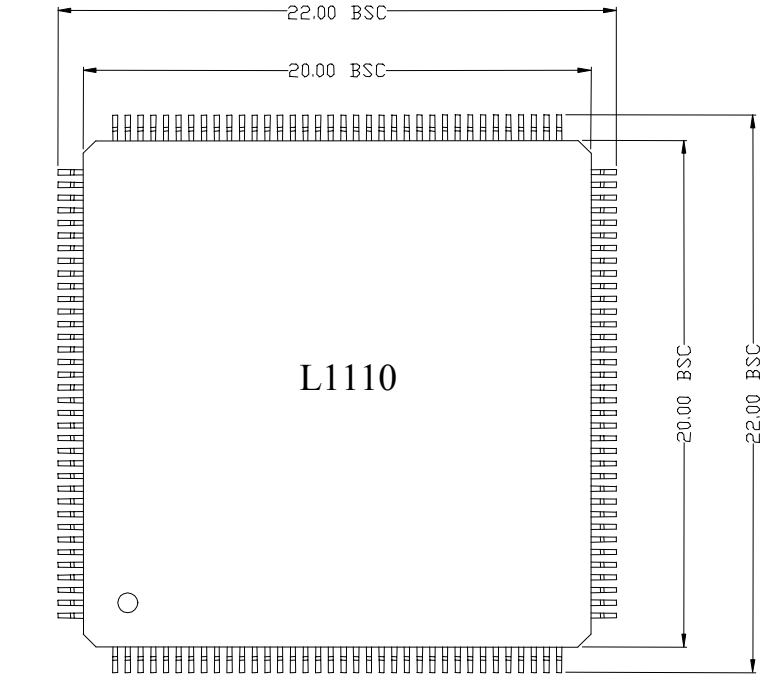
Signal Name	Pin Type	5V Tolerance	Power Plane	Drive [mA]	PU Ext.	Description
CPU Interface						
D[15:0]	I/OZC	No	S	2		Memory Data Bus
A[25:0]	IC	No	S			Memory Address Bus
nRESET	IC	No	S			Hardware Reset
nOE	IC	No	S			
nWE	IC	No	S			
nCS	IC	No	S			
nREGSEL	IC	No	S			Register Select
nPIOR	IC	No	S			See SA-1100 / 1110 data book
nPIOW	IC	No	S			for signal description
nPCE[2:1]	IC	No	S			
nPIOIS16	OD	No	S	2	s	
nPOE	IC	No	S			
nPREG	IC	No	S			
nPWAIT	OD	No	S	2	s	
nPWE	IC	No	S			
nPSTSCHG	OD	No	S	2	s	To GPIO/Interrupt
nPCD	OD	No	S	2		To GPIO
PRDY	OD	No	S	2	s	To GPIO/Interrupt
PSKTSEL	IC	No	S			
P_D[15:0]	I/OZT	Yes	P	2		Data Bus
P_A[25:0]	OZT	Yes	P	2		Address Bus
P_nCD[2:1]	ICPU	Yes	S			
P_nCE[2:1]	OZT	Yes	P	2		
P_nIOIS16	ITPU	Yes	P			
P_nIOR	OZT	Yes	P	2		
P_nIOW	OZT	Yes	P	2		
P_nOE	OZT	Yes	P	2		
P_nREG	OZT	Yes	P	2		
P_nWE	OZT	Yes	P	2		
P_nWAIT	ITPU	Yes	P			
P_RESET	OZT	Yes	P	2	p	
P_BVD[2:1]	ITPU	Yes	P			
P_RDY	ITPU	Yes	P			
P_VS[2:1]	ICPU	Yes	S			
S[4:1]	OC	No	S	4		

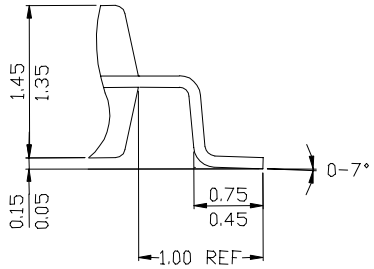
Power Supply							
3V_CORE		1,57,92					
3V_IO		37,58					
5V_IO		84,105,129					
VDDHI		108					
VSS_CORE		19,56,110					
VSS_IO		36,55,72,77,93, 109,123,142					

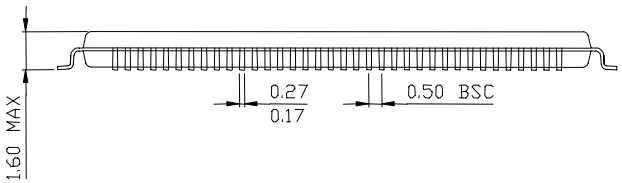
Pin Number Table:

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1.	3V_CORE	37.	3V_IO	73	S4	109	VSS_IO
2.	A0	38.	nPREG	74	nRESET	110	VSS_CORE
3.	A1	39	nPWAIT	75	P_nCD1	111	P_RDY
4.	A2	40	nPIOIS16	76	P_VS1	112	P_A21
5.	A3	41	nPIOW	77	VSS_IO	113	P_A16
6.	A4	42	nPIOR	78	P_D3	114	P_A22
7.	A5	43	D0	79	P_D4	115	P_A15
8.	A6	44	D8	80	P_D11	116	P_A23
9.	A7	45	D1	81	P_D5	117	P_A12
10.	A8	46	D9	82	P_D12	118	P_A24
11.	A9	47	D2	83	P_D6	119	P_A7
12.	A10	48	D10	84	5V_IO	120	P_A25
13.	A11	49	D3	85	P_D13	121	P_A6
14.	A12	50	D11	86	P_D7	122	P_A5
15.	A13	51	D4	87	P_D14	123	VSS_IO
16.	A14	52	D12	88	P_nCE1	124	P_RESET
17.	A15	53	D5	89	P_D15	125	P_A4
18.	LOW	54	D13	90	P_A10	126	P_nWAIT
19.	VSS_CORE	55	VSS_IO	91	P_nCE2	127	P_A3
20.	A16	56	VSS_CORE	92	3V_CORE	128	P_A2
21.	A17	57	3V_CORE	93	VSS_IO	129	5V_IO
22.	A18	58	3V_IO	94	P_nOE	130	P_nREG
23.	A19	59	D6	95	P_A11	131	P_A1
24.	A20	60	D14	96	P_nIORD	132	P_BVD2
25.	A21	61	D7	97	P_A9	133	P_A0
26.	A22	62	D15	98	P_nIOWR	134	P_BVD1
27.	A23	63	PRDY	99	P_A8	135	P_D0
28.	A24	64	nPCD	100	P_A17	136	P_D8
29.	nREGSEL	65	nPSTSCHG	101	P_A13	137	P_D1
30.	A25	66	nPOE	102	P_A18	138	P_D9
31.	nCS	67	nPWE	103	P_A14	139	P_D2
32.	nOE	68	PSKTSEL	104	P_A19	140	P_D10
33.	nWE	69	S1	105	5V_IO	141	P_nIOIS16
34.	nPCE1	70	S2	106	P_nWE	142	VSS_IO
35.	nPCE2	71	S3	107	P_A20	143	P_VS2
36.	VSS_IO	72	VSS_IO	108	VDDHI	144	P_nCD2

Package Diagram: LQFP-144. All dimensions are in mm.

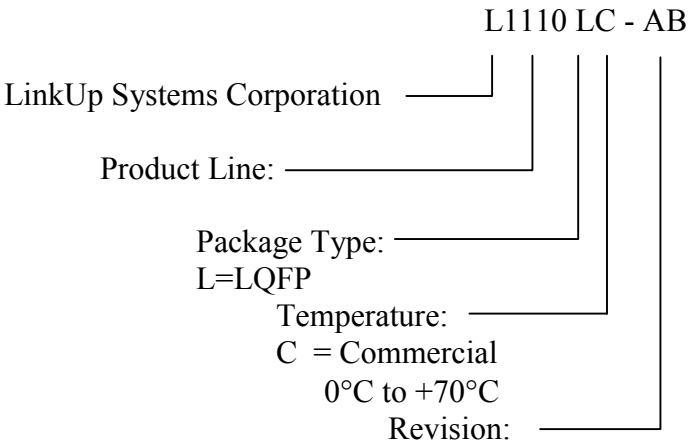






Ordering Information

The order number for the L1110 is:



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