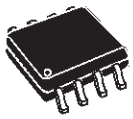
L6380
L6381

HIGH VOLTAGE HIGH-SIDE DRIVER

- $V_{H.V.}$ UP TO 600 V
- SUPPLY VOLTAGE UP TO 17 V
- DRIVER CURRENT CAPABILITY:
  SINK CURRENT = 200 mA
  SOURCE CURRENT = 100 mA
- UNDER VOLTAGE LOCKOUT WITH HYSTERESIS
- CMOS/LSTTL COMPATIBLE INVERTING INPUT
- dV/dt IMMUNITY ± 50 V/nS IN FULL TEMPERATURE RANGE
- CURRENT MODE CONTROL REFERENCE INPUT
- CURRENT/VOLTAGE MODE OPERATION (L6380)
- VOLTAGE MODE OPERATION (L6381)
- 8 PINS PACKAGE



MINIDIP **SO8**

ORDERING NUMBERS:

L6380 (MINIDIP) L6380D (SO)	L6381 (MINIDIP) L6381D (SO)

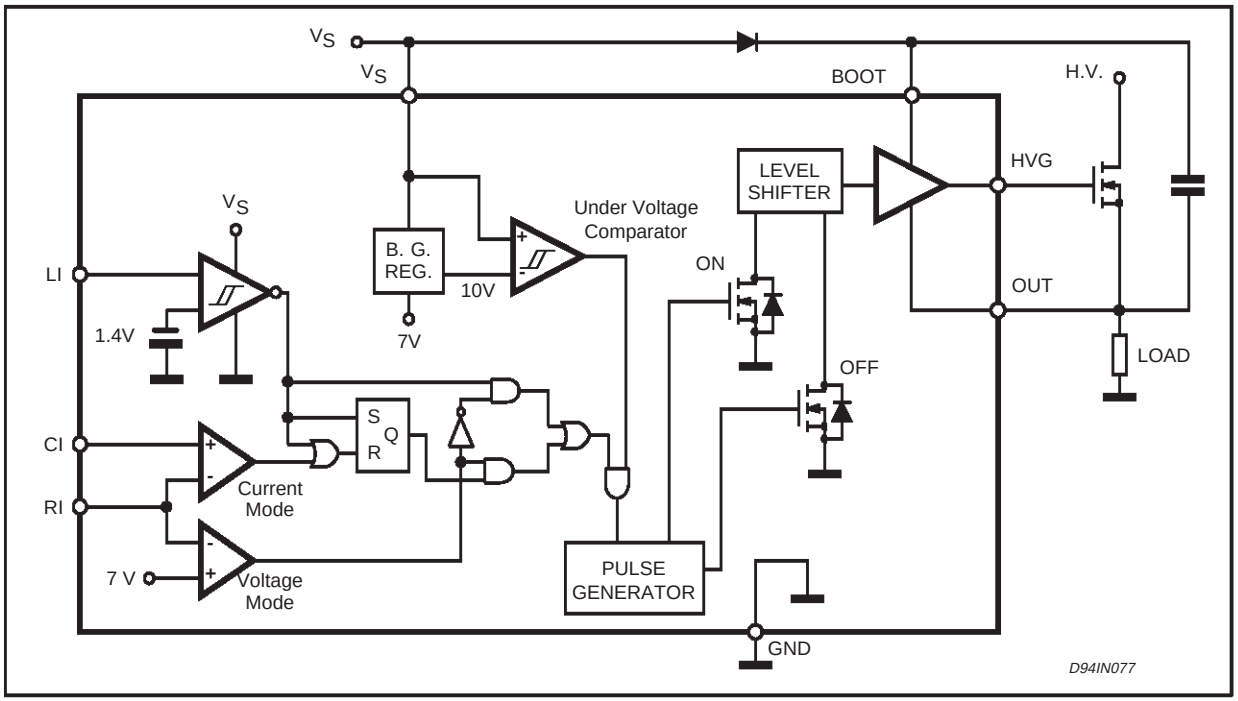
DESCRIPTION

The L6380/L6381 is a high-voltage device with a driving stage floating up to 600V.

It can be used to drive N-channel power MOSFET and IGBT, in high-side and low-side configurations.

The device has a logic input (CMOS and LSTTL compatible) and two comparator inputs compatible to ground.

L6380 BLOCK DIAGRAM



To drive the external power device the signal coming from input logic is fed into a pulse generator that in turns drives the level shifting sructure (that include two High Voltage DMOS) designed to ensure low power dissipation and high noise immunity. The output buffer (in Totem Pole arrangement) is able to sink from or source to the gate of the external device the current needed to switch it ON or OFF.

The falling edge of the signal coming from the input logic will turn ON while the rising edge will turn OFF the driven power device. This operation will ensure low current sinking from the HV rail during commutations.

Current / Voltage Mode Operation

To select the Voltage Mode Operation the user have to set on the RI pin a voltage higher than the internal reference (7V). In this way the IC will function as an inverting buffer driven by the LI input pin (see Voltage Mode Timing Diagram).

If the voltage on RI input pin is lower than 7V the Current Mode Operation will be enabled. In this configuration the RI input will set the reference voltage to the non inverting input of the Current Mode Comparator (see block diagram), whose inverting input, the CI input pin, in allowable to close a current control loop with a voltage drop coming from a sense resistor. To summarise (see Current Mode Timing Diagrams):

The output of the Current Mode Comparator will mask the LI input whenever the CI voltage is higher than the RI input (and the RI voltage is below 7V).

Under Voltage Lockout

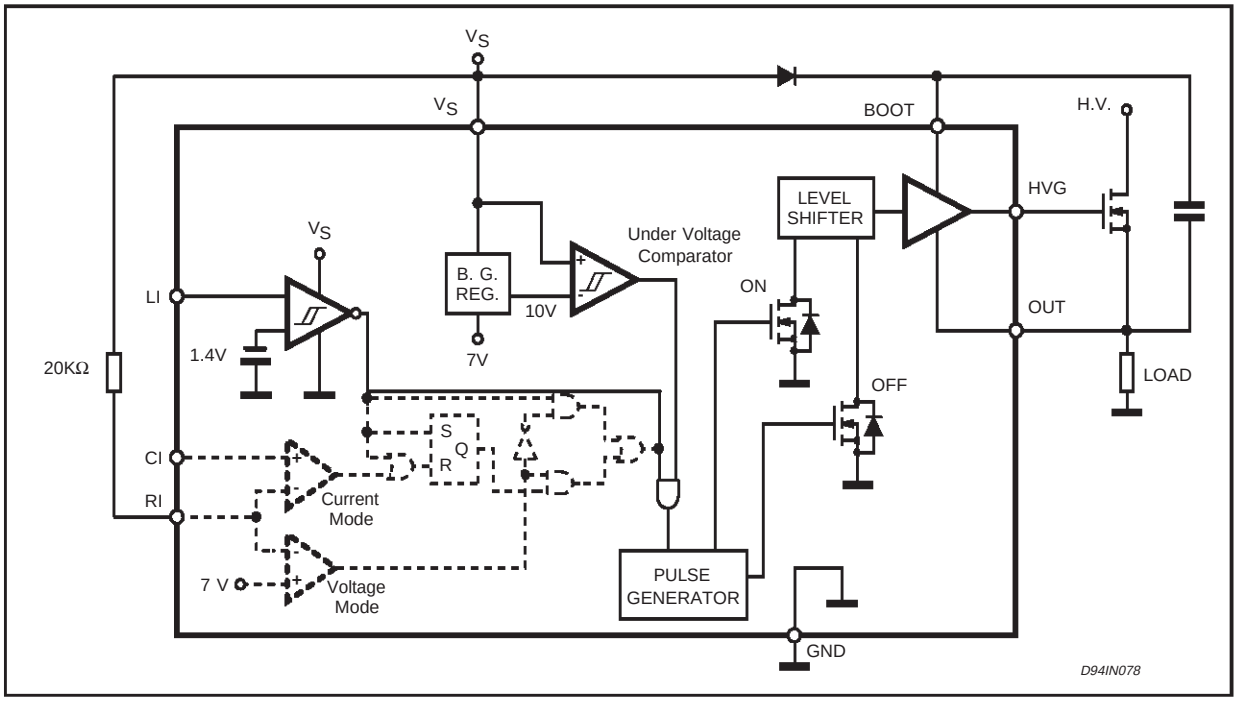
The output buffer if switched off whenever Vs decrease below Vth OFF.

The IC will remail in this shut down status until Vs has risen above VthON, the hysteresis will provide a good noise immunity.

Applications

The L6380/L6381 can be used in motor control applications (AC, DC and switched reluctance), electronic ballasts, heating and welding, switching power supplies and UPS.

L6381 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

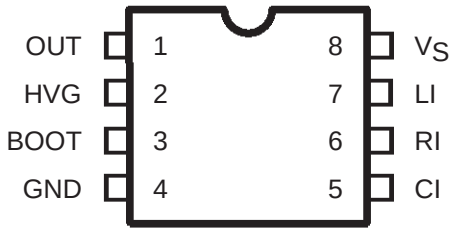
Symbol	Parameter	Value	Unit
V_{BOOT}	Supply voltage of bootstrapped section	600+V_S	V
V_{HVG}	Gate voltage of upper driver	600+V_S	V
V_{OUT}	Output voltage	600	V
V_{BOOT} - V_{OUT}	Difference between boot voltage and output voltage	18	V
V_{HVG} - V_{OUT}	Difference between gate voltage of upper gate and output voltage	18	V
V_S	Supply voltage	18	V
V_{IN}	Input voltage	V_S-2V	V
dV_{OUT}/dt	Transient offset supply voltage	±50	V/ns
V_{OUT} - V_{GND}	Difference between output voltage and ground ($t_p \leq 100$ ns)	-10	V
T_{amb}	Ambient Temperature Range (operative)	-25 to +85	°C
T_J	Junction temperature	150	°C
T_{ST}	Storage temperature	-40 to +150	°C
P_{tot}	Total Power Dissipation (at T_j = 85°C)	650	mW

Note: ESD immunity for pins 1, 2 and 3 is guaranteed up to 900V (Human Body Model)

THERMAL DATA

Symbol	Parameter		MINIDIP	SO8	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance, Junction Ambient	Max.	100	150	°C/W

L6380 PIN CONNECTION (Top view)



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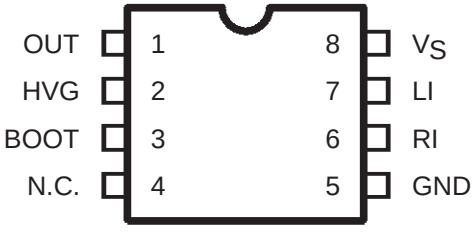
L6381 PIN CONNECTION (Top view)



D94IN081

ELECTRICAL CHARACTERISTICS

DC OPERATION (V_S = 15V; T_j = 25°C; unless otherwise specified.)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	8	Supply Voltage (operative)				17	V
V_{thON}		UV Turn-On Theshold		10	10.5	11	V
V_{thOFF}		UV Turn-Off Theshold		9	9.5	10	V
V_{Shys}		UV Hysteresis		0.5	0.75	1	V
I_q		Quiescent Current Before Start-Up	V_S≤8V		300	700	mA
I_{qs}		Quiescent Supply Current			2	3	mA
V_{il}	7	Logic Input Low Level				0.8	V
V_{ih}		Logic Input High Level		2			V
V_{co}	6 vs 5	Input Comparator Offset				100	mV
V_{thRI}	6	Mode Selection Internal Threshold Voltage		6.5	7	7.5	V
I_{so}	2	Source Current	V_{BOOT}-V_{OUT}=12V; V_{HVG}-V_{OUT}=0V; t_p≤10µs	130		230	mA
I_{si}		Sink Current	V_{BOOT}-V_{OUT}=12V; V_{HVG}-V_{OUT}=6V; t_p≤10µs	-320		-180	mA
I_{qBOOT}	3	Boot Supply Quiescent Current	V_{HVG} = V_{BOOT}		70		µA
$I_{lkgBOOT}$		Boot Leakage Current	V_{BOOT}=500V			10	µA
I_{lkgHVG}	2	Gate Driver Leakage Current	V_{HVG}=500V			10	µA
I_{lkgOUT}	1	Output Leakage Current	V_{OUT}=500V			10	µA
I_{bias}	5, 6	Input Bias Current				2	µA
	7					30	µA

AC OPERATION (V_S = 15V; T_j = 25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_r	Gate Driver Rise Time	C_L(HVG, OUT)=1nF; V_{OUT}=0 to 500V		70	100	ns
t_f	Gate Driver Fall Time			50	100	ns
t_{ON}	Turn-On Delay				400	ns
t_{OFF}	Turn-Off Delay				400	ns

Figure 1: AC Operation Test Circuit

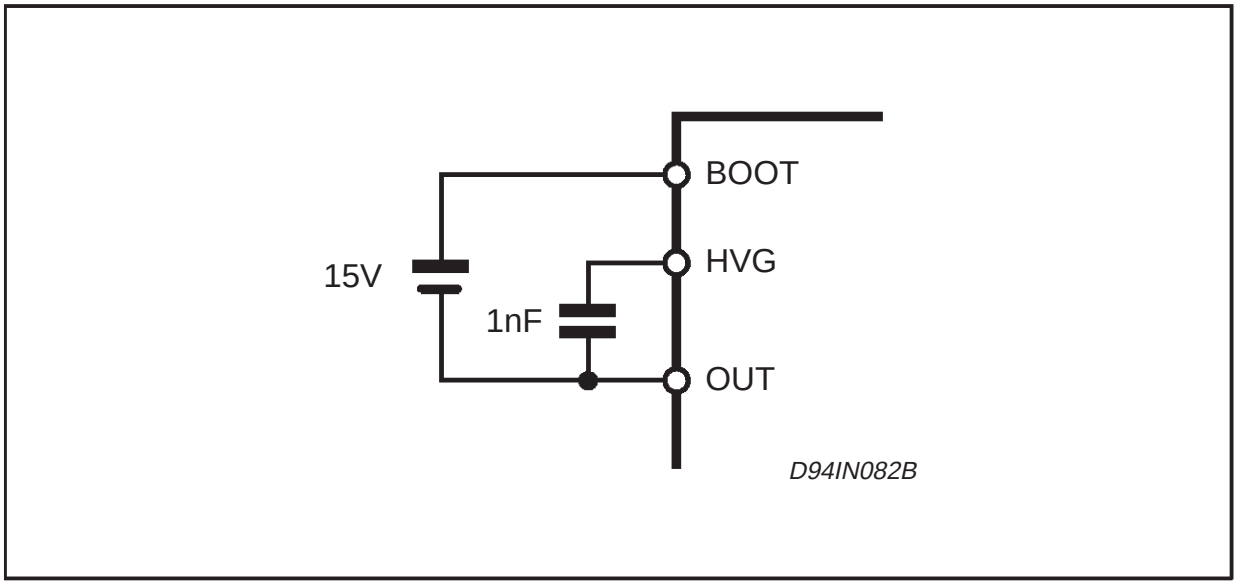
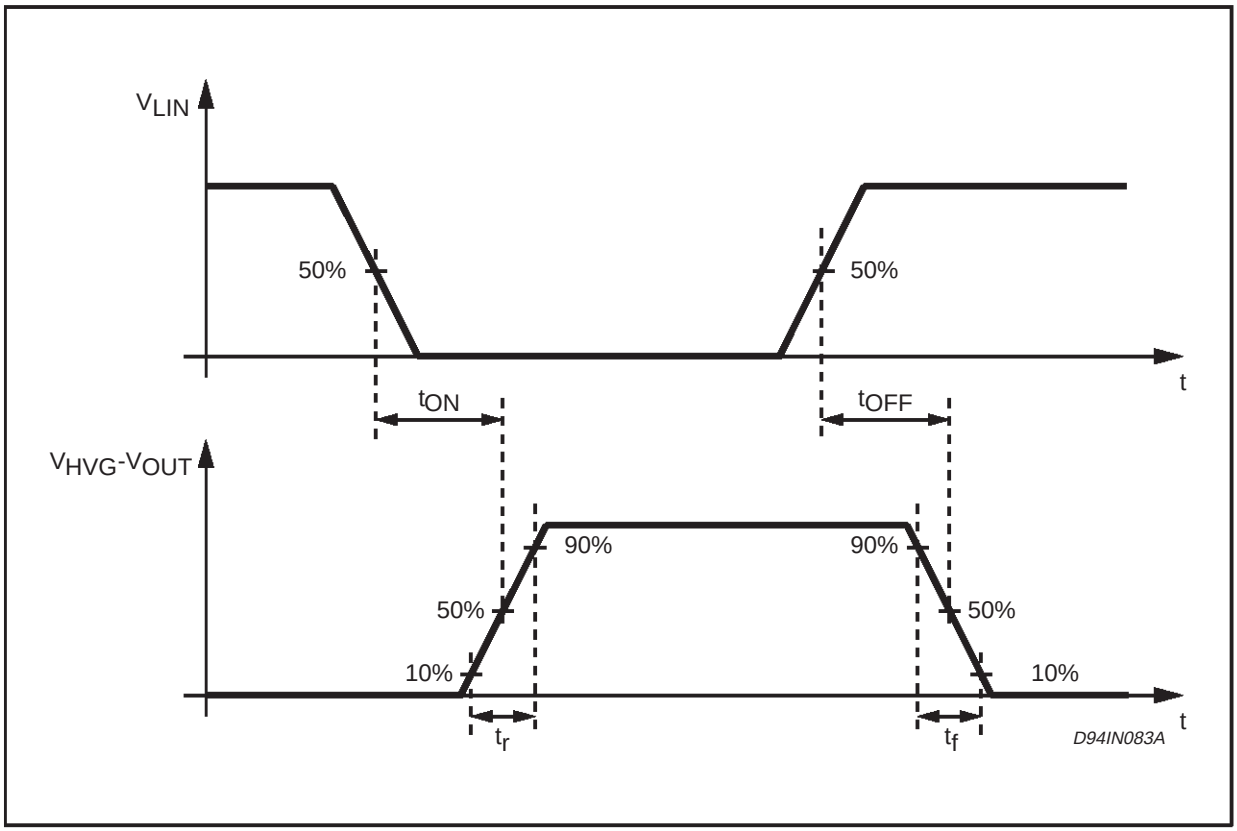
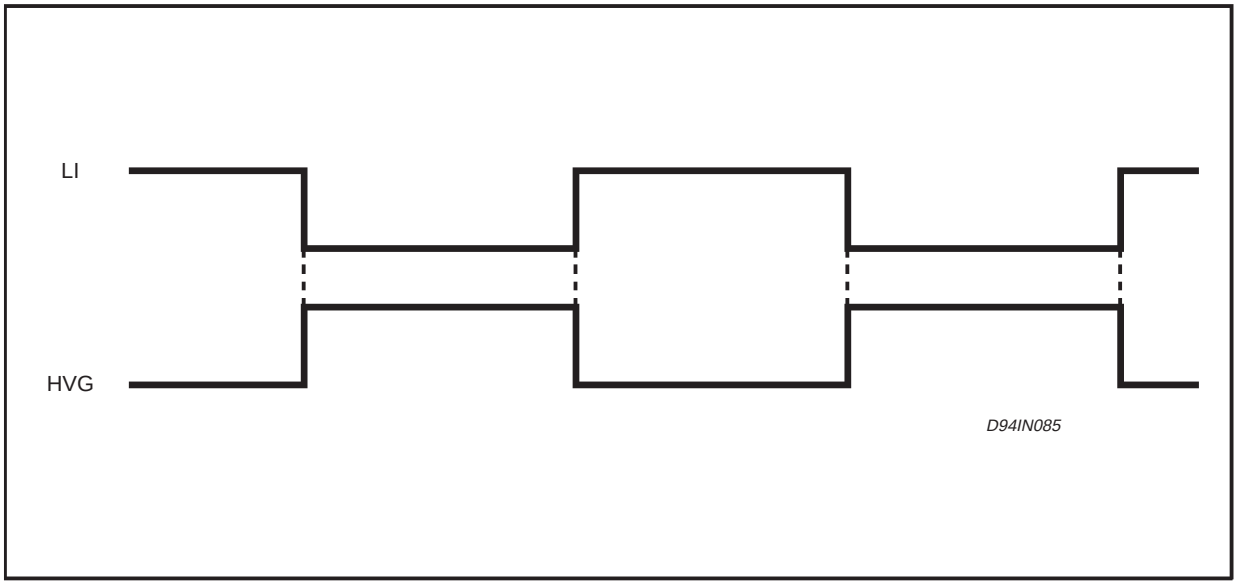


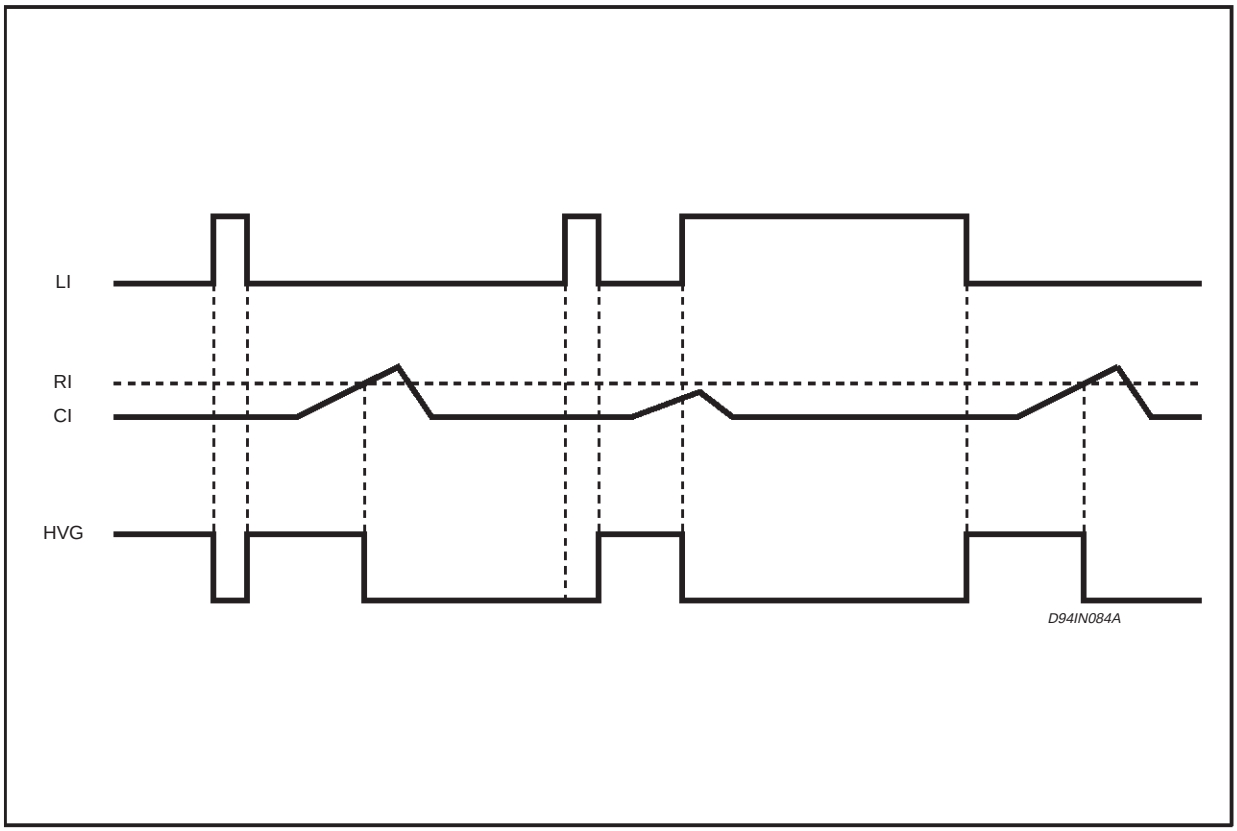
Figure 2: Switching Waveforms

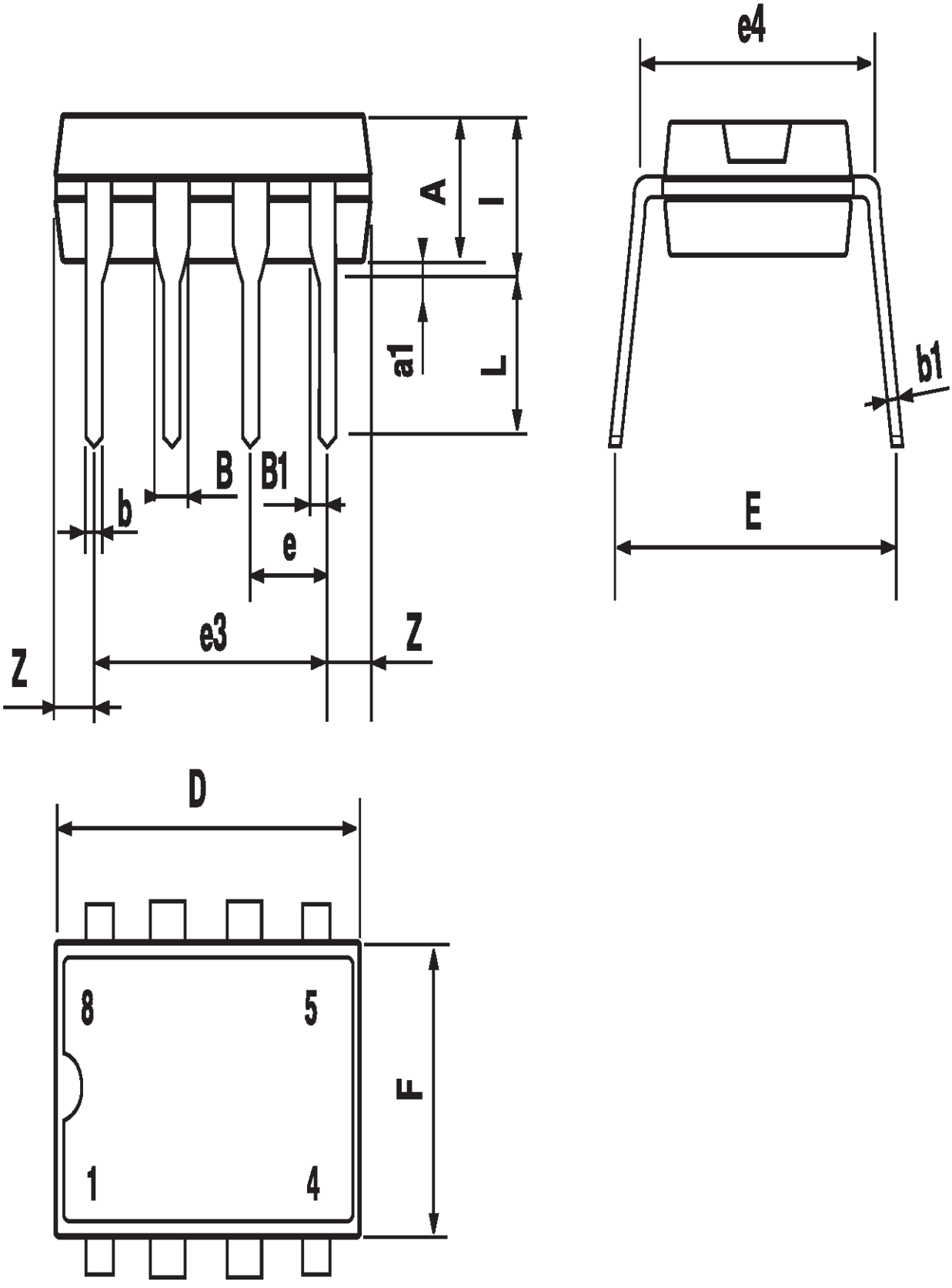


Voltage Mode Timing Diagrams



Current Mode Timing Diagrams

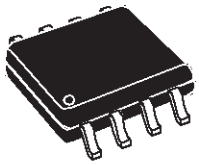



e4
A
L
a1
b1
B
B1
b
e
E
e3
Z
Z
D
8
5
1
4
F

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



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