DATA SHEET

DECEMBER, 1998
Revision 1.1

LXT981 Single-Speed, 5-Port Fast Ethernet Repeater

with Integrated Management Support

General Description

The LXT981 is a 5-port Class II Fast Ethernet Repeater that is fully compliant with IEEE 802.3 standards. Four ports directly support 100BASE-TX copper media and also support 100BASE-FX fiber media via pseudo-ECL (PECL) interfaces. The fifth port, a 100 Mbps Media Independent Interface (MII), connects to Media Access Controllers (MACs) for bridge/switch applications. The MII can also be configured to interface to another PHY device, such as the LXT970.

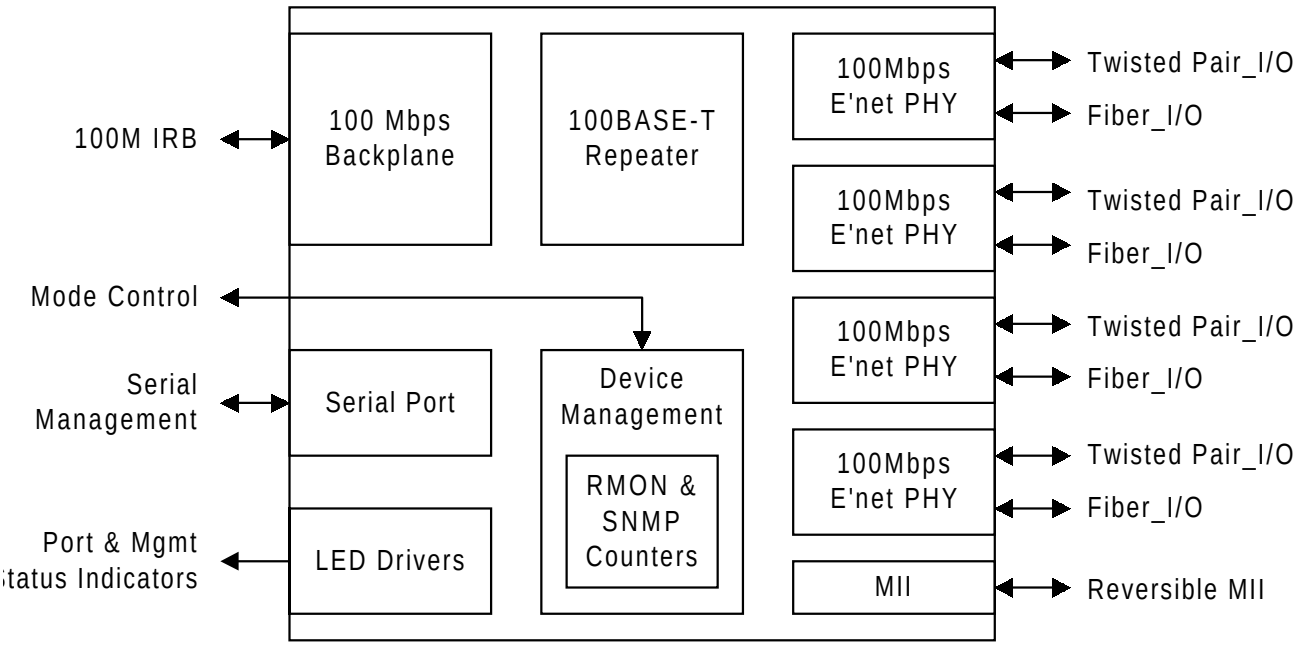
The LXT981 provides an Inter-Repeater Backplane (IRB) for expansion, operating at 100 Mbps. Up to 240 ports can logically be combined into one repeater using this backplane. The LXT981 supports SNMP and RMON management via on-chip 32- and 64-bit counters. The counters and control information are accessible via a high-speed Serial Management Interface (SMI). The device supports two source address tracking registers per port and a source address matching function.

The LXT981 enables cost-efficient 100BASE-TX intelligent repeater systems for stackable/modular and stand-alone applications.

Features

- Four 100 Mbps ports with complete twisted-pair PHYs including integrated filters and 100BASE-FX PECL interfaces.
- MII port connection to either MAC or PHY.
- Cascadable IRBs.
- Hardware assist for RMON and the Repeater MIB.
- High-speed SMI.
- Two address-tracking registers per port.
- Source address matching function.
- Integrated LED drivers with user-selectable modes.
- Available in 208-pin QFP package.
- Case temperature range: 0-115°C.

LXT981 Block Diagram



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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT981 Pin Assignments

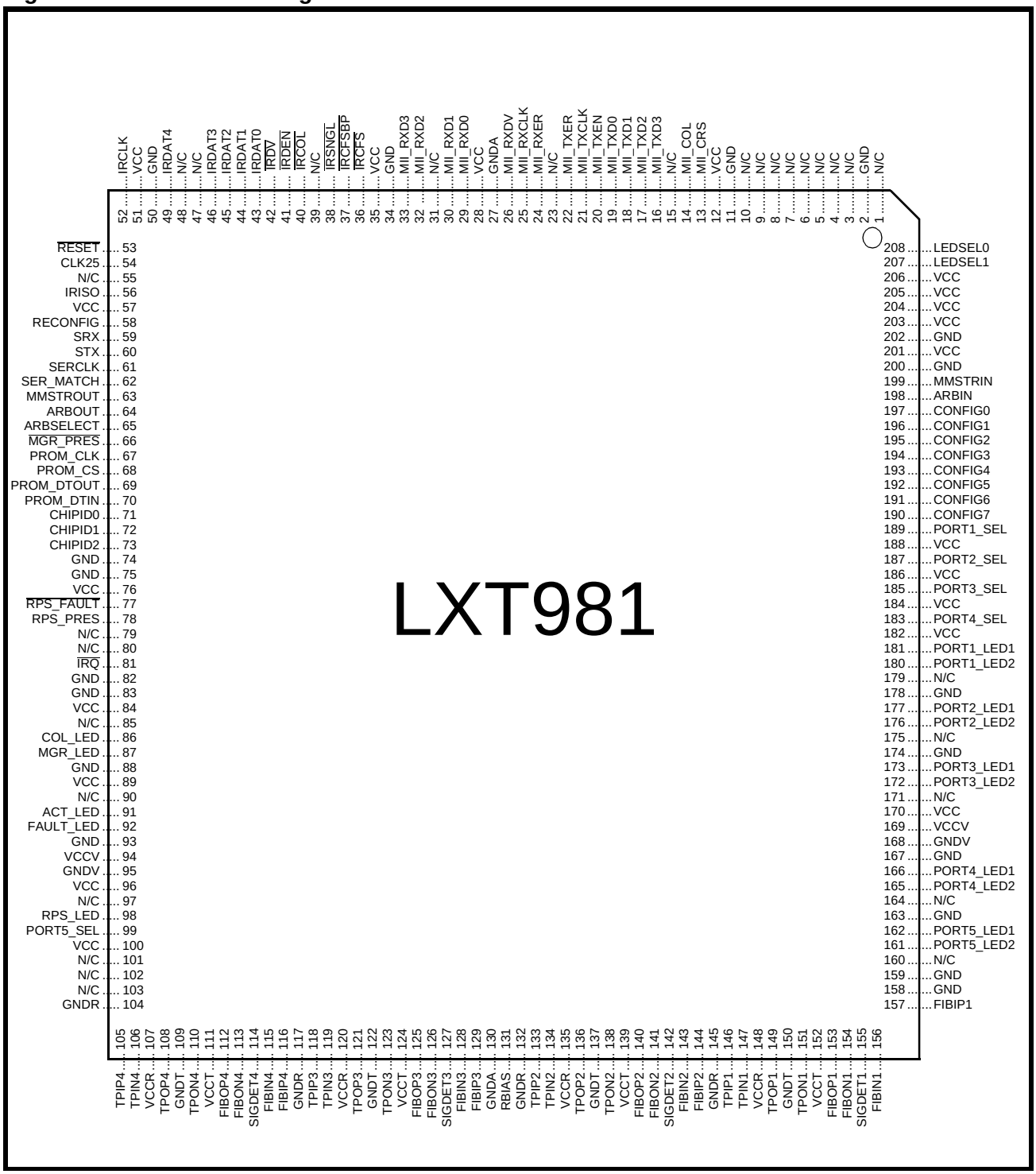


Table 1: Mode Control Signal Descriptions

Pin	Symbol	Type[1]	Description
189	PORT1_SEL	TTL Input PU Latched on reset	**Mode Select - Ports 1 through 4.** These pins set the default value of the Port Mode Control Register for the associated port as follows: Low = 100BASE-FX High = 100BASE-TX
187	PORT2_SEL		
185	PORT3_SEL		
183	PORT4_SEL		
99	PORT5_SEL	Input, PU	**Mode Select - Port 5.** Selects operating mode of the MII interface. Pin is monitored at power-up and reset. Subsequent changes have no effect. High = PHY Mode (LXT981 acts as PHY side of the MII) Low = MAC Mode (LXT981 acts as MAC side of the MII)

1. NC = No Clamp. Pad will not clamp input in the absence of power.
PU = Input contains pull-up.
PD = Input contains pull-down.
I/O = Input / Output
TTL = Transistor-Transistor Logic..

Table 2: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
149, 151	TPOP1, TPON1	Analog Output	**Twisted-Pair Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports' twisted-pair line drivers. These pins can be left open when not used.
136, 138	TPOP2, TPON2		
121, 123	TPOP3, TPON3		
108, 110	TPOP4, TPON4		
146, 147	TPIP1, TPIN1	Analog Input	**Twisted-Pair Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports' twisted-pair receivers. These pins can be left open when not used.
133, 134	TPIP2, TPIN2		
118, 119	TPIP3, TPIN3		
105, 106	TPIP4, TPIN4		

Table 3: Fiber Port Signal Descriptions

Pin	Symbol	Type	Description
153, 154	FIBOP1, FIBON1	Output PECL	**Fiber Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports' PECL drivers. These pins can be left open when not used.
140, 141	FIBOP2, FIBON2		
125, 126	FIBOP3, FIBON3		
112, 113	FIBOP4, FIBON4		

Table 3: Fiber Port Signal Descriptions – continued

Pin	Symbol	Type	Description
157, 156 144, 143 129, 128 116, 115	FIBIP1, FIBIN1 FIBIP2, FIBIN2 FIBIP3, FIBIN3 FIBIP4, FIBIN4	Input PECL	**Fiber Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports' PECL receivers. These pins can be left open when not used.
155 142 127 114	SIGDET1 SIGDET2 SIGDET3 SIGDET4	Input PECL	**Signal Detect - Ports 1 through 4.** Signal detect for the fiber ports. These pins can be left open when not used.

Table 4: PHY Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Output	**Receive Data.** The LXT981 transmits received data to the controller on these outputs. Data is driven on the falling edge of MII_RXCLK.
26	MII_RXDV	Output	**Receive Data Valid.** Active High signal, synchronous to MII_RXCLK, indicates valid data on MII_RXD<3:0>.
25	MII_RXCLK	Output	**Receive Clock.** MII receive clock for expansion port. This is a 2.5 or 25 MHz clock derived from the CLK25 input (refer to Table 11).
24	MII_RXER	Output	**Receive Error.** Active High signal, synchronous to MII_RXCLK, indicates invalid data on MII_RXD<3:0>.
22	MII_TXER	Input	**Transmit Error.** The MAC asserts this input when an error has occurred in the transmit data stream and responds by sending 'Invalid Code Symbols' on the line.
21	MII_TXCLK	Output	**Transmit Clock.** 2.5 or 25 MHz continuous output derived from the 25 MHz input clock.
20	MII_TXEN	Input	**Transmit Enable.** External controllers drive this input High to indicate that data is being transmitted on the MII_TXD<3:0> pins. Tie this input Low if it is unused.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Input	**Transmit Data.** External controllers use these inputs to transmit data to the LXT981. The LXT981 samples MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Output	**Collision.** Signal is driven High to indicate that a collision has occurred.
13	MII_CRS	Output	**Carrier Sense.** Active High signal indicates transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode. All MII signals are Transistor-Transistor Logic (TTL).

Table 5: MAC Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Input	**Receive Data.** The LXT981 receives data from the PHY on these pins. Data is sampled on the rising edge of MII_RXCLK.
26	MII_RXDV	Input	**Receive Data Valid.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate valid data on MII_RXD<3:0>.
25	MII_RXCLK	Input	**Receive Clock.** MII receive clock for expansion port. This is a 25 MHz clock.
24	MII_RXER	Input	**Receive Error.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate invalid data on MII_RXD<3:0>.
22	MII_TXER	Output	**Transmit Error.** The LXT981 asserts this signal asserted when an error has occurred in the transmit data stream.
21	MII_TXCLK	Input	**Transmit Clock.** 25 MHz continuous input clock. Must be supplied from same source as CLK25 system clock.
20	MII_TXEN	Output	**Transmit Enable.** The LXT981 drives this output High to indicate that data is being transmitted on the MII_TXD<3:0> pins.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Output	**Transmit Data.** The LXT981 drives these outputs to transmit data to the PHY. The device drives MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Input	**Collision.** The PHY asserts this active High signal to notify the LXT981 that a collision has occurred.
13	MII_CRS	Input	**Carrier Sense.** The PHY asserts this active High signal to notify the LXT981 that the PHY is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.
All MII signals are Transistor-Transistor Logic (TTL).

Table 6: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type[1]	Description[2]
199	MMSTRIN	TTL Input PD, NC	**Management Master Input.** The Management Master (MM) daisy chain ensures that collisions will be counted correctly in multi-board applications. Attach the MMSTRIN input of each device to the MMSTROUT output of the previous device. Ground MMSTRIN of the first or only device.
63	MMSTROUT	Output	**Management Master Output.** MM daisy chain output. In hot-swap applications, a 1 kΩ - 3 kΩ resistor can be used as a bypass between MMSTRIN and MMSTROUT.
36	$\overline{\text{IRCFS}}$	Analog I/O	**IRB Collision Force Sense.** $\overline{\text{IRCFS}}$ is a three-level signal that determines the number of active ports on the "logical repeater." High level (5V) indicates no ports active; Mid level (approx. 2.8V) indicates one port active; Low level (0V) indicates more than one port active, resulting in a collision. This signal requires a 240Ω pull-up resistor and connects between chips on the same board. Do not connect between boards.
37	$\overline{\text{IRCFSBP}}$	Analog IO, NC	**IRB Collision Force Sense - Backplane.** This three-level signal functions the same as IRCFS, but connects between chips with ChipID = 0, on different boards. This signal requires a single 82Ω pull-up resistor on each stack.
38	$\overline{\text{IRSNGL}}$	I/O, Schmitt MOS PU	**Single Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from one or more ports. This signal should not be connected between boards.
40	$\overline{\text{IRCOL}}$	I/O, Schmitt MOS PU	**100 Mbps Multiple Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from more than one port (collision). It should not be connected between boards.
41	$\overline{\text{IRDEN}}$	Open Drain Output	**IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver ('245) used to buffer the 100 Mbps IRB in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all $\overline{\text{IRDEN}}$ outputs together. If $\overline{\text{IRDEN}}$ is tied directly to the DIR pin on a '245, attach the on-board IRDAT, IRCLK and $\overline{\text{IRDV}}$ signals to the "B" side of the '245, and connect the off-board signals to the "A" side of the '245.
42	$\overline{\text{IRDV}}$	I/O, Open Drain, Schmitt MOS PU	**IRB Data Valid.** This active Low signal indicates repeater port activity. $\overline{\text{IRDV}}$ frames the clock and data of the packet on the backplane. This signal requires a 120Ω pull-up resistor.
43 44 45 46 49	IRDAT0 IRDAT1 IRDAT2 IRDAT3 IRDAT4	I/O Tri-state Schmitt MOS PU	**IRB Data.** These bidirectional signals carry data on the IRB. Data is driven on the falling edge and sampled on the rising edge of IRCLK. These signals can be buffered between boards.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 6: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type[1]	Description[2]
52	IRCLK	I/O Tri-state Schmitt MOS, PD	**IRB Clock.** This bidirectional, non-continuous, 25 MHz clock is recovered from received network traffic. Schmitt triggering is used to increase noise immunity. This signal must be pulled to VCC when idle. One 1 kΩ pull-up resistor on both sides of a ‘245 buffer is recommended.
56	IRISO	Output	**Stack IRB Isolate.** This output allows one LXT981 per board the ability to enable or disable an external bidirectional transceiver (‘245). Attach the output to the Enable input of the ‘245. The output is driven High (disable) to isolate the IRB.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
2. Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 7: Serial Management Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
58	RECONFIG	TTL Input PD, NC	**Reconfigure**. This input controls the driving of the clock signal on the high-speed Serial Management Interface (SERCLK). When this input is High, the LXT981 drives SERCLK with a 625 kHz output. When this input is Low, SERCLK is an input to the LXT981. In addition, a Low-to-High transition on RECONFIG causes the LXT981 to drive 13 continuous 0s on the Serial Management Interface (SMI), causing a re-arbitration to occur.
62	SER_MATCH	Output	**Serial Match.** The LXT981 device with ChipID = 0 asserts this active High output whenever it detects a message on the SMI that matches the local Hub ID. Refer to Figure 10 on page 29.
59	SRX	TTL Input, PD	**Serial Receive.** Receive data input for the SMI. Must be tied to STX externally. SRX is sampled on the rising edge of SERCLK.
60	STX	Open Drain Output	**Serial Transmit.** Transmit data output for the SMI. Must be tied to SRX externally. Data transmitted on STX is compared with data received on SRX. In the event of a mismatch, STX is put in the high impedance state. STX is driven on the falling edge of SERCLK.
61	SERCLK	TTL Output, Tri-state, PD	**Serial Clock.** Clock for the SMI. Depending on RECONFIG, this pin is either a 625 kHz output or a 0 to 2 MHz input.
198	ARBIN	TTL Input, PD, NC	**Arbitration In/Out**. Used with Chain Arbitration. If used, tie ARBIN to ARBOUT of the previous device. ARBIN at the top of the daisy chain can be connected to ground or to ARBOUT of the SCC. If unused, tie ARBIN High.
64	ARBOUT	Output, NC	

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   TTL = Transistor-Transistor Logic.

Table 7: Serial Management Interface Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
65	ARBSELECT	TTL Input, PU	**Arbitration Mode Select.** 0 = EEPROM based, 1 = chain based.
66	$\overline{\text{MGR\_PRES}}$	Input, PU, NC	**Manager Present.** This signal is sensed at power-up and hardware reset. If the signal is High, it indicates that no local manager is present, and the LXT981 enables all ports and sets all LEDs to operate in “hardware mode”. If it is Low, indicating that a manager is present, the LXT981 disables all ports, pending control of network manager.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
PU = Input contains pull-up.
PD = Input contains pull-down.
TTL = Transistor-Transistor Logic.

Table 8: LED Signal Descriptions

Pin	Symbol	Type[1]	Description
208	LEDSEL0	TTL Input, PD	**LED Mode Select**. Must be static.
207	LEDSEL1		00 = Mode 1, 01 = Mode 2, 10 = Mode 3
181	PORT1_LED1	Output	**LED Driver 1 - Ports 1 through 5.** Programmable LED driver. Active Low. Refer to “Port LEDs” on page 20.
177	PORT2_LED1		
173	PORT3_LED1		
166	PORT4_LED1		
162	PORT5_LED1		
180	PORT1_LED2	Output	**LED Driver 2 - Ports 1 through 5.** Programmable LED driver. Active Low. Refer to “Port LEDs” on page 20.
176	PORT2_LED2		
172	PORT3_LED2		
165	PORT4_LED2		
161	PORT5_LED2		
86	COL_LED	Output	**Collision LED Driver.** Active Low indicates collision.
87	MGR_LED	Output	**Manager Present LED Driver.** Active Low indicates Manager present.
91	ACT_LED	Output	**Activity LED Driver.** Active Low indicates activity.
92	FAULT_LED	Output	**Fault LED Driver.** Active Low indicates global fault.
98	RPS_LED	Output	**Remote Power Supply LED Driver.** Active Low indicates RPS fault.

1. PD = Input contains pull-down.
TTL = Transistor-Transistor Logic.

Table 9: PROM Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
67	PROM_CLK	TTL Input Tri-State Output, PD	**PROM Clock.** 1 MHz clock for reading PROM data (ChipID = 0). If a PROM is not used, this pin must be tied Low.
68	PROM_CS	Output Tri-State	**PROM Chip Select.** Selects EPROM. An active High signal driven only by the chip with ID of 0.
69	PROM_DTOUT	Output Tri-State	**PROM Data Output.** Selects read instruction for EPROM. Active High signal driven only by the chip with ID of 0.
70	PROM_DTIN	TTL Input, PD	**PROM Data Input.** If PROM not used, can be tied Low or High.

1. PD = Input contains pull-down.

Table 10: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type[1]	Description
12, 28, 35, 51, 57, 76, 84, 89, 96, 100, 170, 182, 184, 186, 188, 201, 203-206	VCC	Digital	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 11, 34, 50, 74, 75, 82, 83, 88, 93, 158, 159, 163, 167, 174, 178, 200, 202	GND	Digital	**Ground.** Connect each of these pins to digital ground.
94, 169	VCCV	Analog	**VCO Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDV should be supplied for each of these pins
95, 168	GNDV	Analog	**VCO Ground**.
111, 124, 139, 152	VCCT	Analog	**Transmitter Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDT should be supplied for every one of these pins.
109, 122, 137, 150	GNDT	Analog	**Transmitter Ground.**
107, 120, 135, 148	VCCR	Analog	**Receiver Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDR should be supplied for every one of these pins

1. PU = Input contains pull-up; PD = Input contains pull down.

Table 10: Power Supply and Indication Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
104, 117, 132, 145,	GNDR	Analog	**Receiver Ground.**
131	RBIAS	Analog	**RBIAS.** Used to provide bias current for internal circuitry. The 100 µA bias current is provided through an external 22.1 kΩ, 1% resistor to GNDA.
27, 130	GNDA	Analog	**Analog Ground.**
78	RPS_PRES	TTL Input, PD	**Redundant Power Supply Present.** Active High input indicates presence of redundant power supply. Tie Low if not used.
77	$\overline{\text{RPS\_FAULT}}$	TTL Input, PU	**Redundant Power Supply Fault.** Active Low input indicates redundant power supply fault. The state of this input is reflected in the RPS_LED output (refer to Table 8). Tie High if not used.

1. PU = Input contains pull-up; PD = Input contains pull down.

Table 11: Miscellaneous Signal Descriptions

Pin	Symbol	Type[1]	Description
53	$\overline{\text{RESET}}$	CMOS Input Schmitt, NC	**Reset.** This active Low input causes internal circuits, state machines, and counters to reset (address tracking registers do not reset). On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5V. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an ‘LS14 or similar device.
54	CLK25	CMOS Input Schmitt	**25 MHz system clock.** Drive with MOS levels.
71 72 73	CHIPID0 CHIPID1 CHIPID2	TTL Input, PD	**Chip ID.** These pins assign unique ChipIDs to as many as eight devices on a single board. One device on each board must be assigned ChipID = 0.
81	$\overline{\text{IRQ}}$	Open Drain Output	**Interrupt request.** Active Low interrupt. Refer to Tables 58 and Figure 59 on page 66 for criteria and clearing options.

1. NC = No Clamp. Pad will not clamp input in the absence of power
PU = Input contains pull-up; PD = Input contains pull down.
TTL = Transistor-Transistor Logic..

Table 11: Miscellaneous Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
197 196 195 194 193 192 191 190	CONFIG0 CONFIG1 CONFIG2 CONFIG3 CONFIG4 CONFIG5 CONFIG6 CONFIG7	TTL Input PD	**Configuration Register Inputs.** These inputs allow the user to store system-specific information (board type, plug-in cards, status, etc.) in the Serial Configuration Register (address AC). This register may be read remotely through the Serial Management Interface.
1, 3-10, 15, 23, 31, 39, 47, 48, 55, 79, 80, 85, 90, 97, 101-103, 160, 164, 171, 175, 179	N/C	-	**No Connects.** Leave these pins unconnected.

1. NC = No Clamp. Pad will not clamp input in the absence of power
PU = Input contains pull-up; PD = Input contains pull down.
TTL = Transistor-Transistor Logic..

FUNCTIONAL DESCRIPTION

Introduction

As a fully integrated IEEE 802.3 repeater with 100 Mbps functionality, the LXT981 is a very versatile device allowing great flexibility in Ethernet design solutions. Figures 2, 3, and 4 show some typical applications, and Figure 5 shows a more complete I/O circuit. Refer to Application Information (page 33) for specific circuit implementations.

This multi-port repeater provides four 100BASE-TX/ 100BASE-FX ports. In addition, there is a bidirectional Media Independent Interface (MII) expansion port that may be connected to either a MAC, or to a PHY.

The LXT981 provides a repeater state machine and an Inter-Repeater Backplane (IRB) for 100 Mbps operation. The repeater fully meets IEEE 802.3 Class II requirements. Each port may be configured independent of the other ports.

The LXT981 incorporates RMON support by providing on-chip counters and hardware assistance for a fully managed environment. The backplane allows multiple devices to be stacked and function as one logical repeater.

Port Configuration

At power-up, hardware reset or software reset (but not at repeater reset), the LXT981 reads the hardware configuration pins to determine operating conditions for each of its ports. Each of the four media ports has its own configuration pin (PORT*n*_SEL) to select 100TX or 100FX operation (High = TX, Low = FX).

Figure 2: Typical LXT981 Managed Repeater Architectures

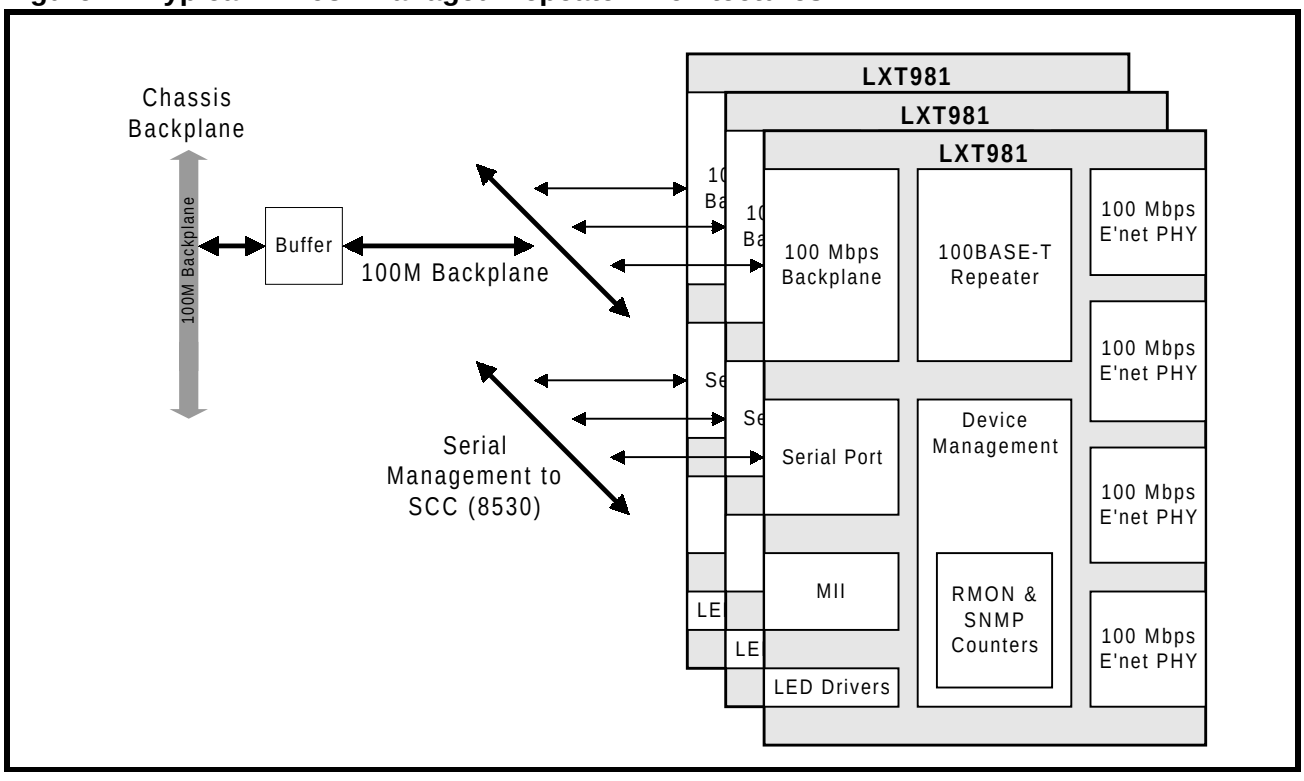


Figure 3: Typical Unmanaged Repeater Architectures

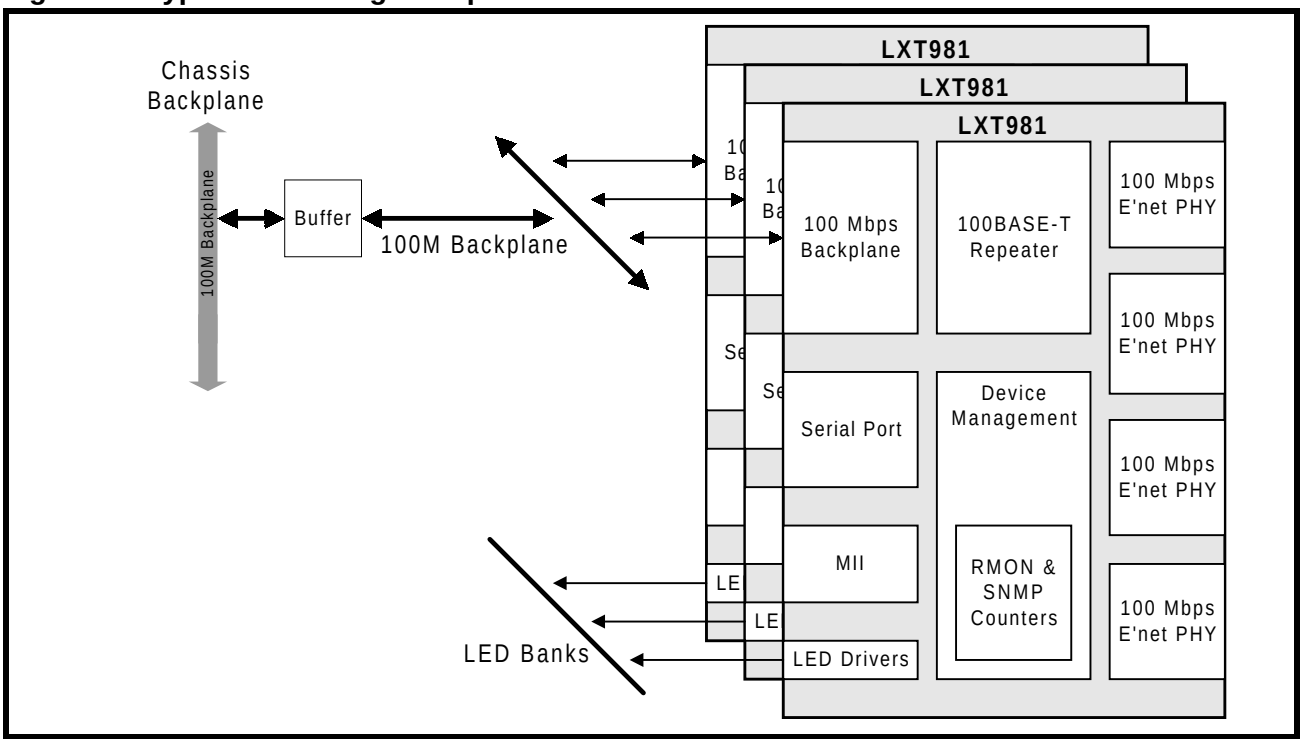


Figure 4: Typical Hybrid Switch/Repeater Application

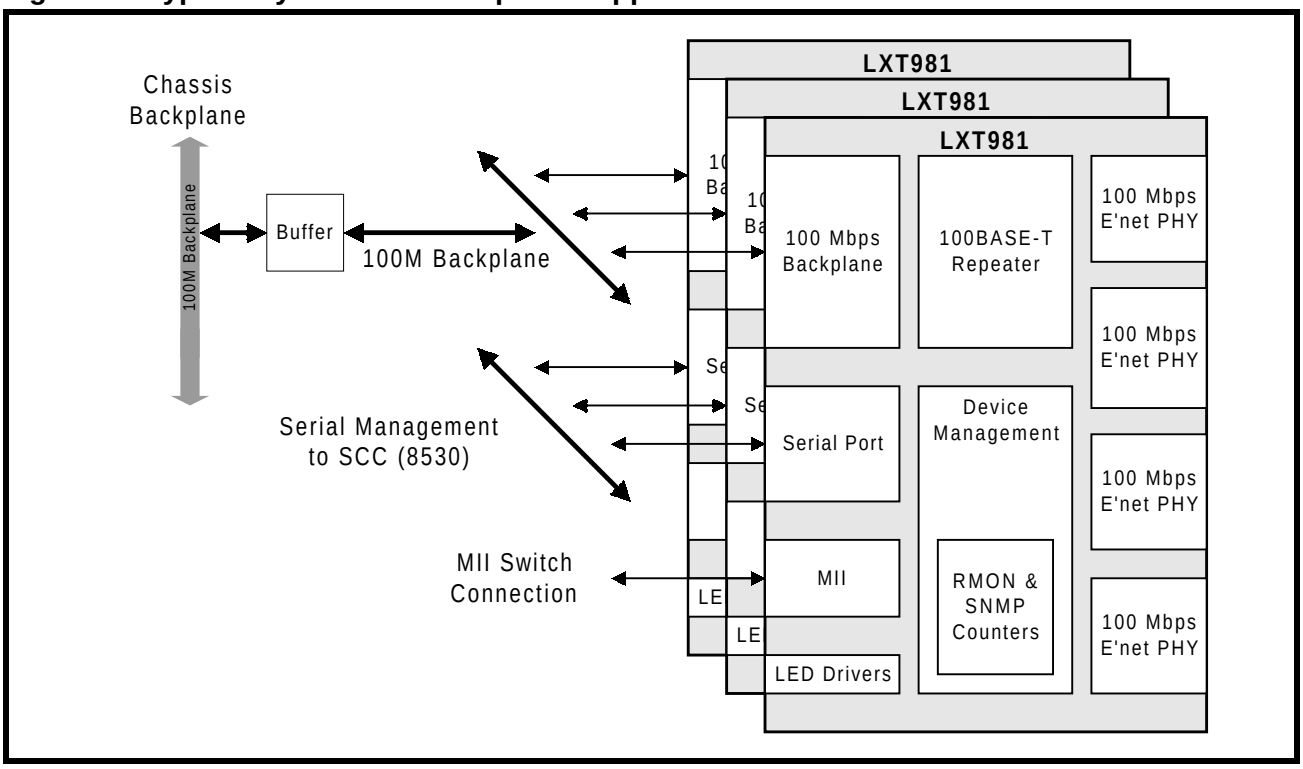
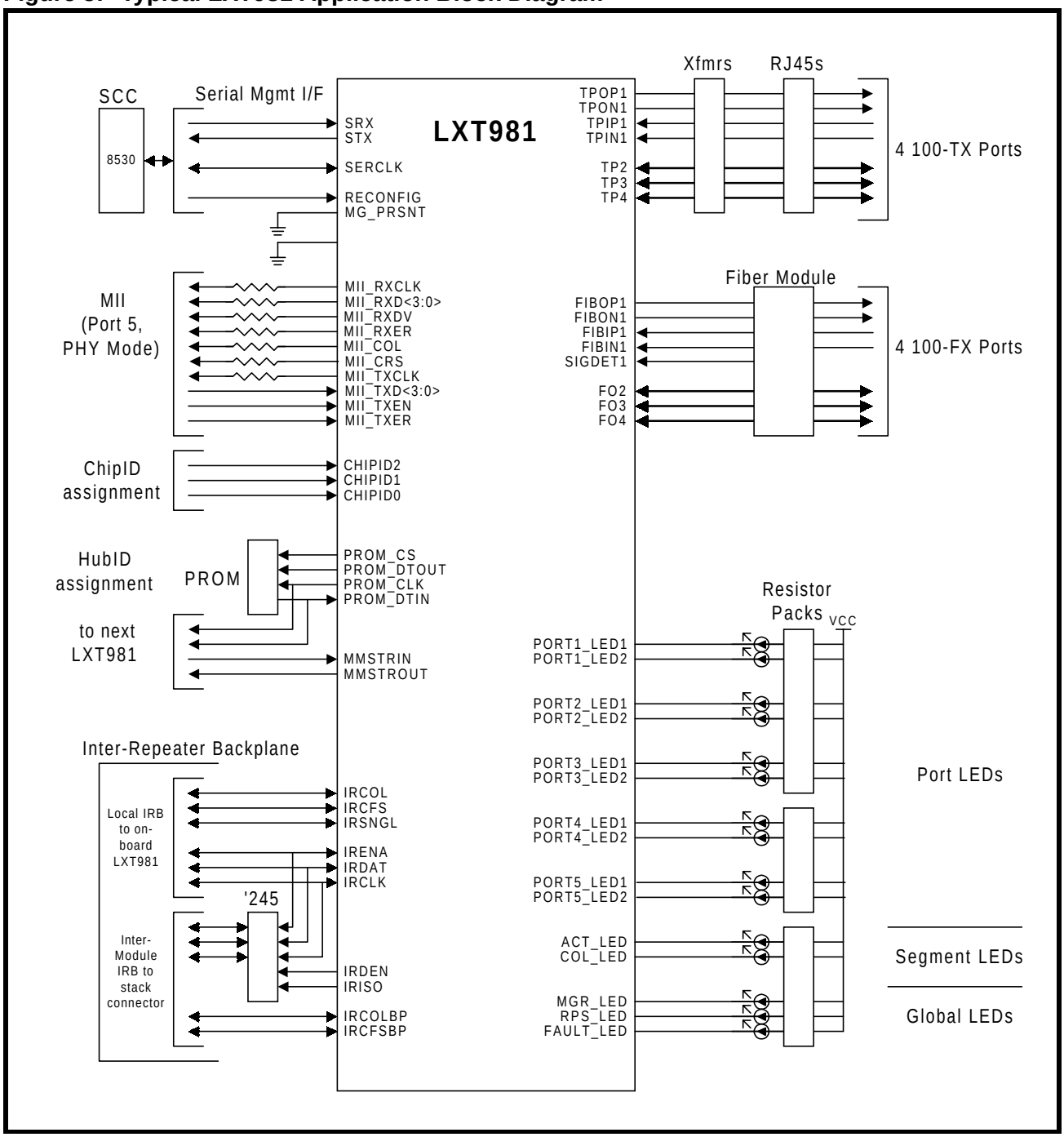


Figure 5: Typical LXT981 Application Block Diagram



Interface Descriptions

100BASE-TX Interface

The twisted-pair interface for each port consists of two differential signal pairs—one for transmit and one for receive. The transmit signal pair is TPOP/TPON, the receive signal pair is TPIP/TPIN. Refer to Table 2 for 100BASE-T port pin assignments and signal descriptions. The twisted-pair interface for a given port is enabled at all times except when 100FX is selected.

The transmitter is current driven and requires magnetics with 2:1 turns ratio. A 400Ω resistive load should be placed across the TPOP/N pair, in parallel with the magnetics. The centertap of the primary side of the transmit winding must be tied to a quiet VCC for proper operation. When the twisted-pair interface is disabled, the transmitter outputs are tri-stated.

The receiver requires magnetics with a 1:1 turns ratio, and a load of 100Ω. When the twisted-pair port is enabled, the receiver actively biases its inputs to approximately 2.8V. When the twisted-pair interface is disabled, no biasing is provided. A 4 kΩ load is always present across the TPIP/TPIN pair.

The LXT981 sends and receives a continuous, scrambled 125 Mbaud MLT-3 waveform on this interface. In the absence of data, IDLE symbols are sent and received in order to keep the link up.

100BASE-FX Interface

Each fiber interface consists of the FIBOP/FIBON (transmit) and FIBIP/FIBIN (receive) signal pair. Refer to Table 3 for 100BASE-FX port pin assignments and signal descriptions. Each interface also provides a Signal Detect input that can be tied to the corresponding output on the fiber transceiver for determining signal presence and quality.

The transmit pair is biased to approximately 1.5V and generally must be AC-coupled to the transceiver. The receive pair will accommodate an input bias in the 2V-5V range, and can be DC-coupled to the transceiver. Refer to Figure18 for a typical interface circuit.

The fiber interface for each port is enabled when the mode select is set to 100FX, and is disabled in all other cases. When a fiber port is disabled, its outputs are pulled to ground, and its inputs are tri-stated. The input and output pins on unused fiber ports may be left unconnected.

Each fiber port transmits and receives a continuous, 1V peak-to-peak, non-scrambled, NRZI waveform. The LXT981 does not support scrambling on the fiber interface.

Remote Fault Reporting

The SD pin detects signal quality and reports a remote fault if the signal quality starts to degrade. Loss of signal quality will also block any further data from being received and causes loss of the link. The remote fault code consists of 84 consecutive 1s followed by a single 0, and is transmitted at least three times. The LXT981 transmits the remote fault code and sets the associated interrupts when both of the following conditions are true:

- Fiber mode is selected
- Signal Detect indicates no signal, or the receive PLL cannot lock

Media Independent Interface

The LXT981 supports a standard Media Independent Interface (MII) interface. This interface can be programmed to operate either as the PHY side of the interface (PHY mode) or as the MAC side of the interface (MAC mode). The MII always operates as a nibble-wide (4B) interface. Symbol mode (5B interface) is not supported on the LXT981 MII.

NOTE

The MII does not auto-negotiate, auto-speed select, auto-link, or partition.

Serial Management Interface

The Serial Management Interface (SMI) provides system access to the status, control, and statistic gathering abilities of the LXT981. The interface is designed to allow multiple devices to be managed from a single multi-drop (daisy-chain) connection, and to use the minimum number of signals (2) for ease of system design.

The interface itself consists of two digital NRZ signals —clock and data. Refer to Table 7 for serial management I/F pin assignments and signal descriptions. Data is framed into HDLC-like packets, with a start/stop flag, header and CRC field for error checking. Zero-bit insertion/removal is used. The interface can operate at any speed from 0 to 2 Mbps.

Address assignment is provided via one of two arbitration mechanisms which are activated whenever the device is powered up or reset/reconfigured. Refer to the section on the SMI Refer to “Address Arbitration” on page 30.

Inter-Repeater Backplane

The LXT981 provides an Inter-Repeater Backplane (IRB), which allows multiple cascaded LXT981 devices to function as one large repeater. Up to 240 ports can be supported in a single cascade (192 TP ports + 48 MII ports). This provides support for stackable and modular hub architectures. Refer to Table 6 on page 8 for IRB pin assignments and signal descriptions.

Repeater Operation

The LXT981 contains a complete 100 Mbps Repeater State Machine (100RSM) that is fully IEEE 802.3 Class II compliant. Multiple LXT981s can be cascaded on the IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The IRB is a 5-bit symbol-mode interface. It is designed to be stackable.

The LXT981 maintains a complete set of statistics for its local repeater segment. These are accessible through the high-speed management interface.

The LXT981 performs the following 100 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Handling of received code violations. The LXT981 will substitute the “H” symbol for all invalid received codes.
- SOP, SOJ, EOP, EOJ delay <46BT (class II compliant).
- Collision Enforcement. During a collision, the LXT981 drives a 1010 jam signal (encoded as Data 5 on TX links) to all ports until the collision ends. There is no minimum enforcement time.
- Partition. The LXT981 partitions any port that participates in excess of 60 consecutive collisions or one collision approximately 575.2 µs long. Once partitioned, the LXT981 continues monitoring and transmitting to the port, but will not repeat data received from the port until it properly un-partitions.
- Un-partition. The LXT981 supports two un-partition algorithms. The default algorithm, which complies with the IEEE 802.3 specification, un-partitions a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.
- The LXT981 also provides an alternate un-partition algorithm, which is available through the management interface. The alternate algorithm will un-partition a port on *either* transmit or receive of at least 450-560 bits without collision on the partitioned port.
- Isolate. The LXT981 will isolate any port that transmit more than two successive false carrier events. A false carrier event is defined as a packet that does not start with a /J/K symbol pair. Note: this is not the same function as the 100IRB isolate function, which involves segmenting the backplane.
- Un-isolate. The LXT981 will un-isolate a port that remains in the IDLE state for 33000 +/- 25% BT or that receives a valid frame at least 450-500 BT in length.
- /T/R generation. The LXT981 can insert a /T/R symbol pair (End of Stream Delimiter) on any incoming packet that does not include one. This feature is optional, and is enabled through the management interface.
- Jabber. The LXT981 will ignore any receiver that remains active for more than 57,500 bit times. The LXT981 exits this state when all jabbering receivers return to the idle condition.

The isolate and symbol error functions do not apply to the MII port.

Management Support

Configuration and Status

The LXT981 provides management control and visibility of the following functions:

- Reset and zeroing of counters
- Device and board configuration
- LED functions
- Source address tracking (per port)
- Source address matching (per chip)
- Device/revision ID

SNMP and RMON Support

The LXT981 provides SNMP and RMON support through its statistics gathering function. Statistics are gathered on all data that flows through the device for each of the ports, including the MII. The LXT981 also maintains statistics for the entire 100 Mbps repeater. Since cascaded LXT981s operate as a single logical repeater, any device in the cascade would maintain the same repeater statistics as any other device. All statistics are stored as 32- or 64-bit quantities.

Per-port counters include:

Readable Frames	Readable Octets	FCS Errors
Alignment Errors	FramesTooLong	ShortEvents
Runts	Collisions	LateEvents
VeryLongEvents	DataRateMismatch	AutoPartitions
Broadcast	Multicast	SA Changes
Isolates	Symbol Errors	

Source Address Management Functions

The LXT981 provides two source address management functions for all ports: source address tracking and source address matching. These functions allow a network manager to track source addresses at each port, or to identify any port that sourced a particular Source Address.

LED Drivers

The LXT981 provides 15 LED drivers:

- 2 mode-selectable port LED drivers (10 total)
- 2 segment LED drivers (activity and collision)
- 3 management LED drivers (manager present, global fault, and redundant power supply fault.

Refer to Table 8 for LED interface pin assignments and signal descriptions.

Requirements

Power

The LXT981 has four types of +5V power supply input pins: VCC, VCCV, VCCR, and VCCT). These inputs may be supplied from a single power supply although ferrites should be used to filter the power going to the analog and digital power planes. As a matter of good practice, these supplies should be as clean as possible. Specific operating recommendations are shown in the Test Specifications section, Table 23 on page 43.

Each supply input should be decoupled to its respective ground. Refer to Table 10 on page 11 for power and ground pin assignments, and to “General Design Guidelines” on page 33 for layout guidelines.

Clock

A stable, external 25 MHz system clock source (CMOS) is required by the LXT981. This is connected to the CLK25 pin. Refer to Test Specifications, Table 24 on page 43, for clock timing requirements.

Bias Current

The LXT981 requires a 22.1 kΩ, 1% resistor connecting its RBIAS input to ground.

Reset

At power-up, the reset input must be held low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive reset if there are multiple LXT981 devices. Refer to Figure 22 on page 42 for circuit details.

PROM

An external, auto-incrementing 48-bit PROM can be used for two purposes:

- to assign a unique ID to all LXT981s on a board
- to support the EPROM-based address arbitration mechanism on the Serial Management Interface (SMI). Refer to "Address Arbitration" on page 30.

Multiple devices on the same board can share a single common PROM. The LXT981 with ChipID = 0 actively reads the PROM at power-up; all other LXT981s listen in. If PROM arbitration is not used, the PROM data input signal must be tied either High or Low. Refer to Table on page 11 for PROM interface pin assignments and signal descriptions.

Chip ID

Each LXT981 on a board requires a unique 3-bit Chip ID value asserted on these pins in order for the SMI to function correctly. One LXT981 on each board must be assigned ChipID = 0.

When Substituting a LXT982 Device

The LXT982 can be substituted in LXT981 designs for an unmanaged single-speed solution without changing the LXT981 Chip ID pin states. The LXT981 Chip ID 0, Chip ID 1, and Chip ID 2 pins are renamed $\overline{\text{FPS}}$, GND, and GND respectively for the LXT982. For cascading, the first LXT982 device is addressed 000 and all others 001 as indicated by the pin names. The LXT982 requires one chip to have the LXT981-equivalent address 000 and all other LXT982s a non-000 address.

Management Master I/O Link

In multiple device applications, the Management Master daisy chain (MMSTRIN/MMSTROUT) ensures that collisions are counted correctly. Connect the MMSTRIN input to the MMSTROUT output of the previous device, even across board boundaries. Ground the MMSTRIN input of the first or only device in the system. In hot-swap applications, resistive bypassing can be used, with a value between 1 and 3 kΩ.

IRB Bus Pull-ups

Even when the LXT981 is used in a stand-alone configuration, pull-up resistors are required on the following IRB signals:

- IRCFS
- IRCFSBP
- IRDV
- IRCLK

Refer to Table 6 on page 8 for IRB pin assignments and signal descriptions. See Figure 21 on page 41 for sample circuits.

LED Operation

The LXT981 provides three types of LED indicators: port, segment, and management (refer to Table 8 on page 10). Three user-selectable LED modes determine which conditions are indicated on which pins, and how particular conditions are indicated. The LED mode is selected via the LEDSEL<1:0> pins and reflected in an internal register. The LEDs generally operate under hardware control although some limited software overrides are available. In addition to On and Off states, some LED drivers provide a blink state output.

Blink Rates

Two programmable blink rates are provided. The default period for the slow blink rate is 1.6s. The default period is 0.4s for the fast blink rate. These rates may be changed via the LED Timer Register. The slow blink rate is defined by the upper 8 bits and the fast blink rate is defined by the lower 8 bits of the LED Timer Register. Refer to Tables 66 through 68 for details.

Power-Up and Reset Conditions

During reset or power-up, all LEDs turn on steady and remain on for approximately 2 seconds after reset is cleared. After reset, the collision, activity, and redundant power supply LEDs revert to hardware control. The global fault and port LEDs revert to hardware control unless a manager is present in the system.

Port LEDs

Port LEDs are provided for the four twisted-pair ports and the MII port. The LXT981 has two LED driver pins for each port as described in Table 8. These pins can drive standard LEDs. Three user-selectable modes are provided

for the port LEDs. The information conveyed by the port LED states in each mode is listed in Tables 12 through 14.

Software Overrides of Port LEDs

The port LED Control Register allows limited software overrides of the Port LEDs. Two bits per port provide independent control of each port. However, both LEDs for the respective port receive the same override (both port *n* LEDs will be simultaneously set to On, Off, or Blink). Refer to Tables 62 and 67 for coding and bit assignments.

Segment LEDs

These outputs can directly drive LEDs to indicate activity and collision status. No software overrides are provided for these LED drivers, and they are not affected by LED mode selection. Pulse stretchers are used to extend the on-time for these LEDs.

Collision LED

The collision LED turns on for approximately 120 µs when the LXT981 detects a collision on the segment. During the time that the collision LED is on, any additional collisions are ignored by the collision LED logic.

Activity LED

The Activity LED turns on for approximately 4 ms when the LXT981 detects any activity on the segment. During the time that the activity LED is on, any additional activity is ignored by the activity LED logic.

Management LEDs

These LED driver outputs indicate management status conditions.

Manager Present LED

When active, this LED indicates the presence of a Manager in the system. It is not affected by LED mode selection and does not allow software overrides.

Global Fault LED

The global fault LED indicates one or more of the following conditions: any port partitioned, any port isolated or RPS fault. How the condition is indicated depends on the LED mode as shown in Tables 12 through 14.

Software Overrides of the Global Fault LED

Two bits in the global LED Control Register allow software overrides to control the global fault LED. Refer to Tables 62 and 66 for coding and bit assignments.

Redundant Power Supply LED

The redundant power supply LED is controlled by the RPS_FLT and RPS_PRES pins. The LED state reflects the states of these two inputs, depending on the LED mode selected as listed in Tables 12 through 14.

Table 12: LED Mode 1 Indications

LED	Hardware Control			Software Control
	On	Blink	Off	
PORT*n*LED1	Link up, not partitioned, not isolated	N/A	Any other state	Off via Port Led Control Register, address 0B2
PORT*n*LED2	Link up, partitioned or isolated	N/A	Any other state	
RPS	Present, fault	N/A	Any other state	N/A
Global FAULT	Any port partitioned, any port isolated or rps fault	N/A	Any other state	Off via global LED Control Register, address 0B1

Table 13: LED Mode 2 Indications

LED	Hardware Control			Software Control
	On	Blink	Off	
PORT*n*LED1	Port enabled, link up, not partitioned	Port enabled, partitioned, 10M or 100M with link (slow blink)	Any other state	On, Off, or Fast Blink via Port Led Control Register, address 0B2
PORT*n*LED2	N/A	N/A	Always off	
RPS	Present, no fault	Present, fault	Not present	N/A
Global FAULT	N/A	Any port partitioned, any port isolated or RPS fault (slow blink)	Any other state	On, Off, or Slow Blink via Global Led Control Register, address 0B1

Table 14: LED Mode 3 Indications

LED	Hardware Control			Software Control
	On	Blink	Off	
PORT*n*LED1	Link up, not partitioned, not isolated	N/A	Any other state	Off via port LED Control Register, address 0B2
PORT*n*LED2	Receive activity (20 ms pulse)	N/A	Any other state.	
RPS	Present, fault	N/A	Any other state	N/A
Global FAULT	Any port partitioned, any port isolated or rps fault	N/A	Any other state	Off via global LED Control Register, address 0B1

IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. This backplane uses a combination of digital and analog signals. IRB signals can be characterized by connection type as Local (connected between devices on the same board), Stack (connected between boards), or Full (connected between devices on the same board *and* between boards). Refer to Tables 15 and 16 for details on buffering and pull-up requirements, and to Figure 21 on page 41 for application circuitry.

IRB Isolation

The ISOLATE output is provided to control the enable pin of an external bidirectional transceiver. In multi-board applications, it can be used to isolate one board from the rest of the system. Only one device can control these signals. The output states of this pin are controlled by the isolate bits in the Master Configuration Register.

NOTE

Inter-board analog signals will be isolated internally by the device.

MMSTRIN, MMSTROUT

This daisy chain is provided for correct gathering of statistics in multiple-device configurations. In multiple-board applications, this daisy chain must be maintained across boards. In stand-alone applications, or for the first device in a chain, the MMSTRIN input must be pulled Low in order for the management counters to work correctly.

Table 15: IRB Signal Types

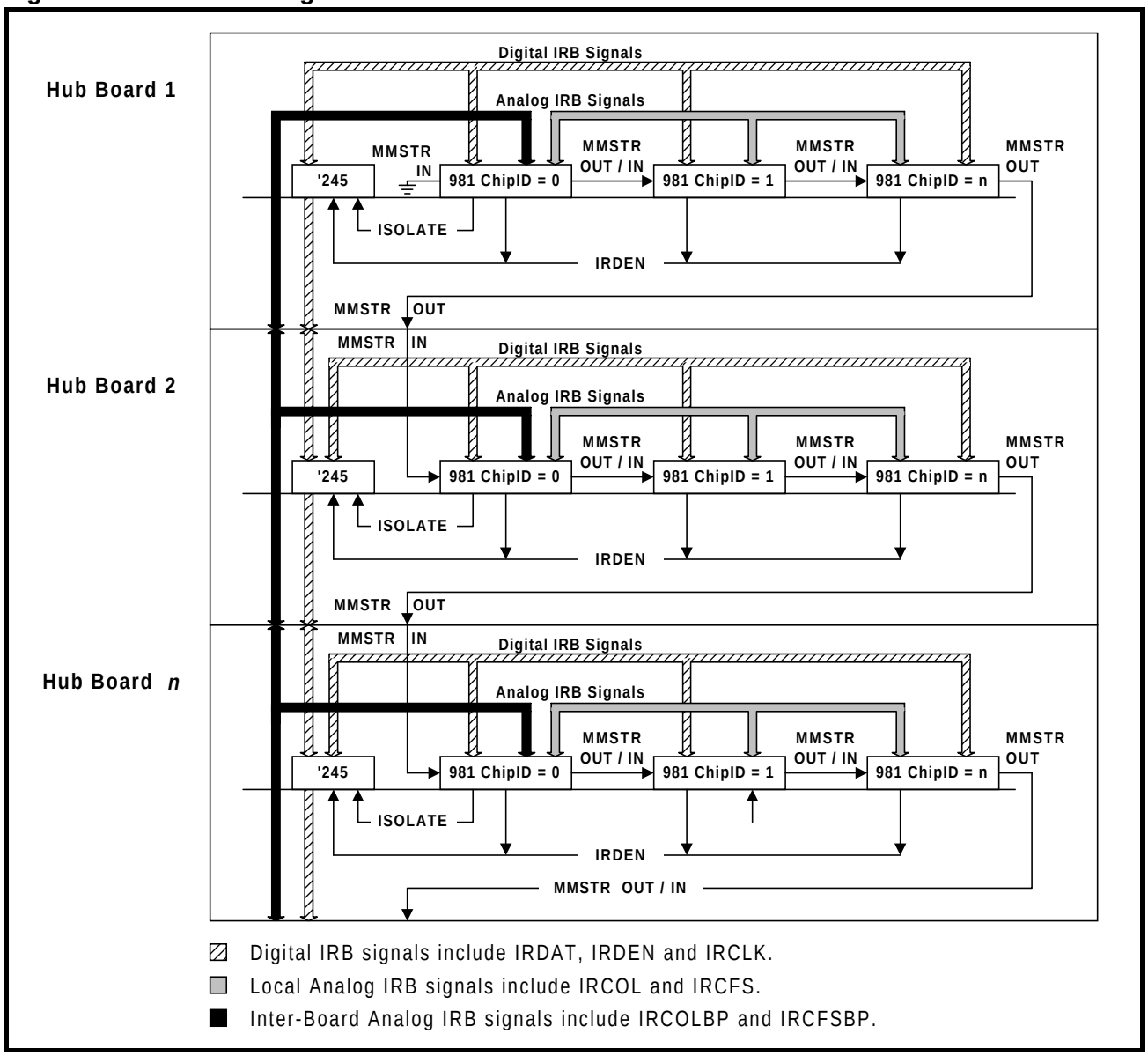
Connection Type	Connections Between Devices (same board)	Connections Between Boards
Full	Connect all.	Connect using buffers.
Local	Connect all.	Do not connect.
Stack	For devices with ChipID ≠ 0, pull-up at each device and Do Not Interconnect.	Connect devices with ChipID = 0 between boards. Use one pull-up resistor per stack.
Special (xxISO)	For devices with ChipID ≠ 0, leave open. For device with ChipID = 0, connect to buffer enable.	Do not connect.

Table 16: IRB Signal Details

Name	Pad Type	Buffer	Pull-up	Connection Type
100 Mbps IRB Signals				
IRDAT<4:0>	Digital	Yes	No	Full
IRCLK	Digital	Yes	1 kΩ	Full
$\overline{\text{IRDV}}$	Digital, Open Drain	Yes	120Ω	Full
$\overline{\text{IRCFS}}$	Analog	No	240Ω, 1%	Local
$\overline{\text{IRCFSBP}}$	Analog	No	82Ω, 1%	Stack
$\overline{\text{IRCOL}}$	Digital	No	No	Local
$\overline{\text{IRSNGL}}$	Digital	No	No	Local
$\overline{\text{IRDEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local
IRISO	Digital	N/A[1]	No	Special

1. Isolate and Driver Enable signals are provided to control an external bidirectional transceiver.

Figure 6: IRB Block Diagram



MII Port Operation

The LXT981 MII allows a MAC or PHY to directly connect into the repeater environment. The LXT981 maintains the same statistics for this 'Port' as it does for the other ports (except for illegal symbols). The LXT981 does *not* provide MDIO/MDC capability, as this is provided via the serial controller interface.

Mode control is provided via the PORT5_SEL pin (High = PHY Mode, Low = MAC Mode).

PHY Mode Operation

PHY Mode allows the LXT981 to interface to a 100 Mbps MAC. In PHY mode the LXT981 passes the full 56 bits of preamble through before sending the SFD.

MAC Mode Operation

MAC Mode allows the user to attach an additional PHY to the LXT981. In this mode the PHY provides both MII_TXCLK and MII_RXCLK. The MII_TXCLK must be frequency-locked to the 25 MHz oscillator used by the LXT981. The LXT981 does not provide an elasticity buffer to compensate for frequency differences. When operating in MAC mode, the LXT981 generates the full 56 bits of preamble before sending the SFD across the MII.

MII Port Timing Considerations

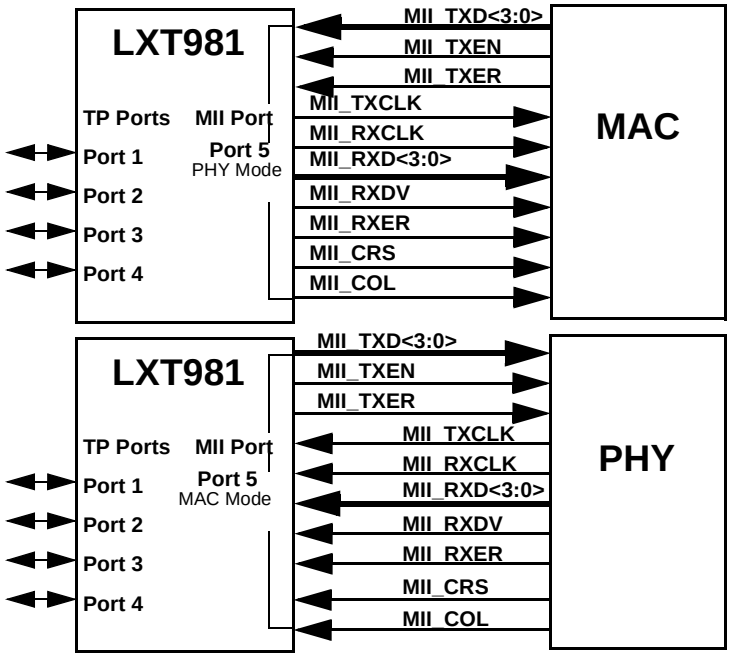
The IEEE 802.3u specification provides propagation delay constraints for standard PHY devices in Section 24.6, and for Repeater devices in Section 27. The LXT981 MII port is a hybrid that does not fit either of these categories. The critical consideration that applies to the LXT981 MII port is the overall end-to-end system propagation delay (132 Bit Times maximum). The LXT981 supports the intent of the Class II repeater application. Figure 8 summarizes the propagation delay issues relevant to the LXT981 MII port.

Figure 7: LXT981 MII (Port 5) Operation

The LXT981 MII port is reversible.

When PHY mode is selected, the LXT981 acts as the PHY side of the MII. In this mode an external MAC sends TX Data to the LXT981 to be repeated to the network. The LXT981 repeats network data to the MAC via the RX Data lines.

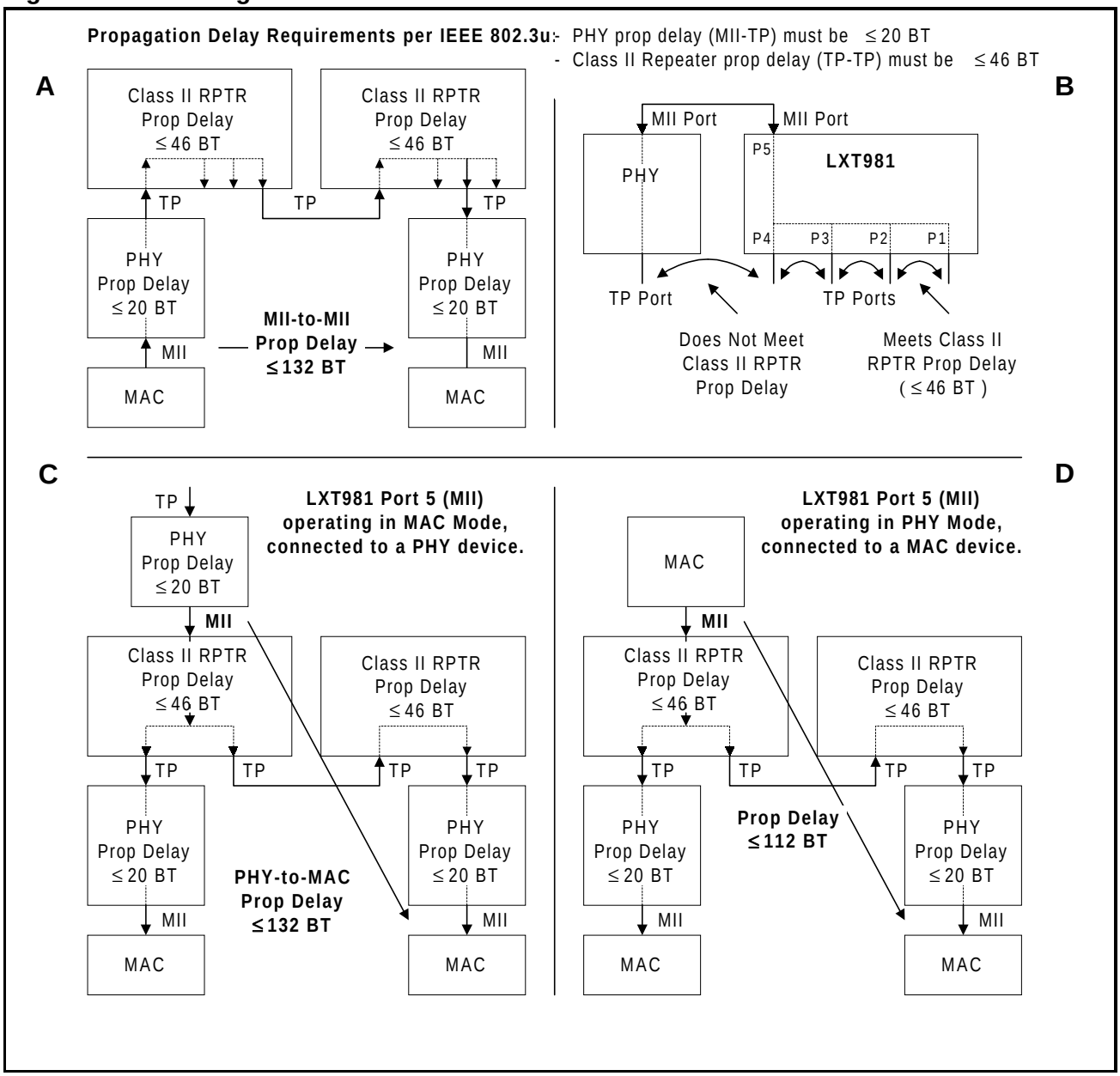
When MAC mode is selected, the LXT981 acts as the MAC side of the MII. In this mode the LXT981 repeats network data to the PHY via the TX Data lines.
The external PHY sends data to the LXT981 to be repeated to the



The LXT981 architecture treats the MII port as a fifth repeater port. The timing delay (latency) from the MII port to any other port meets the requirements for a Class II repeater (≤ 46 BT). It does not meet the requirements for a standard MII-PHY interface (20 - 24 BT). When operating in MAC mode with a PHY connected to the LXT981 MII port (Figure 8B), the fifth TP port does not have the latency characteristics of a Class II repeater with respect to the other ports.

With a MAC connected to the LXT981 MII port (Figure 8D), the maximum latency to any other MAC is 112 BT (not including cable delay). The MAC connected to the LXT981 has an advantage relative to other MACs because it has one less transceiver delay.

Figure 8: MII Timing Issues

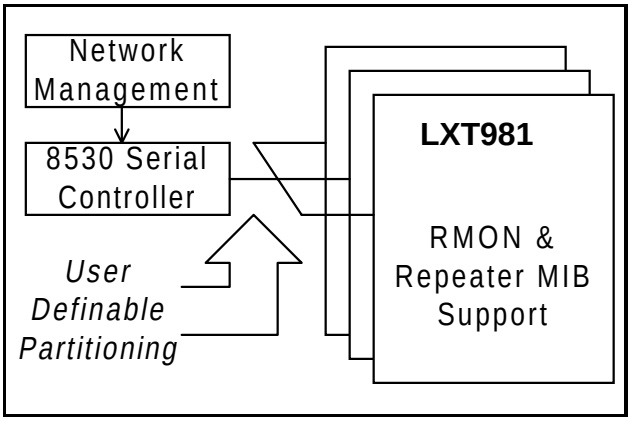


Serial Management I/F

The Serial Management Interface (SMI) provides access to repeater MIB variables, RMON Statistics attributes and status and control information. A network manager can access the interface through a simple serial communications controller. The interface is designed to be used in a multi-drop configuration, allowing multiple LXT981 devices to be managed from one common line.

The interface consists of a data input line (SRX), data output line (STX), and a clock (SERCLK), and can operate up to 2 Mbps. The interface operates on a simple command response model, with the network manager as the master and the LXT981 devices as slaves. Figure 9 is a simplified view of typical SMI architecture. Refer to Figure 20 on page 41 for circuit details.

Figure 9: Typical SMI Architecture



Serial Clock

SERCLK is a bidirectional pin; direction control is provided by the RECONFIG input. If RECONFIG is High, the LXT981 will drive SERCLK at 625 kHz. If RECONFIG is Low, SERCLK is an input, between 0 and 2 MHz. There is no lower bound to how slow the interface can operate. The clock can be stopped after each operation, as long as an idle (10 ones in a row) is transmitted first.

Serial Data I/O

The serial data pins, SRX and STX, should be tied together. The SRX input is compared with the STX output. If a mismatch occurs, STX goes to a high impedance. STX is driven on the falling edge of SERCLK. SRX is sampled on the rising edge. Refer to Test Specifications (Figure 33 on page 56) for timing information.

Read and Write Operations

Normally the network manager directs read and write operations to a specific LXT981 device using a two-part address consisting of HubID and ChipID. The interface allows up to 127 32-bit registers to be read at one time. Up to two registers can be written at a time.

Some registers may be automatically cleared when subsequent write operations are performed on other registers. Refer to the “Auto-Clearing Registers” section, which follows on page 28

Management Frame Format

The SMI uses a simple frame format, which is shown in Figure 10. Table 17 describes the individual fields. Table 18 shows how the bits for the header field would be stored in memory, assuming that they are transmitted LSB to MSB, low address to high address. Table 19 lists the command set and Table 20 provides a variety of typical packets.

All frames begin and end with a flag of consisting of “01111110”. All fields are transmitted LSB first. Zero-bit stuffing is required if more than five 1s in a row appear in the header, data or CRC fields. In addition, all operations directed to the device must be followed by an idle (ten 1s in a row), and the first operation must be preceded with an idle.

NOTE

The LXT981 uses the CCITT method of CRC (X16 + X12 + X5 +1).

Auto-Clearing Registers

Two registers, the Interrupt Status Register, see Table 57 on page 66 and the Search Port Match Register, see Table 47 on page 62, exhibit an "Auto Clearing" feature.

How Auto Clearing Works

Before executing any write command, the device first reads the most recently accessed register. If the accessed register was an auto-clearing register and set to Auto-Clear Mode, it will be read and cleared.

Example: A read or write command is performed on the Interrupt Status Register. Next, a write command is performed on Port Status Register. The write command to the Port Status Register causes an internal read of the Interrupt Status Register. If the Interrupt Status Register was set to Auto-Clear Mode, it will be read and cleared—as a result of the write command to the Port Status Register. Because the read and clear is internal (and automatic), the user may not be aware that all data in register 1 is now lost.

NOTE

The Auto-Clear behavior of the Interrupt Status Register and the Search Port Match Register is determined by the auto-clear bit in the Repeater Configuration Register, see Table 63 on page 70.

Preserving Auto-Clearing Register Data

To preserve auto-clearing data in either the interrupt status register or the Search Port Match Register, always follow any read or write commands to these registers with a read command to a register that does not auto clear. In other words, do not leave the read pointer on an auto-clearing register.

Example: If you read the interrupt status register (address: 0AE), immediately follow with a "dummy" read of the port link status register (address: 098). This dummy read moves the pointer, ensuring that the information in the interrupt status register is not inadvertently lost through auto clearing. After the "dummy" read, you are now free to go perform any read or write operation without fear of losing data in the auto clearing registers.

NOTE:

There is nothing inherently special about using one particular register for the "dummy" read instead of another. Using the port link status register (in the preceding example) is only a suggestion; a read command to any other register that is not auto-clearing is also acceptable.

Table 17: SMI Message Fields

Message	Description
Start or Stop Flag	"01111110". Protocol requires zero insertion after any five consecutive "1s" in the data stream.
Hub ID	Identifies board or sub-system. Assigned by one of two arbitration mechanisms at power-up.
Chip ID	Identifies one of eight LXT devices on a board or sub-system. Assigned by 3 external pins on each device.
Command	Identifies the particular operation being performed (see Table 19)
Length	Specifies number of registers to be transferred (1 to 127). Maximum is 2 per write, 127 per read.
Address	Specifies address of register or register block to be transferred.

Interrupt Functions

The LXT981 provides a single open-collector pin for external interrupt signalling. Seven different interrupt conditions may be reported. The Interrupt Status Register identifies the specific interrupt condition (refer to Table 59). The Interrupt Mask Register allows specific interrupts to be masked. Interrupts may be cleared in two ways, depending on the status of bit 11 in the Repeater Configuration Register (refer to Table 64 on page 70).

Figure 10: Serial Management Frame Format

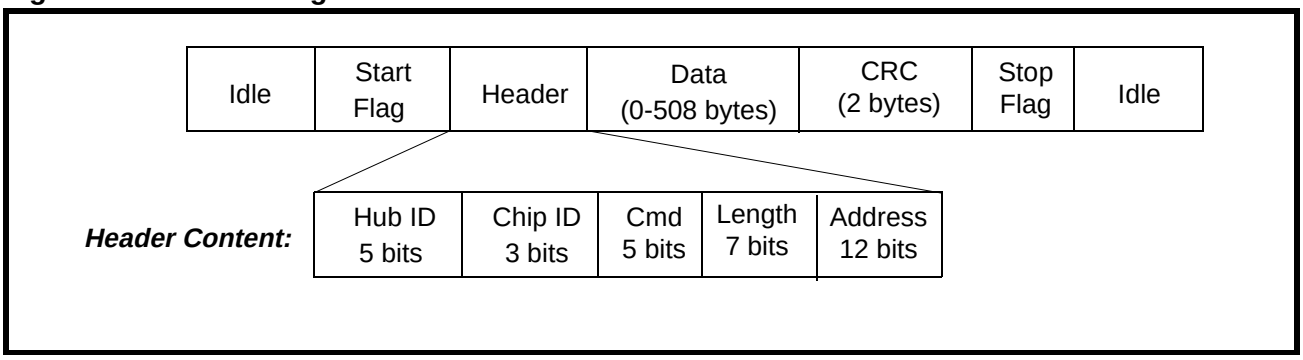


Table 18: Serial Management Header Storage

	MSB							LSB
Increasing Address ↑	Addr 11	Addr 10	Addr 9	Addr 8	Addr 7	Addr 6	Addr 5	Addr 4
	Addr 3	Addr 2	Addr 1	Addr 0	Length 6	Length 5	Length 4	Length 3
	Length 2	Length 1	Length 0	CMD 4	Cmd 3	Cmd 2	Cmd 1	Cmd 0
	ChipID 2	ChipID 1	ChipID 0	HubID 4	HubID 3	HubID 2	HubID 1	HubID 0

Table 19: Serial Management Interface Command Set

Command Value	Name	Usage	Normally Sent By	Description
18 (Hex)	Write	Normal Ops	Network Mgr	Used to write up to 2 registers (8 bytes) at a time.
04 (Hex)	Read	Normal Ops	Network Mgr	Used to read up to 127 registers at a time.
08 (Hex)	Request ID	Arbitration	LXT981	Requests Hub ID. Repeated periodically.
00 (Hex)	ConfigChg	Arbitration	LXT981	Notifies system of configuration change (hot swap). Requests new arbitration phase.
10 (Hex)	Re-arbitrate	Arbitration	Network Mgr	Re-starts arbitration.
14 (Hex)	Assign HubID	Arbitration Mech. 2	Network Mgr	Assigns Hub ID to device with ARBIN=0 and ARBOUT = 1 (top of chain).
0C (Hex)	Set Arbout to 1	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 1.
1C (Hex)	Set Arbout to 0	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 0.
02 (Hex)	DevID	Config	Network Mgr	Asks device to send contents of Device Revision Register.

Table 20: Typical Serial Management Packets

Message	Contents of Fields in Serial Management Packet					
	Hub ID	Chip ID	Command	Length	Address	Data
Write [1, 2]	User defined	User defined	18 Hex	01 or 02 Hex	User defined	User defined
Read Request [1, 3]	User defined	User defined	04 Hex	01 to 7F Hex	User defined	Null
Read Response [3]	00000	000	04 Hex	01 to 7F Hex	User defined	Data values
Assign Hub ID (Arb Method 1)	11111	111	18 Hex	02 Hex	188 Hex	Formatted per Table 69 on page 72
Assign Hub ID (Arb Method 2)	11111	111	14 Hex	01 Hex	000 Hex	Hub ID (LSB) and 27 “Os”
Set Arbout to 0	User defined	User defined	1C Hex	00 Hex	000 Hex	Null
Set Arbout to 1	User defined	User defined	0C Hex	00 Hex	000 Hex	Null
Arb Request	00000	000	08 Hex	02 Hex	190 Hex	PROM ID
Resend Arbitration	11111	111	10 Hex	00 Hex	000 Hex	Null
Resend Arbitration Response	00000	000	08 Hex	02 Hex	190 Hex	EEPROM ID
Device type/ Revision code	User defined	User defined	02 Hex	01 Hex	000 Hex	Null
Device/Revision Response	00000	000	02 Hex	01 Hex	0AD Hex	Device type/ revision

1. Other than checking that the top 3 bits of the address equals 000, the LXT981 does not check if the user writes or reads past the highest location in the data sheet. There are no adverse effects for writing or reading locations above the specified range.
2. If the user performs a write operation of length 1 or 2 and does not send a data field, the LXT981 will write junk into the specified registers. This constitutes an invalid command.
3. If the user reads past the highest location of the LXT981, all those locations will read back 0s. If a read operation is performed with a length of 0, the LXT981 will not respond.

Address Arbitration

Each device has a two part address, consisting of a Hub ID and a Chip ID. The Chip ID is assigned by the input pins CHIPID<2:0>. The manager assigns the Hub ID, and each LXT981 within a particular box will have the same Hub ID. The Hub ID is assigned through one of two arbitration mechanisms as shown in Figure 11.

EPROM Arbitration Mechanism

This mechanism requires one serial EPROM with a unique 48-bit ID on each board. This ID can consist of serial number, date/week/year of manufacture, etc. The ARBSELECT pin must be pulled Low. At power-up, the device with ChipID = 0 reads a 48-bit ID from the PROM. All other devices on the board listen in and record this ID. The device with ChipID = 0 then transmits Arbitration Request messages on the Serial Management Interface (SMI) every 2-3 ms. The request messages from the two boards may collide; if this happens a resolution scheme ensures that only one message will be transmitted.

The network manager must respond to each request with a message that includes the 48-bit ID and the Hub ID. All devices hear this message, but only those that match the 48-bit ID receive the Hub ID as their own. Once a Hub ID has been assigned to a hub, that hub will cease requesting a Hub ID. This process continues until all Hubs have been assigned an ID. Should a board power off and back on, the hub will re-request an ID, which the manager can then give out. The command types have been assigned so that an address

arbitration packet will always win out over normal requests.

Chain Arbitration Mechanism

When constructing the stack, the designer should create a daisy chain by tying the ARBOUT pin of each LXT981 to the ARBIN pin of the following LXT981. The manager is at the top of the stack and has control of the ARBIN for the first LXT981. The manager progressively assigns hub IDs using the "Assign Address" and "Set ARBOUT to ZERO" commands. The manager will initially set its ARBOUT (first LXT981's ARBIN) to zero. Since the assign address command only works on the LXT981 that has an ARBIN of 0 and an ARBOUT of 1, the first LXT981 can be assigned an address. After the first LXT981 has been assigned an address, it can uniquely be told to switch its ARBOUT to zero. This creates the (01) condition on the next LXT981 in the line. This LXT981 is then assigned an address and the process continues until all chips have been assigned a unique address. The manager can verify that a Hub is still present by performing DEVICE ID commands. If a change of configuration is detected, the manager can perform a broadcast write to return each hub's ARBOUT to 1, and then re-perform the address assignment process.

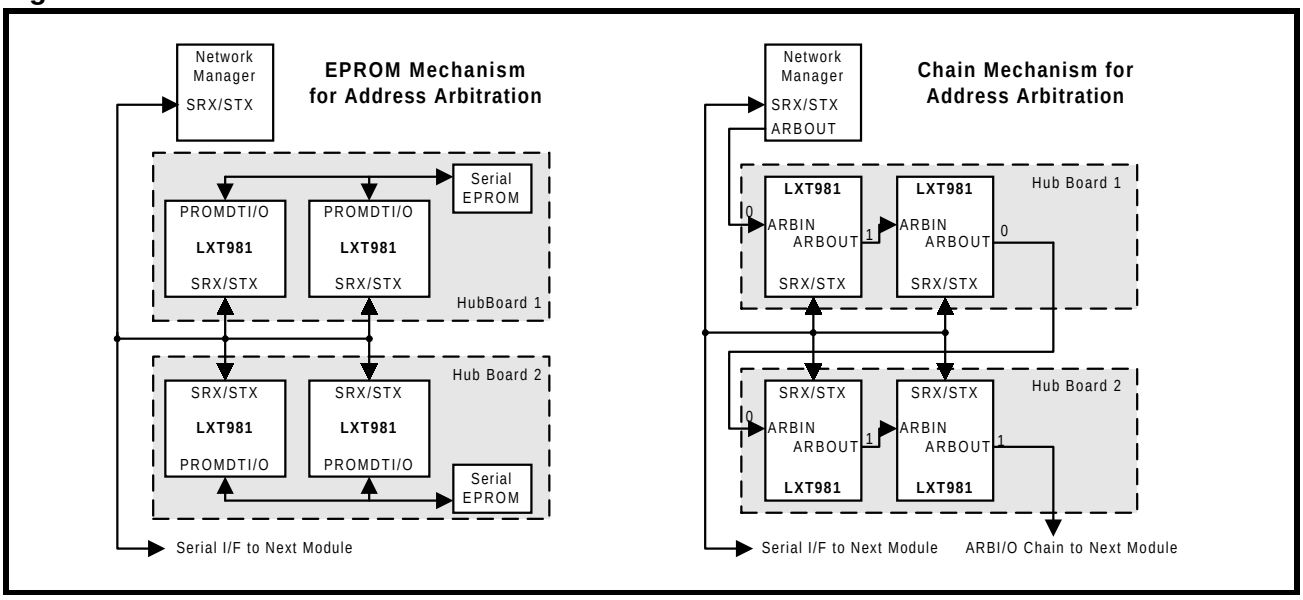
When using the chain arbitration method, set up the daisy chain so that the device with ChipID = 0 is the first device on the board that the chain passes through. Tie to ARBOUT of the SCC or to previous hub in the daisy chain. The first hub ARBIN can also be grounded. When assigning IDs, the first chain bit, located in the Device Revision Register (refer to Table 65) can then be used to determine when a new board has been encountered.

Address Re-Arbitration

Two mechanisms for address re-arbitration following a configuration change, such as a hot-swap of a board:

- Manual Re-arbitration - If the LXT981 detects a Low-to-High transition on RECONFIG, or if RECONFIG is High at power-up, it sends out a "Configuration Change" message (all 0s) on the Serial Management Interface (SMI) that the network manager can use to detect that re-arbitration is required. This message will be sent regardless of which arbitration mechanism is selected; however, in "Chain" Arbitration it will be sent once, but can be ignored.
- Network Manager. The network manager can detect or re-start arbitration at any time by sending the "Re-arbitrate" command.

Figure 11: Address Arbitration Mechanisms



Serial EEPROM Interface

The serial EEPROM interface has been designed to allow the vendor to load in optional information unique to each board. Items such as serial number and date of manufacture. can be placed in the serial EEPROM which is also used in the address arbitration process. Each board must contain a unique set of information. Additionally, only one serial EEPROM is required per board, they are not required per chip. The LXT981 reads in the first 48 bits (three 16-bit words) out of the EEPROM and stores them in a register. This read occurs only on power-up as this information is static. Only the LXT981 with a ChipID of 000 will drive the serial EEPROM control lines; all other LXT981s will listen in on the data and clock lines. The first bit to be shifted into the LXT981 from this interface would correspond to bit 47, while the last would be 0. The serial EEPROM shifts out the most significant bit (15) of the word first. Note that an auto incrementing EEPROM must be used.

Figure 12: Serial EEPROM Interface

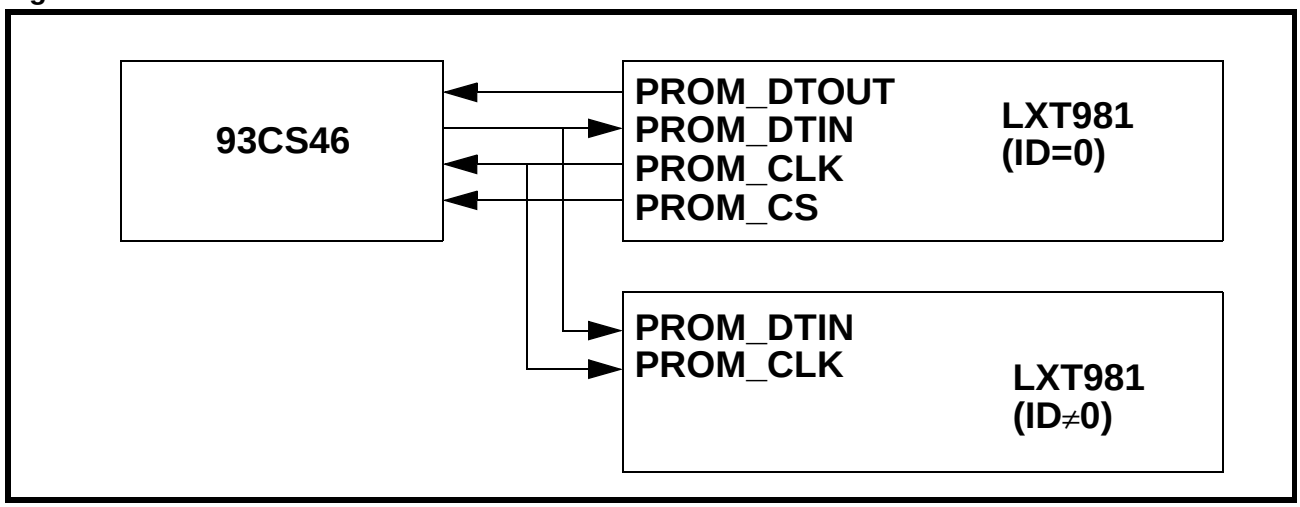
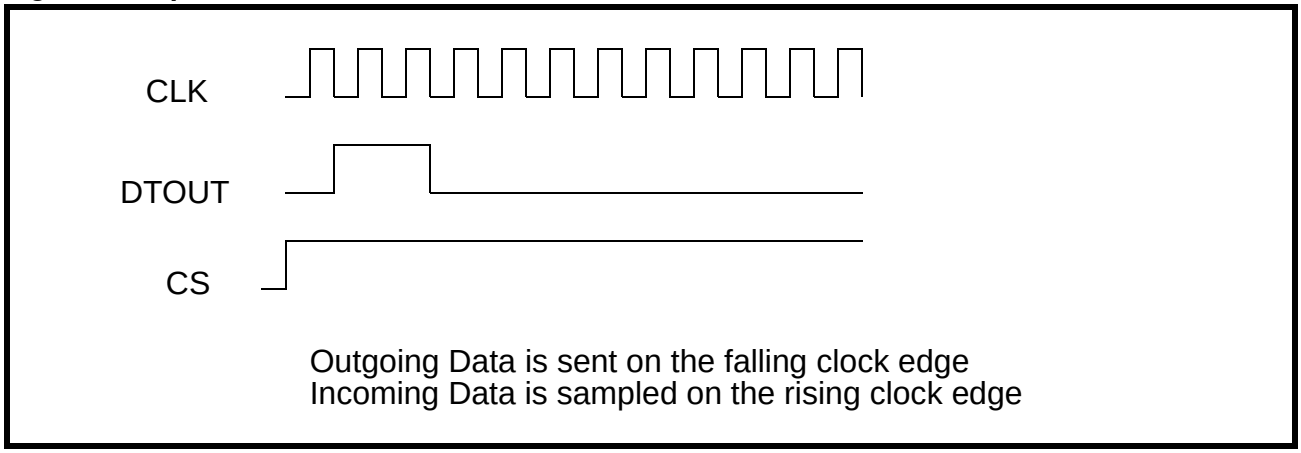


Figure 13: Optional R/W Serial EEPROM Interface



APPLICATION INFORMATION

Design Recommendations

The LXT981 has been designed to comply with IEEE requirements and to provide outstanding receive BER and long-line-length performance. Lab testing has shown that the LXT981 can perform well beyond the required distance of 100m. As with any finely crafted device, reaping the full benefits of the LXT981 requires attention to detail and good design practice.

General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT981 and the RJ45 connectors at the edge of the board.
- Do not extend any circuit power or ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having these problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (>32-bits) running at a high clock rate.
- DC-to-DC converters.

Many of these issues can be improved just by following good general design guidelines. In addition, Level One also recommends filtering between the power supply and the analog VCC pins of the LXT981. Filtering has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT981, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to divide the VCC plane into two sections. The digital section supplies power to the digital VCC pin and to the external components. The analog section supplies power to VCCH, VCCT, and VCCR pins of the LXT981. The break between the two planes should run under the device. In designs with more than one LXT981, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. The beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. Each LXT981 draws a maximum of 500 mA from the analog supply so beads rated at 750 mA should be used. A bulk cap (2.2 -10 µF) should be placed on each side of each ferrite bead to stop switching noise from traveling through the ferrite.

In addition, a high-frequency bypass cap (.01µf) should be placed near each analog VCC pin.

Ground Noise

The best approach to minimize ground noise is strict use of good general design guidelines and by filtering the VCC plane.

Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes. The following guidelines are recommended:

- Follow the guidelines in the *LXT980 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPOP/N and TPIP/N signals, away from the magnetics, and away from the RJ45 connectors.
- Place the layers so that the TPOP/N and TPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPOP and TPIP/N.

Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ45 connectors to the magnetics, and can be used to terminate unused signal pairs ('Bob Smith' termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2kV isolation to the Bob Smith termination.

MII Terminations

Series termination resistors are recommended on all MII signals driven by the LXT981. The proper value = nominal trace impedance minus 13Ω. If the nominal trace impedance is not known, use 55Ω.

The RBIAS Pin

The LXT981 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to ground. Surround the RBIAS trace with ground; do not run high-speed signals next to RBIAS.

The Twisted-Pair Interface

Because the LXT981 transmitter uses 2:1 magnetics, system designers must take extra precautions to minimize parasitic shunt capacitance in order to meet return loss specifications. These steps include:

- Use compensating inductor in the output stage (see Figure 19 on page 40).
- Place magnetics as close as possible to the LXT981.
- Keep transmit pair traces short.
- Do not route transmit pair adjacent to a ground plane. If possible, eliminate planes under the transmit traces completely. Otherwise, keep planes 3-4 layers away.
- Some magnetic vendors are producing magnetics with higher than average return loss performance. Use of these improved magnetics increases the return loss budget available to the system designer.
- Improve EMI performance by filtering the output centertap. A single ferrite bead may be used to supply centertap current to all four ports.

In addition, follow all the standard guidelines for a twisted-pair interface:

- Route the signal pairs differentially, close together. Allow nothing to come between them.
- Keep distances as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- If possible, place entire receive termination network on one side and transmit on the other.
- Keep termination circuits close together and on the same side of the board.
- Always put termination circuits close to the source end of any circuit.
- Bypass common-mode noise to ground on the in-board side of the magnetics using 0.01 µF capacitors.

The Fiber Interface

The fiber interface consists of a pseudo-ECL (PECL) transmit and receive pair to an external fiber optic transceiver. The transmit pair should be AC coupled to the transceiver, and biased to 3.7V with a 50Ω equivalent impedance. The receive pair can be DC-coupled, and should be biased to 3.0V with a 50Ω equivalent impedance. Figure 18 on page 39 shows the correct bias networks to achieve these requirements.

Magnetics Information

The LXT980 requires a 1:1 ratio for the receive transformers and a 2:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 21 for transformer specifications and *Magnetic Manufacturers for Networking Product Applications* (App. Note 73) for a reference list of compatible magnetic components. Before committing to a specific component, designers should test and validate the magnetics in the specific application to verify that system requirements are met.

Table 21: LXT980 Magnetics Specifications

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	2 : 1	–	–	
Insertion loss	0.0	–	1.1	dB	80 MHz
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	–	–	-40	dB	.1 to 60 MHz
	–	–	-35	dB	60 to 100 MHz
Return Loss - standard	–	–	-16	dB	30 MHz
	–	–	-10	dB	80 MHz
Return Loss - improved	–	–	-20	dB	30 MHz
	–	–	-15	dB	80 MHz

Typical Application Circuitry

Figures 14 through 16 are simplified block diagrams showing typical applications. Figures 17 through 22 show application circuitry details.

Figure 14: Managed Repeater Stack

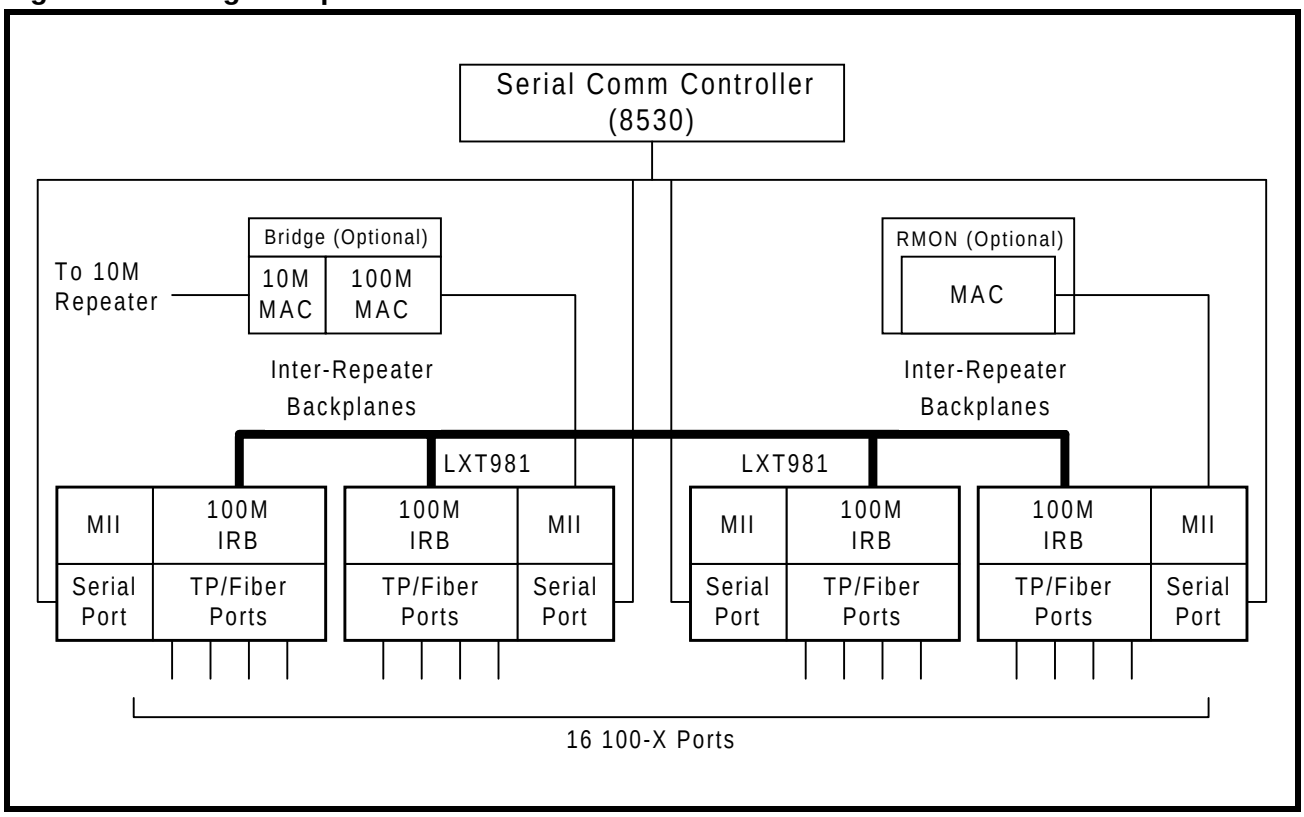


Figure 15: Unmanaged Repeater Stack

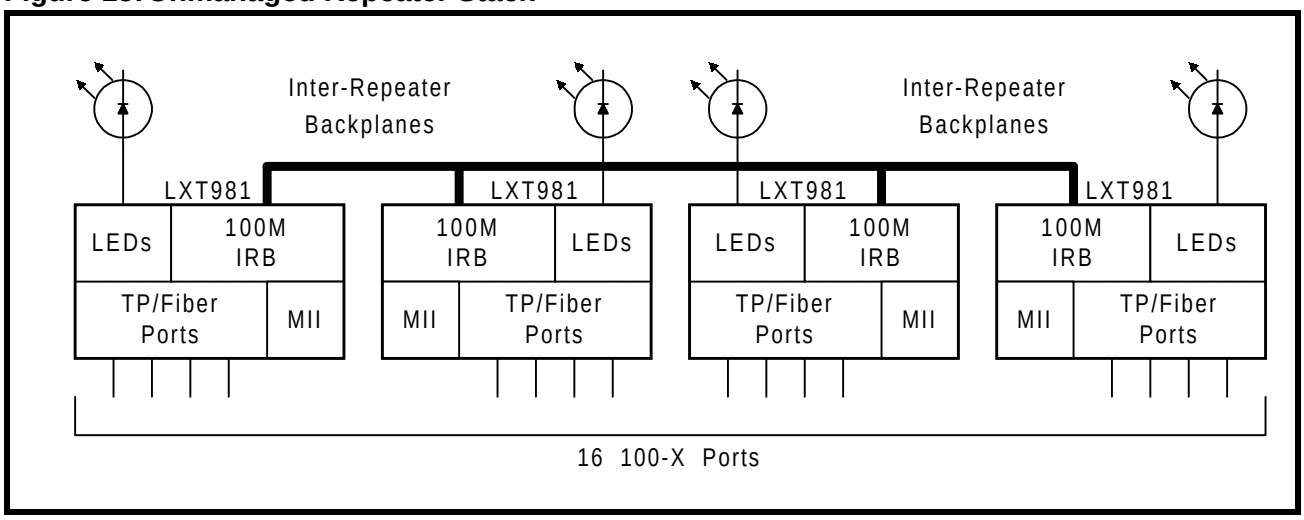


Figure 16: Hybrid Switch/Repeater Application

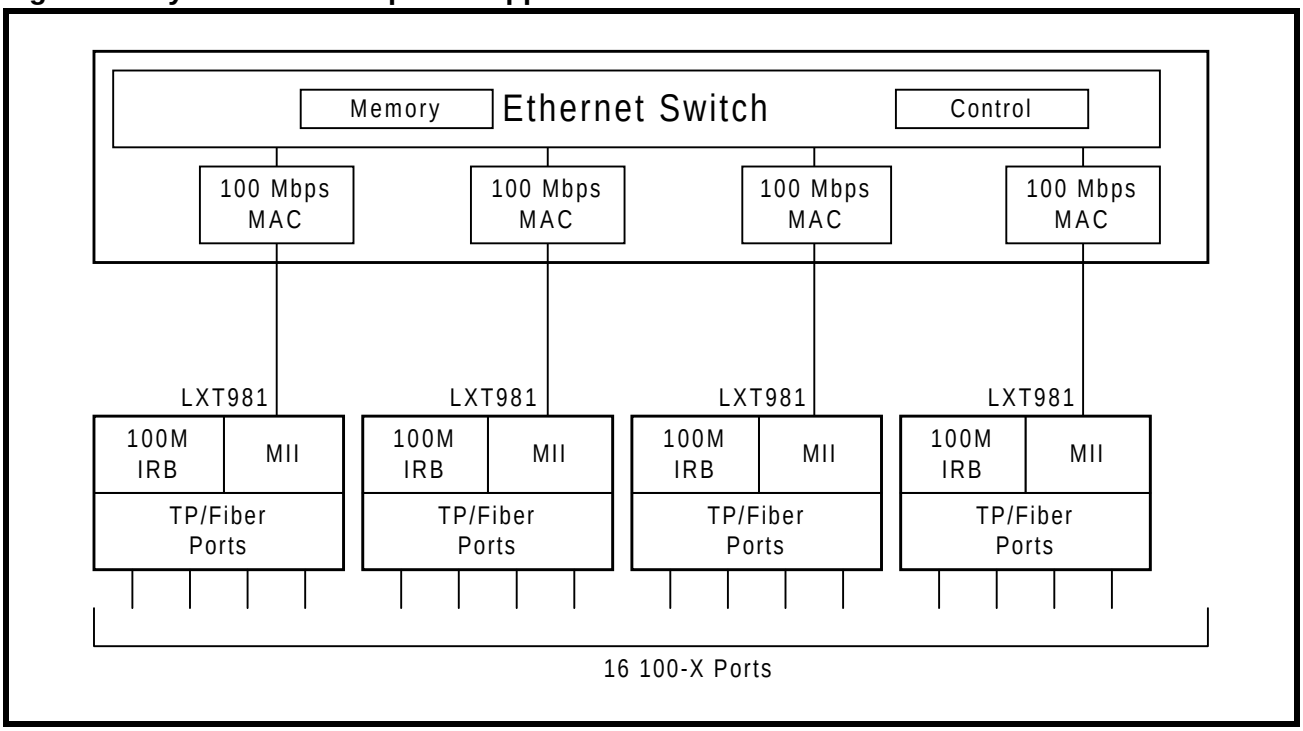


Figure 17: Power and Ground Connections

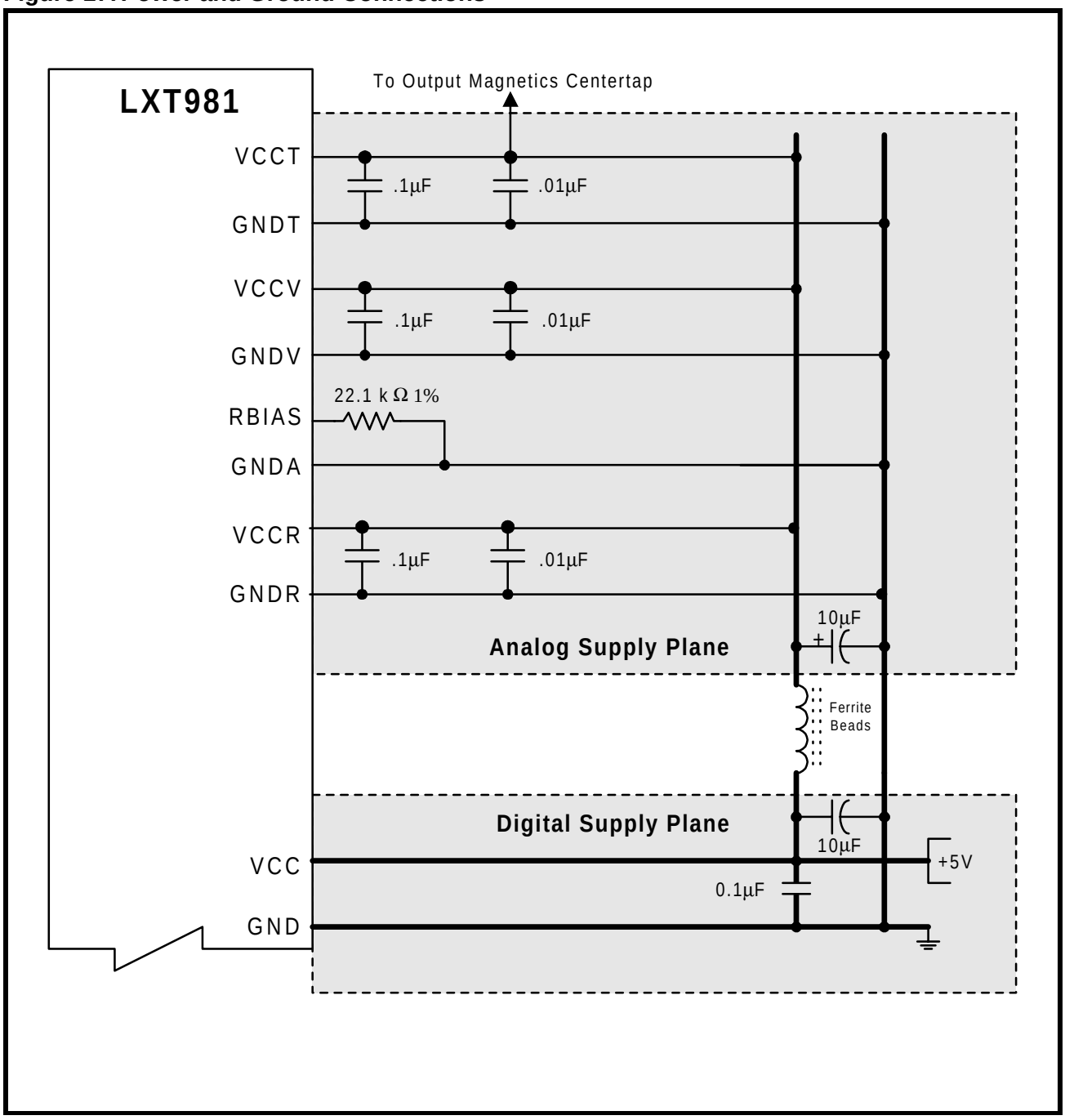
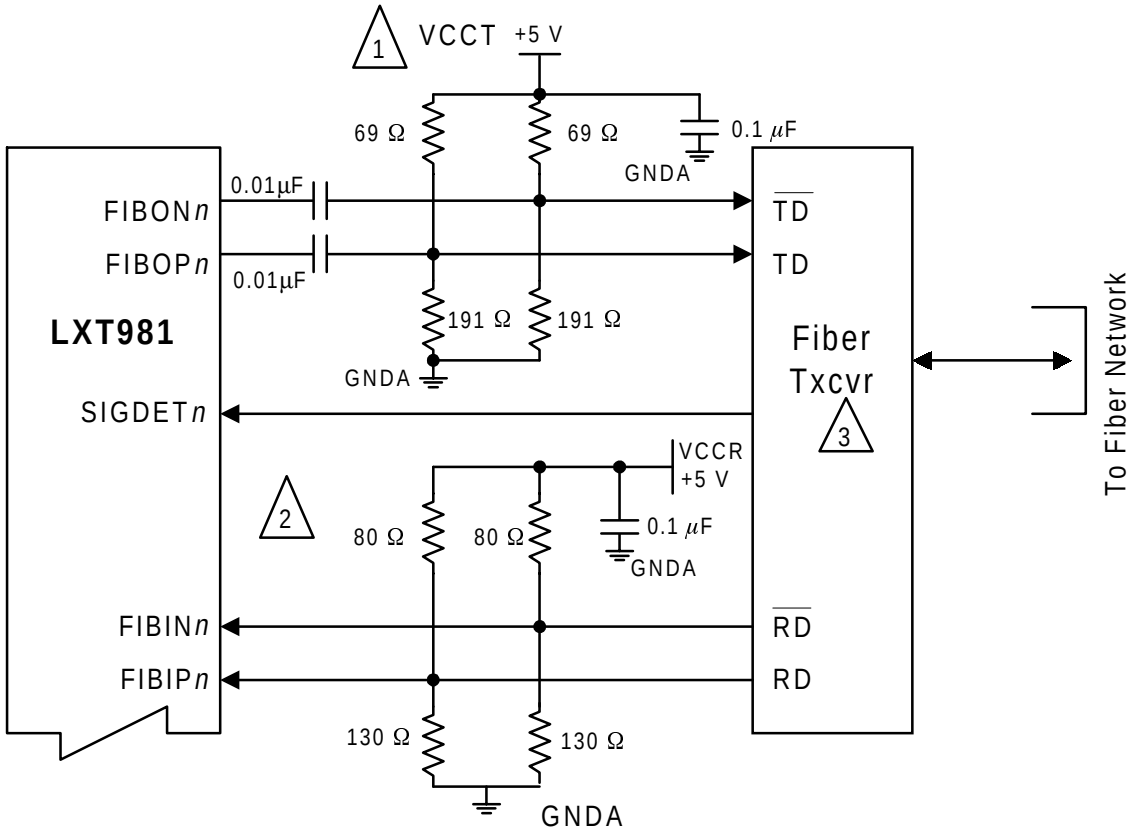


Figure 18: Typical Fiber Port Interface

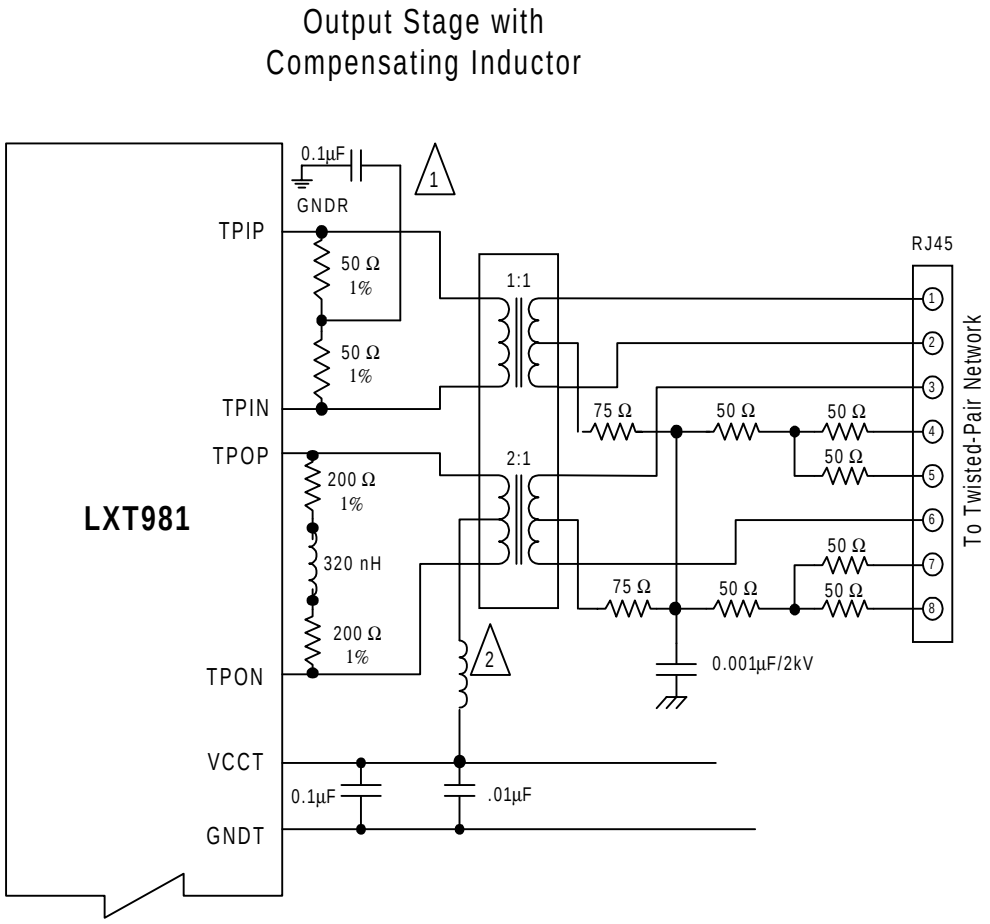


1. Suggested supply layout for fiber-only applications. In combination twisted-pair and fiber applications, use VCCD/GNDD.

2. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON, FIBOP and SIGDET may be left unconnected.

3. Refer to fiber transceiver manufacturers recommendations for termination circuitry.
Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.

Figure 19: Typical Twisted-Pair Port Interface



1. Receiver common mode bypass cap may improve BER performance in systems with noisy power supplies.
2. A single ferrite bead may be used to supply centertap current to all 4 ports.

Figure 20: Typical Serial Management Interface Connections

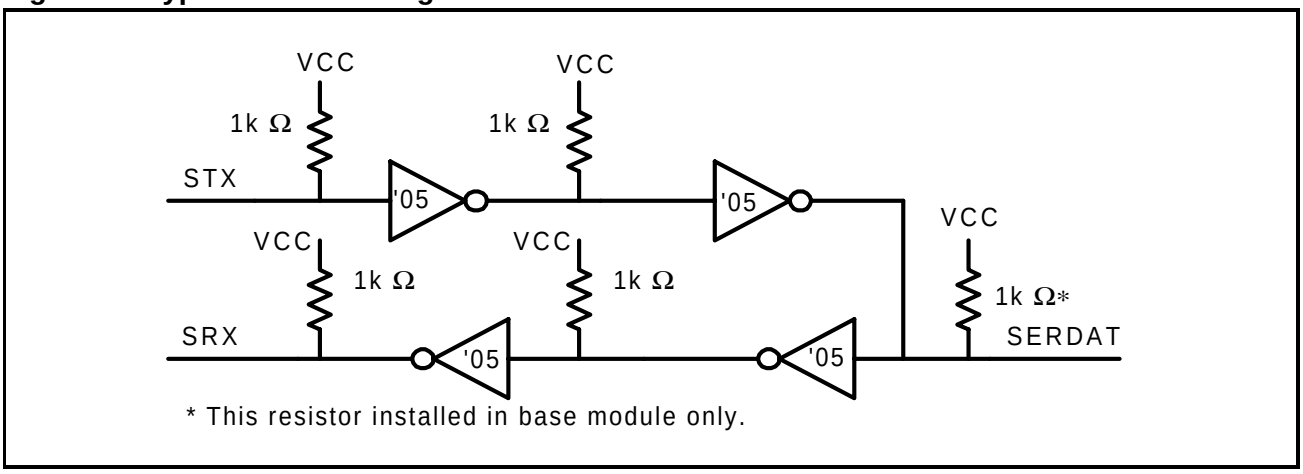


Figure 21: Typical IRB Implementation

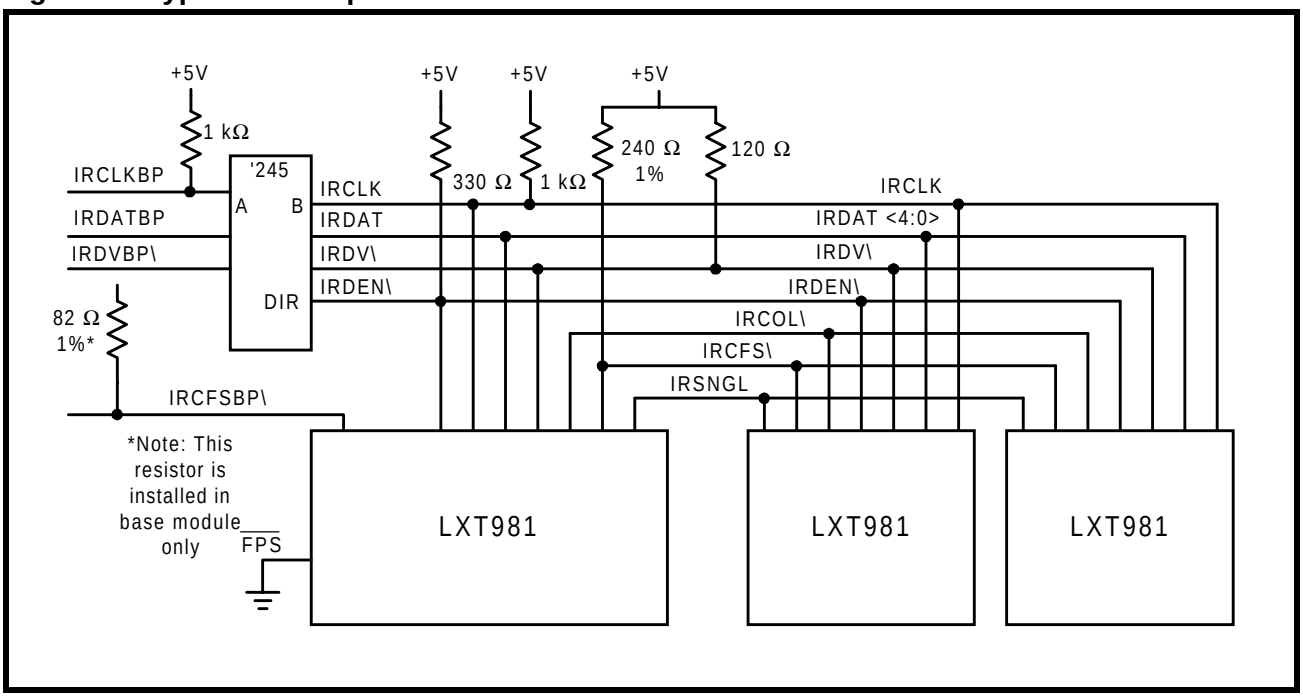
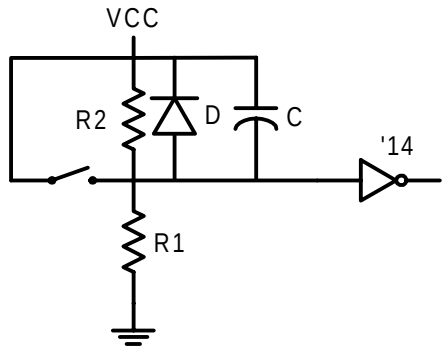


Figure 22: Typical Reset Circuit



t(CR1) > Power supply ramp up time.
R2 discharges C when supply goes away.
‘
14 needed for multiple LXT981 devices.

TEST SPECIFICATIONS

NOTE

Tables 22 through 40 and Figures 23 through 34 represent the performance specifications of the LXT981 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 24 through 40 are guaranteed over the recommended operating conditions specified in Table 23.

Table 22: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply voltage		V_{CC}	-0.3	6	V
Operating temperature	Ambient	T_{OPA}	-15	+80	ºC
	Case	T_{OPC}	–	+130	ºC
Storage temperature		T_{ST}	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 23: Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended supply voltage		V_{CC}	4.75	5.0	5.25	V
		V_{CCV}	4.75	5.0	5.25	V
		V_{CCR}	4.75	5.0	5.25	V
		V_{CCT}	4.75	5.0	5.25	V
Recommended operating temperature	Ambient	T_{OPA}	0	–	70	°C
	Case	T_{OPC}	0	–	115	°C
Power consumption	100BASE-TX, 4 ports active	P_C	–	–	3.5	W
	100BASE-FX, 4 ports active	P_C	–	–	3.0	W

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 24: Input Clock Requirements

Parameter[1]	Sym	Min	Typ[2]	Max	Units	Test Conditions
Frequency	–	–	25	–	MHz	–
Frequency Tolerance	–	–	–	±100	ppm	–
Duty Cycle	–	40	–	60	%	–

1. This table lists requirements which apply to the external clock supplied to the LXT981, not to LXT981 test specifications.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 25: I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	VIL	–	–	0.8	V	TTL inputs
		–	–	30	% VCC	CMOS inputs [2]
		–	–	1.0	V	Schmitt triggers [3]
Input High voltage	VIH	2.0	–	–	V	TTL inputs
		70	–	–	% VCC	CMOS inputs [2]
		VCC-1.0	–	–	V	Schmitt triggers [3]
Hysteresis voltage	–	1.0	–	–	V	Schmitt triggers [3]
Output Low voltage	VOL	–	–	0.4	V	IOL = 1.6 mA
Output Low voltage (LED)	VOLL	–	–	1.0	V	IOLL = 10 mA
Output High voltage	VOH	2.4	–	–	V	IOH = 40 µA
Input Low current	IIL	-100	–	–	µA	–
Input High current	IIH	–	–	100	µA	–
Output rise / fall time	–	–	3	10	ns	CLOAD = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Table 26 for IRB I/O characteristics.
3. Applies to RESET and CLK25 pins only.

Table 26: 100 Mbps IRB Electrical Characteristics

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage		VOL	–	.3	.7	V	RL = 330 Ω
Output rise or fall time		TF	–	4	10	ns	CL = 15 pF
Input High voltage		VIH	VCC - 2.0	–	–	V	CMOS inputs
Input Low voltage		VIL	–	–	2.0	V	CMOS inputs
$\overline{\text{IRCFS}}$ current	single drive	–	7.0	–	9.0	mA	RL = 240Ω
	collision	–	–	–	20.5	mA	RL = 240Ω
$\overline{\text{IRCFSBP}}$ current	single drive	–	20.0	–	25.0	mA	RL = 82Ω
	collision	–	–	–	55.0	mA	RL = 82Ω
$\overline{\text{IRCFS/BP}}$ voltage	single drive	–	3.4	–	4.35	V	–
	collision	–	1.4	–	1.9	V	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 27: 100BASE-TX Transceiver Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage (single ended)	VP	0.95	1.0	1.05	V	Note 2
Signal amplitude symmetry	–	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 16 ns pulse width at 50% of pulse peak,
Overshoot/Undershoot	VOS	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at line side of transformer, line replaced by 100Ω (± .1%) resistor.

Table 28: 100BASE-FX Transceiver Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	–	1.0	V	–
Signal rise/fall time	TRF	–	–	1.6	ns	10 <-> 90 %, 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	2.25	–	VCC - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 23: 100 Mbps Port-to-Port Delay Timing

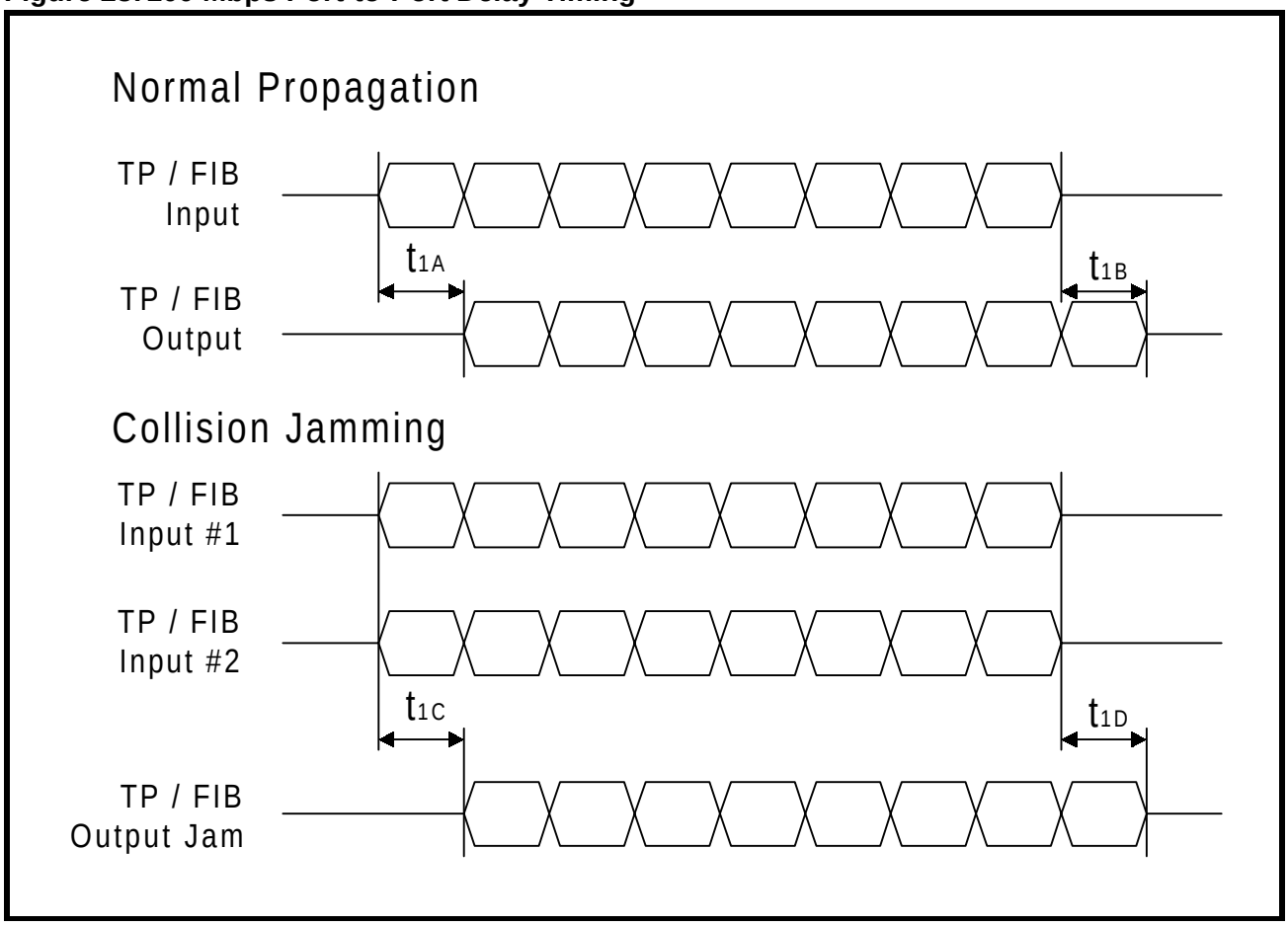


Table 29: 100 Mbps Port-to-Port Delay Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, start of transmission	t1A	–	–	46	BT	–
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, end of transmission	t1B	–	–	46	BT	–
TPIP/N or FIBIP/N collision to TPOP/N or FIBOP/N, start of jam	t1C	–	–	46	BT	–
TPIP/N or FIBIP/N idle to TPOP/N or FIBOP/N, end of jam	t1D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 24: 100BASE-TX Transmit Timing - PHY Mode MII

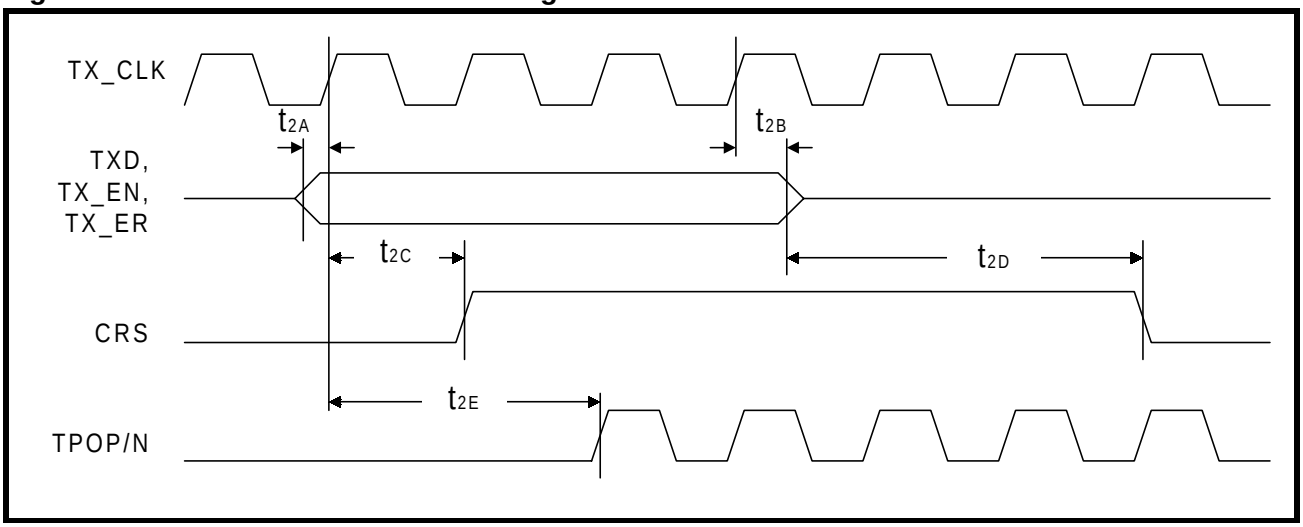


Table 30: 100BASE-TX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t2A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t2C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t2D	0	–	16	BT	–
TX_EN sampled to TPOP/N active (Tx latency)	t2E	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 25: 100BASE-TX Receive Timing - PHY Mode MII

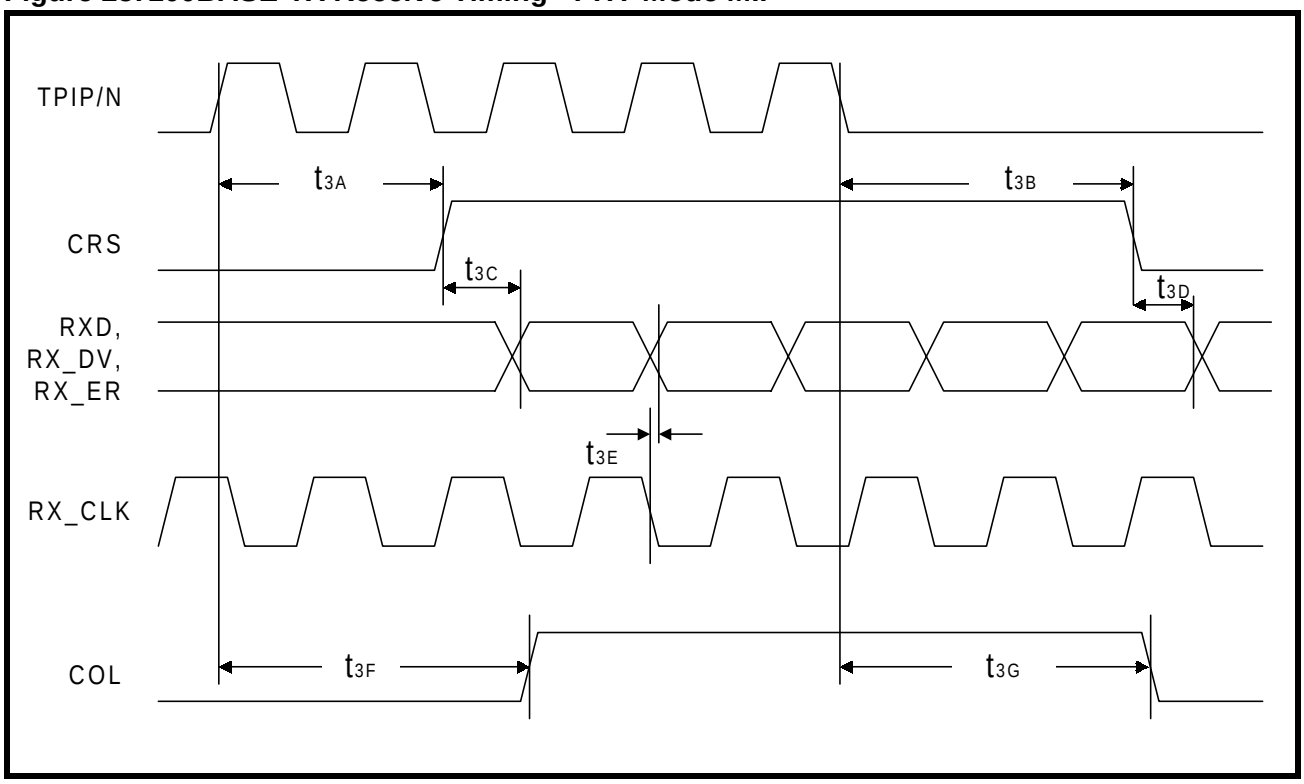


Table 31: 100BASE-TX Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to CRS asserted	t3A	–	–	46	BT	–
TPIP/N quiet to CRS de-asserted	t3B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t3C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t3D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t3E	–	–	10	ns	–
TPIP/N in to COL asserted	t3F	–	–	46	BT	–
TPIP/N quiet to COL de-asserted	t3G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 26: 100BASE-TX Transmit Timing - MAC Mode MII

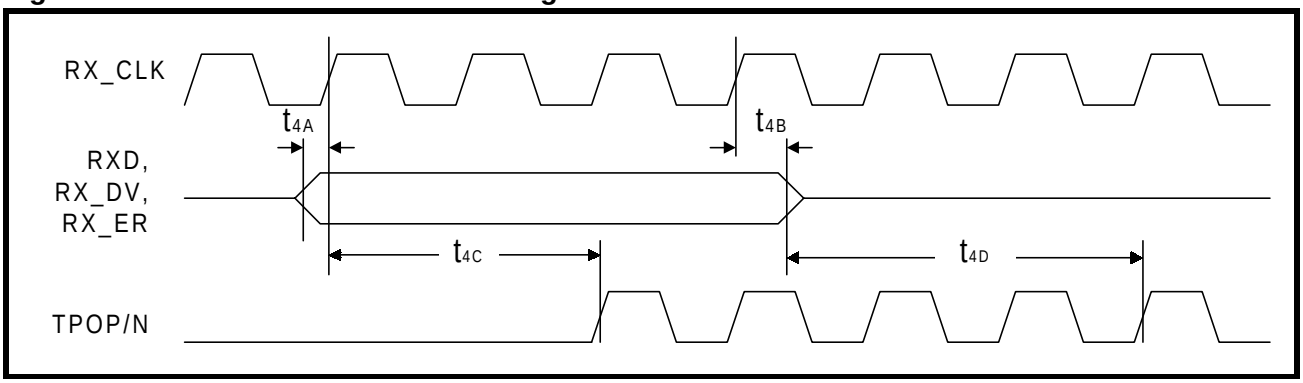


Table 32: 100BASE-TX Transmit Timing Parameters - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t4A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t4B	5	–	–	ns	–
RXD sampled to TPO asserted	t4C	–	–	46	BT	–
RXD sampled to TPO de-asserted	t4D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 27: 100BASE-TX Receive Timing - MAC Mode MII

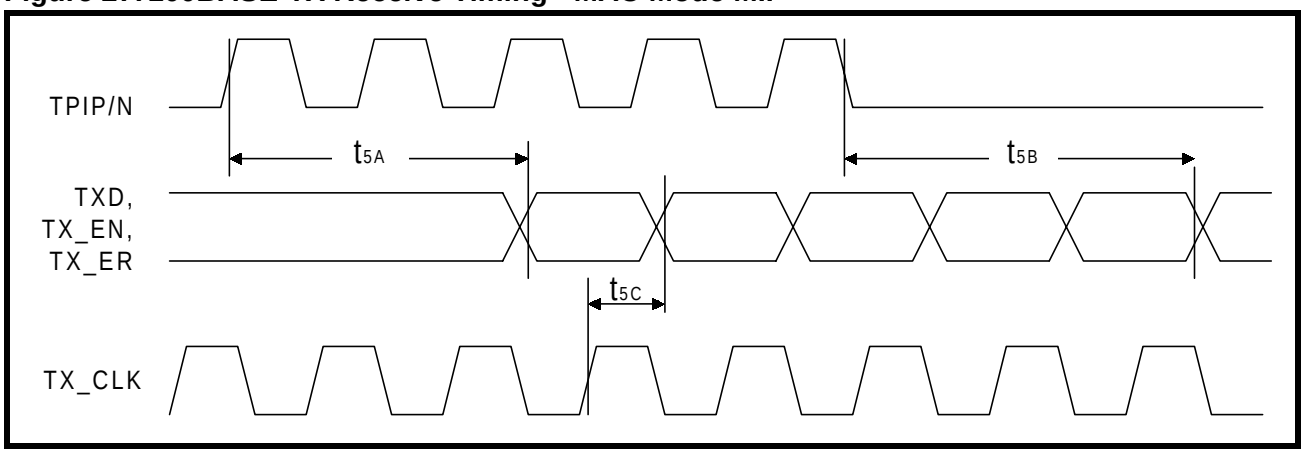


Table 33: 100BASE-TX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to TXD, TX_EN, TX_ER	t5A	–	–	46	BT	–
TPIP/N quiet to TXD de-asserted	t5B	13	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t5C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 28: 100BASE-FX Transmit Timing - PHY Mode MII

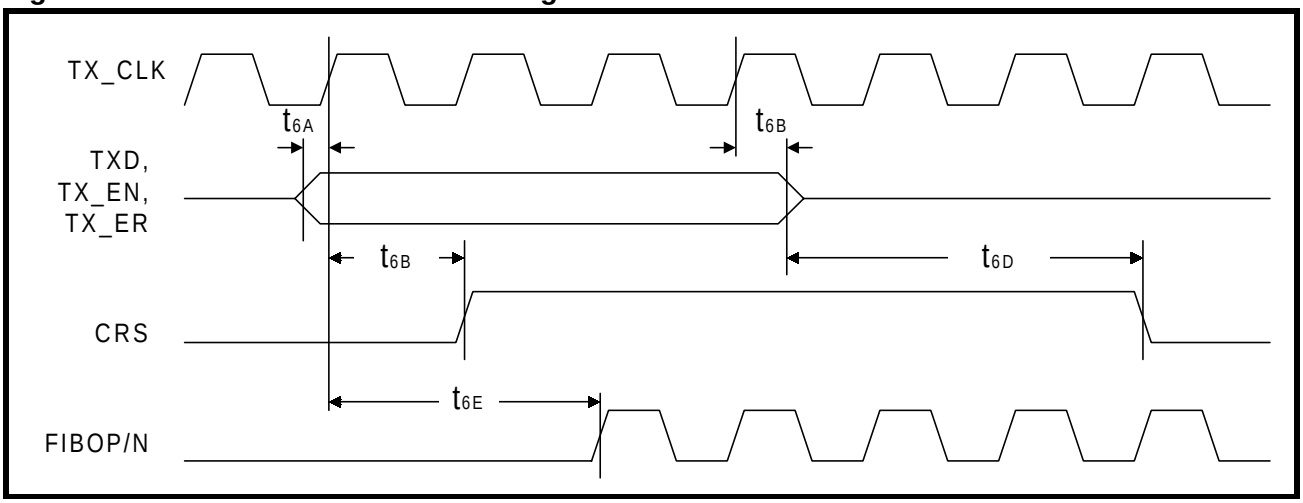


Table 34: 100BASE-FX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t6A	10		–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t6B	5		–	ns	–
TX_EN sampled to CRS asserted	t6C	0		4	BT	–
TX_EN sampled to CRS de-asserted	t6D	0		16	BT	–
TX_EN sampled to FIBOP/N out (Tx latency)	t6E	–		46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 29: 100BASE-FX Receive Timing - PHY Mode MII

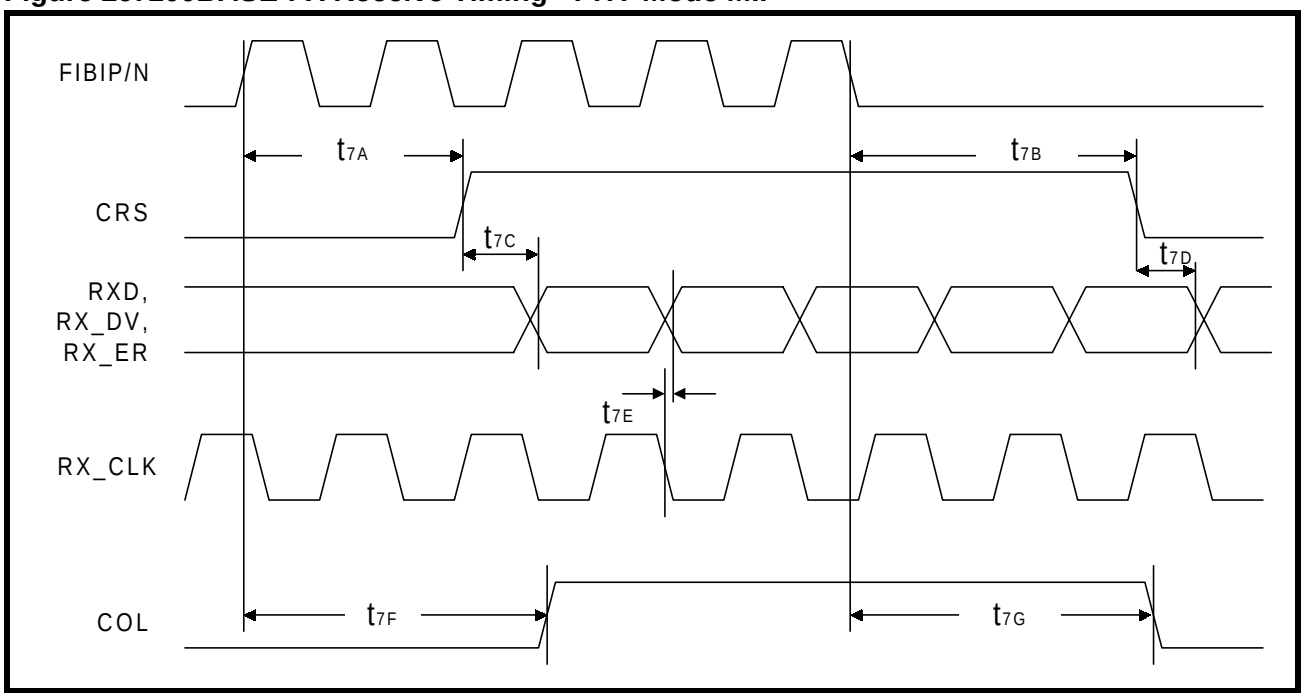


Table 35: 100BASE-FX Receive Timing - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
FIBIP/N in to CRS asserted	t7A	–	–	46	BT	–
FIBIP/N quiet to CRS de-asserted	t7B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t7C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t7D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t7E	–	–	10	ns	–
FIBIP/N in to COL asserted	t7F	–	–	46	BT	–
FIBIP/N quiet to COL de-asserted	t7G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 30: 100BASE-FX Transmit Timing - MAC Mode MII

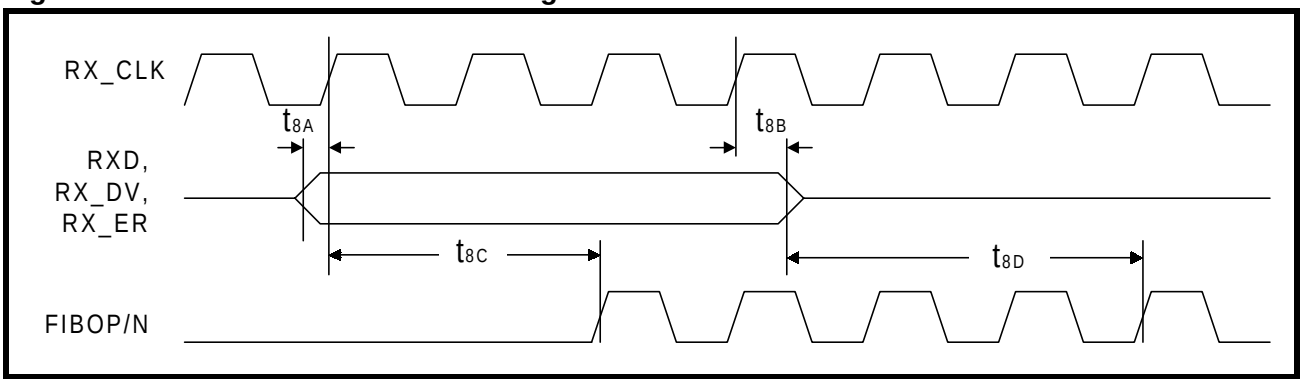


Table 36: 100BASE-FX Transmit Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t8A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t8B	5	–	–	ns	–
RXD sampled to FIBOP/N asserted	t8C	–	–	46	BT	–
RXD sampled to FIBOP/N de-asserted	t8D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 31: 100BASE-FX Receive Timing - MAC Mode MII

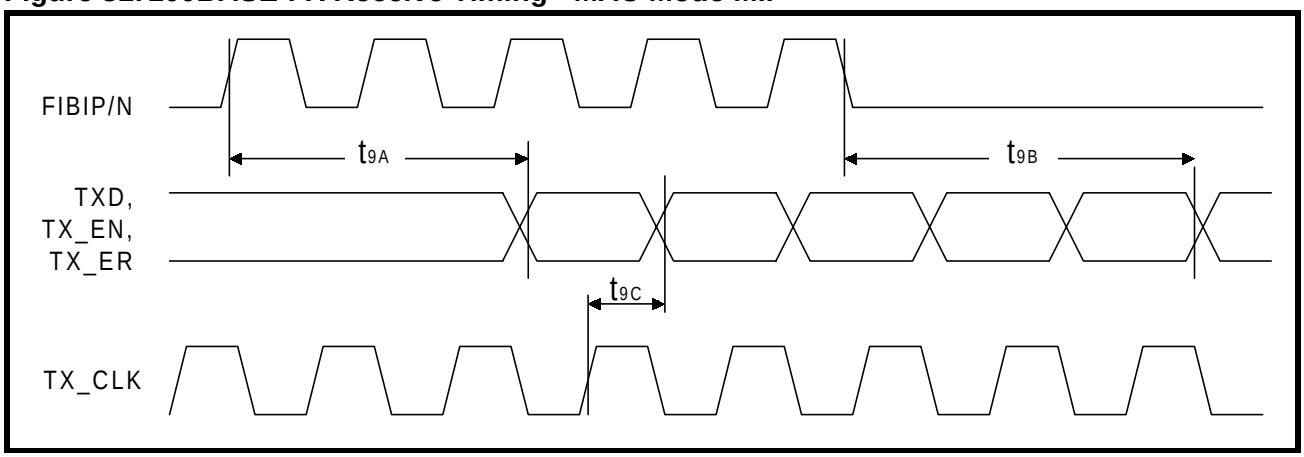


Table 37: 100BASE-FX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
FIBIP/N in to TXD, TX_EN, TX_ER	t9A	–	–	46	BT	–
FIBIP/N quiet to TXD de-asserted	t9B	–	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t9C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 32: 100 Mbps IRB Timing

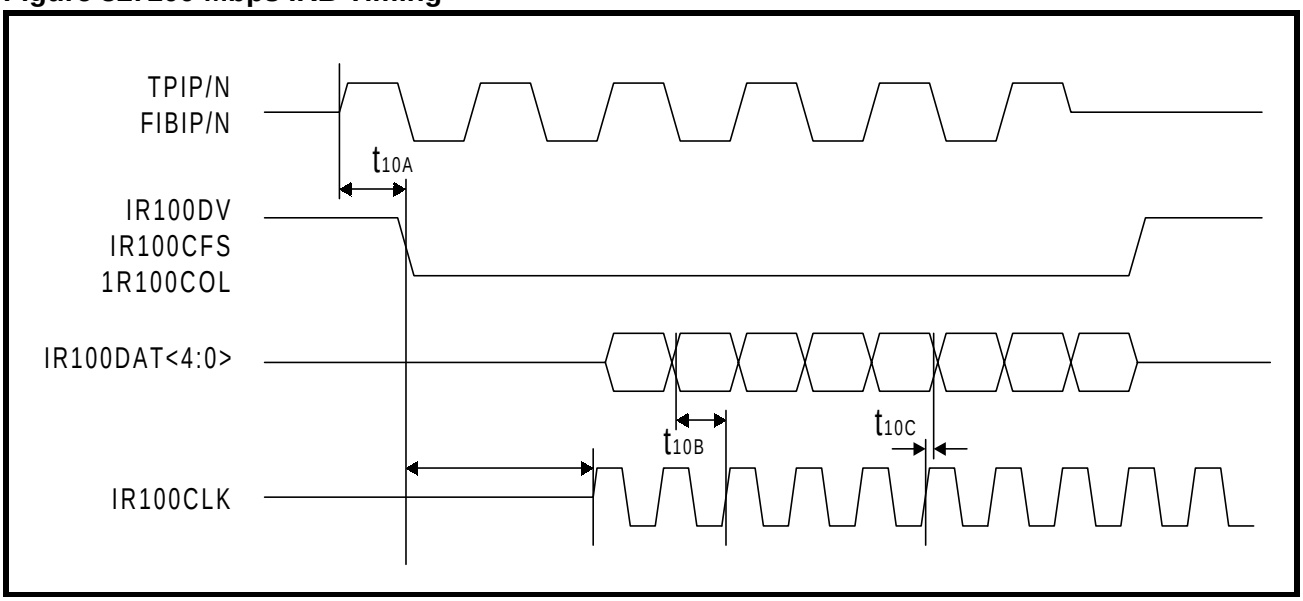


Table 38: 100 Mbps IRB Timing Parameters[1]

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBP/N to $\overline{\text{IR100DV}}$ Low	t10A	18	24	30	BT	–
IR100DAT to IR100CLK setup time	t10B	–	10	–	ns	–
IR100DAT to IR100CLK hold time	t10C	–	0	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and the reciprocal of the bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 33: Serial Management Interface Timing

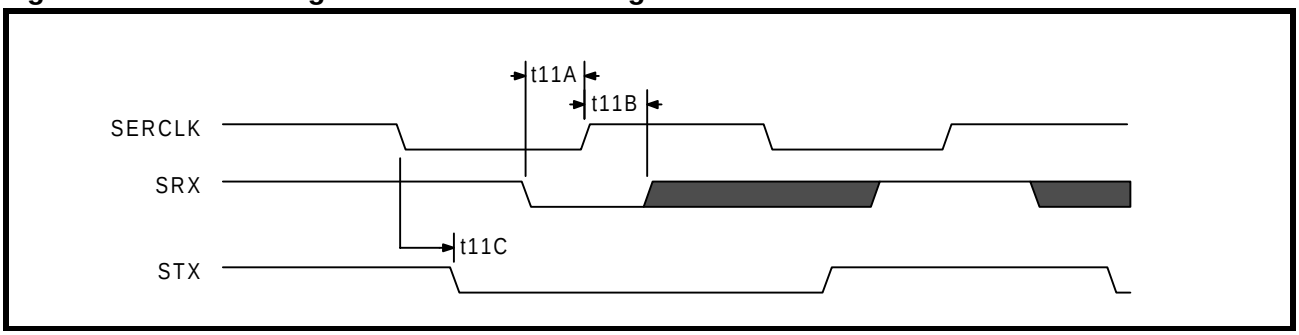


Table 39: Serial Interface Timing Characteristics [1] (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
SERCLK input frequency	–	–	-	2.0	MHz	Depending on RECONFIG, this is either an input or output.
SERCLK output frequency	–	–	625	–	kHz	
Data to clock setup time	t11A	0	–	–	ns	SRX valid to SERCLK rising edge.[2]
Clock to data hold time	t11B	200	–	–	ns	SERCLK rising edge to SRX change.[2]
Data propagation delay	t11C	–	–	200	ns	SERCLK falling edge to STX valid.[3]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. Output.

Figure 34: PROM I/F Timing

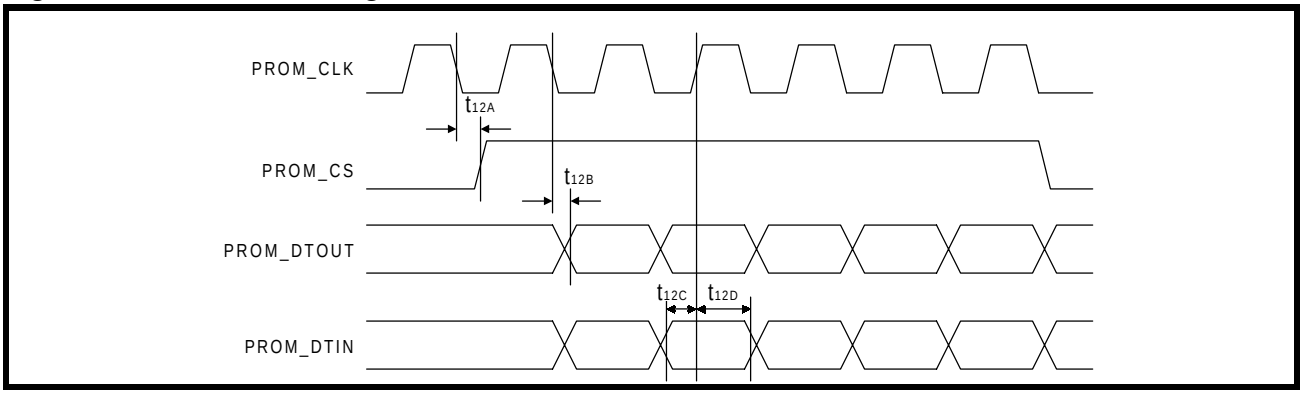


Table 40: PROM I/F Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
PROM_CLK	FPCLK	–	–	1.0	MHz	PROM_CLK frequency
CLK to PROM_CS delay	t12A	–	–	200	ns	CLK falling edge to PROM_CS
CLK to PROM_DTOUT delay	t12B	–	–	20	ns	CLK falling edge to PROM_DTOUT
PROM_DTIN to CLK setup time	t12C	20	–	–	ns	PROM_DTIN to CLK rising edge
PROM_DTIN to CLK hold time	t12D	20	–	–	ns	PROM_DTIN to CLK rising edge

REGISTER DEFINITIONS

The LXT981 register set is composed of multiple 32-bit registers of the types listed in Table 41. All register addresses are hexadecimal.

Table 41: Register Set

Base Address[1]	Register Type	Bit Assignments
00X	Port 1 Counters (TP/FX)	Refer to Tables 42 and 43.
01X	Port 2 Counters (TP/FX)	
02X	Port 3 Counters (TP/FX)	
03X	Port 4 Counters (TP/FX)	
04X	Port 5 Counters (MII)	
05X	Additional Port Error and Isolate Counters	Refer to Tables 42 and 43.
05X, 06X	RMON Counters	Refer to Tables 42 and 44.
07X	Port Addresses	Refer to Tables 45 and 46.
08X	Authorized Addresses	Refer to Table 45.
08X, 09X	Global Addresses	Refer to Tables 45 and 47.
09X	Port Control	Refer to Tables 48 through 49.
09X	Port Status	Refer to Tables 48 and 50.
09X, 0AX, 0BX, 188, 189, 190, 191	General Setup/Status	Refer to Tables 51 through 61 and 62 through 70.

1. X = Offset address of register desired. Note that base register addresses for port counters are offset by 1 (00x refers to Port 1, 01X to Port 2, 02X to Port 3, 03X to Port 4 and 04X to Port 5).

Counter Registers

Table 42 shows bit assignments. When reading a 64-bit counter, read the lower address (lower 32 bits of counter) first, followed by the upper address. The first read causes all 64 bits to be simultaneously latched into an internal holding register. The second read is directed to this holding register. The statistics bit must be set off to write to the counters.

Table 42: Counter Register Bit Assignments

31	30	29	28	27	26	25: 7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25:D7	D6	D5	D4	D3	D2	D1	D0

Port Counter Registers

The Port Counter descriptions in Table 43 are intended to be illustrative. For the exact definition of these counters, refer to the Repeater MIB, RFC 1516. All counters count packets, octets or events that were received at each port. In the descriptions, the length of a packet never includes pre-amble or framing bits (start of frame, end of frame, dribble bits, etc.), but an “event” does include these items.

Table 43: Port Counter Registers

Name	Offset Addr[1]	Description
rptrMonitorPortReadableFrames	0X0	Counts valid-length (64 to 1518 bytes), valid-CRC, collision-free packets. Depending on the state of the CountMode bit in the Master Configuration Register, this counter will count either all packets (CountMode = 0) or only Unicast Packets (CountMode = 1).
rptrMonitorPortReadableOctets [2] (Lower/Upper)	0X1, 0X2	Counts the number of octets in all valid-length (64 to 1518 bytes), valid-CRC, collision-free packets, not including preamble and framing bits. This register is not affected by the CountMode bit.
rptrMonitorPortFrameCheckSequence	0X3	Counts valid length, collision-free packets that had FCS errors, but were correctly framed (had an integral number of octets).
rptrMonitorPortAlignmentErrors	0X4	Counts valid length, collision-free packets that had FCS errors and were incorrectly framed (had a non-integral number of octets).
rptrMonitorPortFramesTooLong	0X5	Counts packets that had a length greater than 1518 octets.
rptrMonitorPortShortEvents	0X6	Counts events ≤ 88 bit times.
rptrMonitorPortRunts	0X7	Counts events > 92 and ≤ 504 bit times.
rptrMonitorPortCollisions	0X8	Counts the number of collisions that occurred, not including late collisions.
rptrMonitorPortLateEvents	0X9	Counts the number of times collision was detected more than 512 bit times after the start of carrier.
rptrMonitorPortVeryLongEvents	0XA	Counts the number of times any activity continued for more than 4 to 7.5 ms.
rptrMonitorPortDataRateMismatches	0XB	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a fifo underflow or overflow.
rptrMonitorPortAutoPartitions	0XC	Counts the number of times this port has been partitioned by the Auto-partition algorithm.
rptrTrackSourceAddrChanges	0XD	Counts the number of times the source address has changed. Minimum roll-over time of 81 hours.

1. Replace “X” in address with specific port to be addressed (offsets 0 through 4 correspond to Ports 1 through 5).
2. This register does not clear to zero.

Table 43: Port Counter Registers – continued

Name	Offset Addr[1]	Description
rptrMonitorPortBroadcastPkts	0XE	Counts the number of good broadcast packets received by this port. Counter is not cleared by ZeroCount bit.
rptrMonitorPortMulticastPkts	0XF	Counts the number of good multicast packets received by this port. Counter is not cleared by ZeroCount bit.
rptrMonitorPortIsolates - Port 1	050	Counts the number of times a port auto isolates. NOTE: When these counters increment, none of the other port counters will increment since the frame never had a valid start.
rptrMonitorPortIsolates - Port 2	051	
rptrMonitorPortIsolates - Port 3	052	
rptrMonitorPortIsolates - Port 4	053	
rptrMonitorPortIsolates - Port 5	054	
rptrMonitorSymbolErrorDuringPacket - Port 1	055	Counts the number of time a packet contained symbol errors. Only one symbol error is counted per packet.
rptrMonitorSymbolErrorDuringPacket - Port 2	056	
rptrMonitorSymbolErrorDuringPacket - Port 3	057	
rptrMonitorSymbolErrorDuringPacket - Port 4	058	

1. Replace “X” in address with specific port to be addressed (offsets 0 through 4 correspond to Ports 1 through 5).
2. This register does not clear to zero.

RMON Counter Registers

The interface counter descriptions in Table 44 are intended to be illustrative. For the exact definition of these counters, refer to the RMON MIB, RFC 1757. All counters count events, octets or packets that were received from the interface. Packet length never includes preamble or framing bits (start of frame, end of frame, dribble bits, etc.).

Table 44: RMON Counter Registers

Name	Type	Addr	Description
etherStatsOctets	R/W	05C, 05D	The number of data octets including those in bad packets and octets in FCS fields, but does not include preamble or other framing bits.
etherStatsPkts	R/W	05E	The number of packets received from the network, including errored packets.
etherStatsBroadcastPkts	R/W	05F	The number of good broadcast packets received. Counter is not cleared by ZeroCount bit.
etherStatsMulticastPkts	R/W	060	The number of good multicast packets received.
etherStatsCRCAlignErrors	R/W	061	The number of valid-length packets (64 to 1518 bytes inclusive) that had a bad Frame Check Sequence (FCS).
etherStatsUndersizePkts	R/W	062	The number of well-formed packets that were smaller than 64 octets.
etherStatsOversizePkts	R/W	063	The number of well-formed packets that were longer than 1518 octets.
etherStatsFragments	R/W	064	The number of ill-formed packets less than 64 octets. Note: Any event without a start-of-frame delimiter (0-octet packet) will be counted as a fragment, no matter how long it is.
etherStatsJabbers	R/W	065	The number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with an FCS error.
etherStatsCollisions/ rptr Monitor Transmit Collisions	R/W	066	The best estimate of the total number of collisions on this interface.
etherStatsPkts64Octets	R/W	067	The number of packets (good and bad) that were 64 octets long.
etherStatsPkts65to127Octets	R/W	068	The number of packets (good and bad) between 65 and 127 octets long.
etherStatsPkts128to255Octets	R/W	069	The number of packets (good and bad) between 128 and 255 octets long.
etherStatsPkts256to511Octets	R/W	06A	The number of packets (good and bad) between 256 and 511 octets long.
etherStatsPkts512to1023Octets	R/W	06B	The number of packets (good and bad) between 512 and 1023 octets long.
etherStatsPkts1024to1518Octets	R/W	06C	The number of packets (good and bad) between 1024 and 1518 octets long.
Not Used	R/W	06D	
rptrMonitorTotalOctets (Lower/Upper)	R/W	06E, 06F	The total number of octets contained in valid frames received on this segment. Counter is not cleared by ZeroCount bit.

Ethernet Address Registers

All Ethernet address registers consist of two 32-bit registers that together contain a 48-bit Ethernet address. Refer to Table 45 for register bit assignments.

Table 45: Ethernet Address Register Bit Assignments

Upper Address	Bits 15:0 contain bits 47:32 of the Ethernet address.
Lower Address	Bits 31:0 contain bits 31:0 of the Ethernet address.

Port Address Tracking Registers

The Port Address Tracking Register set is described in Table 46. These registers continuously monitor the source addresses of packets emanating from the corresponding ports. Refer to Table 45 for bit assignments.

Table 46: Port Address Tracking Registers

Name	Size (bits)	Addr	Description
rptrAddrTrackNewLastSrcAddress Port 1	48	070, 071	Stores the value of the last source address received. Can also act as NewLastSourceAddress via SW. These addresses power-up unknown, but can be zeroed by software. Example Address: 00-20-7B-03-02-01 First Read: $_{msb}037B2000_{lsb}$. Second Read: $_{msb}$ XXXX0102$_{lsb}$ All addresses must read in order. Only the first read updates the holding register. X's are currently defined as zeros.
rptrAddrTrackNewLastSrcAddress Port 2	48	072, 073	
rptrAddrTrackNewLastSrcAddress Port 3	48	074, 075	
rptrAddrTrackNewLastSrcAddress Port 4	48	076, 077	
rptrAddrTrackNewLastSrcAddress Port 5 (MII)	48	078, 079	

1. All Port Address Tracking Registers are Read/Write.

Search Address Registers

The Search Address Register set is described in Table 47.

Table 47: Search Address Registers

Name	Type	Addr	Size (bits)	Description
Search Address Register Refer to Table 45 for bit assignments.	R/W	08A, 08B	48	On-board address search register. Should the user wish to find out if a particular source address has been seen on any of the ports, on any of the segments, this register would be used. Each port within an LXT981 chip will be checked for traffic originating from the source address matching this register. If a match is found, the port number where the traffic originated will be saved thus allowing software to determine where the address is located. The register that contains the port from the search address match function is the Search Address Match Register. (default = X's)
Search Port Match Register	R	090	5	This register holds the port number of the host which uses the address specified in the Search Address Register. When the register clear bit (bit 11) in the Repeater Configuration Register is set to a '0', this register is cleared upon reading. If the register clear bit is set to a '1', this register's bit(s) are cleared by writing a '1' to the appropriate bit(s). (default = 0s)

Control and Status Registers

The control and status register set includes general port control and status registers that conform to the bit assignments shown in Tables 48, 50, and 53. Additional control and status registers with alternate bit assignments are shown in Tables 54 through 61.

Port Link Control Register

The Port Link Control Register is described in Table 49. Refer to Table 48 for Port Link Control Register bit assignments.

Table 48: Port Link Control and Status Register Bit Assignments

31:4	3	2	1	0
Rsvd	Port 4	Port 3	Port 2	Port 1

Table 49: Port Link Control Register

Name	Type	Addr	Description
Port Link Control	R/W	091	This register controls the link function of the 4 twisted-pair ports of the LXT981. When disabled, a port will no longer be disconnected due to Link Fail. When enabled, the port will only remain connected to the network so long as link pulses are being received: 0 = disable, 1 = enable (default).

General Port Control Registers

The General Port Control Register set is described in Table 51. Refer to Table 50 for the general port control registers bit assignments.

Table 50: General Port Control and Status Register Bit Assignments

31:5	4	3	2	1	0
Rsvd	Port 5 (MII)	Port 4	Port 3	Port 2	Port 1

Table 51: General Port Control Registers

Name	Type	Addr	Description
Port Alternate Partition Algorithm Control	R/W	094	Provides per-port selection of Partition Algorithms. 0 = normal, (default). Un-partition a port *only when data can be transmitted* to the port for 450-560 bit times without a collision on that port. 1 = alternate. Un-partition a port when data can be *either received or transmitted* from the port for 450-560 bit times without a collision on that port.
Port Enable	R/W	095	This register controls whether a port is enabled/disabled. If the $\overline{\text{MGR\_PRES}}$ signal is Low on power-up, then all ports will be disabled until such time that management software re-enables them. Otherwise the ports will power on enabled. 0 = disable, 1 = enable (default = 1).

Port Learn and Mode Control Registers

The Port Learn And Mode Control Register set is described in Table 54. Refer to Tables 52 and 53 for the corresponding bit assignments.

Table 52: Port Learn Control Registers

31:10	9	8	7	6	5	4	3	2	1	0
Rsvd	Port 5 (MII)		Port 4		Port 3		Port 2		Port 1	

Table 53: Port Mode Control Registers

31:9	8	7	6	5	4	3	2	1	0
Reserved	Port 5 (MII)	Reserved	Port 4	Reserved	Port 4	Reserved	Port 2	Reserved	Port 1

Table 54: Port Learn and Mode Control Registers

<table>
<tr><th>Name</th><th>Type</th><th>Addr</th><th colspan="3">Description</th></tr>
<tr><td rowspan="5">Port Authorized Learn Enable Control</td><td rowspan="5">R/W</td><td rowspan="5">096</td><td colspan="3">This register is used to encode the level of learning each port will use. The learn encodings are as follows:</td></tr>
<tr><td>Bit 1</td><td>Bit 0</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>Learn each new source address.</td></tr>
<tr><td>0</td><td>1</td><td>Next Lock. Learn only the first source address encountered. After a port learns its first address, it will change the Authorized Learn bits (for that port) to a “10” thus locking down the address.</td></tr>
<tr><td>1</td><td>0</td><td>Lock. Hardware has locked down the address. Only software can now write to this address.</td></tr>
<tr><td>1</td><td>1</td><td>Reserved.</td></tr>
<tr><td>Port Mode Control</td><td>R/W</td><td>097</td><td colspan="3">If this register is written to, it will override the hardware preload of information. Default is set by PORTnSEL pins. Encoding is as follows:
0 = 100Meg Fiber.
1 = 100Meg TP.</td></tr>
</table>

Port Status Registers

The Port Status Register set is described in Table 56. Bit assignments are shown in Table 55.

Table 55: Port Status Register Bit Assignments

31:4	4 [1]	3	2	1	0
Rsvd	Port 5 (MII)	Port 4	Port 3	Port 2	Port 1

1. Bit 4 not used in all registers.

Table 56: Port Status Registers

Name	Type[1]	Addr	Description
Port Link Status [2]	R	098	A read of this register will reflect the current link status of the 4 twisted-pair ports within a LXT981 chip. A ‘1’ indicates that the port is currently in the LINK_GOOD state. (default = 0s)
Port Polarity Status [2]	R	099	A read of this register will reflect the current polarity status of the 4 twisted-pair ports within a LXT981 chip. A ‘1’ indicates that the polarity has been crossed for a given port. (default = 0s)
Port Partition Status	R	09A	A read of this register will reflect the current partition status of all 5 ports within a LXT981 chip. A ‘1’ indicates that the port has been partitioned out of the repeater. A ‘0’ is read if the port is connected. (default = 0s)
Port Isolation Status [2]	R	09D	Fast Ethernet Port Isolation (Clause 27.3.2 of 802.3u).

1. R = Read Only.
2. Bit 4 (MII Port 5) not used in this register.

Interrupt Status/Mask Registers

The Interrupt Status and Mask Registers are described in Tables 58 and 59. Refer to Table 57 for bit assignments.

Table 57: Interrupt Status/Mask Register Bit Assignments

31:8	7	6	5	4	3	2	1	0
Reserved	Far-End Fault	Reserved	Jabber	Isolate	Partition	FCC	Source Address Change	Speed Change Detected

Table 58: Interrupt Status/Mask Register

Name	Type	Addr	Notes
Interrupt Status Register	R(/W)[1]	0AE	This register captures status bits within the LXT981 and holds them. Refer to Table 59 for bit descriptions.
Interrupt Mask Register	R/W	0AF	This register allows masking of individual interrupts. 0 = do not mask (default). 1 = mask.

1. R(/W) When the Register Clear bit (bit11) in the Repeater Configuration Register is set to a '0', this register is cleared upon reading. If the Register Clear bit is set to a '1', these register bit(s) are cleared by writing a '1' to the appropriate bit(s).

Table 59: Interrupt Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:8	Reserved	R/W	Reserved - Write as 0s; ignore on read.	N/A
7	Far End Fault	R/W	A '1' indicates that one of four conditions has occurred: 1. A port in fiber mode received the remote fault code from its link partner. 2. A port in auto-negotiation received 3 FLPs in a row with the remote fault bit set. 3. A port is in fiber mode with remote fault reporting enabled, and either the receive PLL is unlocked or the signal detect input has been lost. 4. A port in auto-negotiation is transmitting FLPs with the remote fault bit set. In conditions 1 and 2 the link partner has detected the remote fault condition and is sending it to the LXT981. In conditions 3 and 4 the LXT981 has detected the remote fault condition and is sending it to the link partner.	0
6	Reserved	R/W	Reserved - Write as 0s; ignore on read.	0

1. R = Read only; R/W = Read/Write.

Table 59: Interrupt Register Bit Definitions – continued

Bit	Name	Type[1]	Description	Default
5	Jabber	R	A ‘1’ indicates that a port is in jabber state. Jabber occurs when any receiver remains active for more than 57,500 bit times. The LXT981 exits this state when all receivers return to the idle condition.	0
4	Isolate	R/W	A ‘1’ indicates that a port has been isolated. The LXT981 isolates any port that transmit more than two successive false carrier events. A false carrier event is defined as a packet that does not start with a /J/K symbol pair.	0
3	Partition	R/W	A ‘1’ indicates that a port has been partitioned. The LXT981 partitions any port that participates in excess of 60 consecutive collisions. In 10M operation, the LXT981 partitions any port that participates in excess of 32 consecutive collisions. Once partitioned, the LXT981 will continue monitoring and transmitting to the port, but will not repeat data received from the port until it properly un-partitions.	0
2	FCC	R/W	A ‘1’ indicates that a port has received too many false carrier events.	0
1	SA Change	R/W	A ‘1’ indicates that a port address changed from that stored in the last-SourceAddress Register.	0
0	Reserved	R/W	Reserved - Write as 0s; ignore on read.	N/A

1. R = Read only; R/W = Read/Write.

MII Status Register

The MII Status Register is described in Table 61. Refer to Table 60 for bit assignments

Table 60: MII Status Register Bit Assignment

31:1	0
Reserved	Selects connecting device type 0 = MAC Mode (connected to a PHY). 1 = PHY Mode (connected to a MAC).

Table 61: MII Status Register

Name	Type	Addr	Description
MII Register	R	0B4	Reports the status of the MII port. Default is set by pins.

Configuration Registers

The Configuration Register set is described in Table 62. Bit assignments for the Configuration Registers are shown in Tables 63 through 70.

Table 62: Configuration Registers

<table>
<tr><th>Name</th><th>Type[1]</th><th>Addr</th><th>Notes</th></tr>
<tr><td>Repeater Configuration Register</td><td>R/W</td><td>0AB</td><td>Refer to Table 63 for bit assignments.</td></tr>
<tr><td>Repeater Serial Configuration Register</td><td>R</td><td>0AC</td><td>This 8 bit register holds user-defined data. These bits may be used to indicate the type of board configuration, port count or other vendor-related data. Default is set by pins.</td></tr>
<tr><td>Device/Revision ID Register</td><td>R</td><td>0AD</td><td>This register follows the IEEE 1149.1 specification. Refer to Table 65 for bit assignments.
The upper 4 bits identify the device revision level. The next 16 bits store the Part ID Number, which in this case is hexadecimal ‘3D5’. The next 11 bits contain a JEDEC Manufacturer ID, which for Level One is hexadecimal ‘FE’. The lowest bit (0) is set only for the first device in a chain.</td></tr>
<tr><td>Reserved</td><td>R</td><td>0B0</td><td>Ignore on read.</td></tr>
<tr><td>Global LED Control Register</td><td>R/W</td><td>0B1</td><td>Refer to Table 66 for bit assignments. This register reflects the LED Mode set by pins 207 and 208, and provides software control for the global fault LED.
LED Mode, Bit Encoding (read only from pins):
<table>
<tr><th>Bit 5</th><th>Bit 4</th><th>Mode Selected</th></tr>
<tr><td>0</td><td>0</td><td>Mode 1</td></tr>
<tr><td>0</td><td>1</td><td>Mode 2</td></tr>
<tr><td>1</td><td>0</td><td>Mode 3</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
Global Fault LED, Bit Encoding:
<table>
<tr><th>Bits 3: 2</th><th>Modes 1 & 3</th><th>Mode 2</th></tr>
<tr><td>0 0</td><td>LED off</td><td>LED off</td></tr>
<tr><td>0 1 [2]</td><td>Hardware control</td><td>Hardware control</td></tr>
<tr><td>1 0</td><td>Reserved</td><td>LED slow blink</td></tr>
<tr><td>1 1 [3]</td><td>LED off</td><td>LED on steady</td></tr>
</table></td></tr>
</table>

1. R = Read only; W = Write only; R/W = Read /Write
2. Default value if manager is not present.
3. Default value if manager is present.

Table 62: Configuration Registers – continued

<table>
<tr><th>Name</th><th>Type[1]</th><th>Addr</th><th>Notes</th></tr>
<tr><td>Port LED Control Register</td><td>R/W</td><td>0B2</td><td>This register provides a measure of software control over the port LED’s. Refer to Table 67 for bit assignments. During reset, the state of this register is all 1s. If a manager is present, this register remains in the all 1s state after reset. Otherwise, the bits default to hardware control. Encoding is as follows:
<table>
<tr><th>Bits 1 : 0</th><th>Modes 1 & 3</th><th>Mode 2</th></tr>
<tr><td>0 0</td><td>LED off</td><td>LED off</td></tr>
<tr><td>0 1</td><td>Reserved</td><td>LED fast blink</td></tr>
<tr><td>1 0 [2]</td><td>Hardware Control</td><td>Hardware Control</td></tr>
<tr><td>1 1 [3]</td><td>LED off</td><td>LED on steady</td></tr>
</table></td></tr>
<tr><td>LED Timer Control Register</td><td>R/W</td><td>0B3</td><td>Refer to Table 68 for bit assignments. Bits 8-15 of this register set the fast blink frequency of the LEDs. Bits 0-7 set the slow blink frequency. The same formula is used in each case, with a maximum of 128 Hz and a minimum of 0.5 Hz.
Example:
fast blink = x32 (0.4 sec)
slow blink = xCC (1.6 sec).</td></tr>
<tr><td>Repeater Reset Register</td><td>W</td><td>0B5</td><td>Writing any data value to this register with the Least Significant Bit (LSB) = 1 causes the repeater functional logic to reset. (Any bits other than LSB do not matter.) The counters and configuration information will be held static and will not be reset. (default = 0s)</td></tr>
<tr><td>Software Reset Register</td><td>W</td><td>0B6</td><td>Writing any data value to this register with the Least Significant Bit (LSB) = 1 is identical to a hardware reset. (Any bits other than LSB do not matter.) Everything is reset except the Source Address RAM. (default = 0s)</td></tr>
<tr><td>Assign Address Register
(1 and 2)</td><td>W</td><td>188, 189</td><td>Refer to Table 69 for bit assignments. Writing a valid 48-bit ID (one that matches the EPROM ID) to this register causes the device to change its Hub ID to the contents of the EPROM ID register listed below. This register cannot be read.</td></tr>
<tr><td>EPROM Address Register
(1 and 2)</td><td>R</td><td>190, 191</td><td>These two registers contain the 48-bit ID read in from EPROM at power-up. Refer to Table 70 for bit assignments.</td></tr>
</table>

1. R = Read only; W = Write only; R/W = Read /Write
2. Default value if manager is not present.
3. Default value if manager is present.

Repeater Configuration Register

This register contains many of the global repeater settings. The Repeater Configuration Register is described in Table . Refer to Table 63 for bit assignments of the Repeater Configuration Register.

Table 63: Repeater Configuration Register Bit Assignments

31:13	12	11	10	9	8	7	6	5	4	3	2	1:0
Rsvd	Enable Port Late Event	Auto Clear	Stats Enabl	Send /T/R	Isolate	Rsvd	Uni-cast Frame Count	Arbit Input Value	Zero Ctrs	Enable FIFO Error	Enable Manch Code Viol	Rsvd

Table 64: Repeater Configuration Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:13	Reserved	R/W	Reserved - Write as 0s; ignore on read.	N/A
12	Enable PortN Late Event	R/W	A ‘0’ does not allow out-of-window collisions to increment portN’s Late Event Counter. A ‘1’ does allow it.	0
11	Auto-Clear	R/W	A ‘0’ causes Interrupt Status Register and Search Port Match Register to automatically clear when read. A ‘1’ requires that the appropriate register bits be written to be cleared. This is done by writing a ‘1’ to the bit(s) that are to be cleared.	0
10	Statistics Enable	R/W	Turns statistics gathering on and off. A ‘1’ enables statistics gathering. ‘0’ disables statistics gathering.	1
9	Send /T/R	R/W	Forces a good /T/R after each 100M transmission. A ‘1’ forces /T/R. ‘0’ disables forced /T/R.	0
8	Isolate	R/W	Isolates the $\overline{\text{IRCFS}}$ stack signal and provides an output pin for disabling an external backplane transceiver. A ‘1’ isolates. ‘0’ does not isolate.	0
7	Reserved	R/W	Reserved - Write as 0s; ignore on read.	N/A
6	CountMode	R/W	Changes the definition of portReadableFrames to only count Unicast Frames. A ‘1’ counts Unicast only. ‘0’ counts all.	0
5	Arbitration Input Value	R	As read from input pin.	N/A

1. R = Read only; R/W = Read/Write.
2. While zeroing is in progress, the CPU will be locked out from accessing the statistics RAM until the Zero Counters bit has been reset back to ‘0’. This will be approximately 15 µs.
3. The rptrMonitorPortBroadcastPkts and rptrMonitorPortMulticastPkts counters (refer to Table 43 on page 58) are not cleared by the Zero Counters bit.

Table 64: Repeater Configuration Register Bit Definitions – continued

Bit	Name	Type[1]	Description	Default
4	Zero Counters	R/W	A '1' causes the LXT981 to sequentially walk through each counter location and zero its contents[2]. When all counter locations have been cleared[3], this bit will be reset to a '0'.	0
3	Enable FIFO error	R/W	When a '1', the LXT981 will not enter transmit collision upon detection of a data rate mismatch.	1
2:0	Rsvd	R/W	Reserved - Write as 0s; ignore on read.	N/A

1. R = Read only; R/W = Read/Write.
2. While zeroing is in progress, the CPU will be locked out from accessing the statistics RAM until the Zero Counters bit has been reset back to '0'. This will be approximately 15 µs.
3. The rptrMonitorPortBroadcastPkts and rptrMonitorPortMulticastPkts counters (refer to Table 43 on page 58) are not cleared by the Zero Counters bit.

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Table 65: Device/Revision Register Bit Assignment

31:28	27:12	11:8	7:1	0
Version	**Part ID**	**Jedec Continuation Characters**	**JEDEC ID[1]**	**1st in Chain[2]**
0000	0000 0011 1101 0101	0000	111 1110	See Note 2

1. The JEDEC ID is an 8-bit identifier. However, the MSB is for parity only and is ignored. Level One's JEDEC ID is FE (1111 1110) which becomes 111 1110.
2. First Chain Bit = 0 if ChipID ≠ 000.
   First Chain Bit = 1 if ChipID = 000.

Table 66: Global LED Control Register Bit Assignments

31:6	5	4	3	2	1:0
Reserved	**Mode Control**		**Global Fault LED**		**Reserved**

Table 67: Port LED Control Register Bit Assignments

31:10	9	8	7	6	5	4	3	2	1	0
Rsvd	**Port 5 (MII)**		**Port 4**		**Port 3**		**Port 2**		**Port 1**	

Table 68: LED Timer Control Register Bit Assignments

31:16	15:8	7:0
Reserved	Slow Blink Frequency	Fast Blink Frequency
1. Period = 7.8125 ms x (Register Value + 1) 2. $\text{Frequency} = \frac{1}{7.8125\text{ms} \times (\text{Register Value} + 1)}$		

Table 69: Address Assignment Register Bit Assignments

Assign Addr 1	31:0		
	Bits (47:16) of the EPROM Serial number		
Assign Addr 2	31:21	20:16	15:0
	Zeros	Hub ID(4:0)	Bits (15:0) of the EPROM serial number

Table 70: EPROM Address Register Bit Assignments

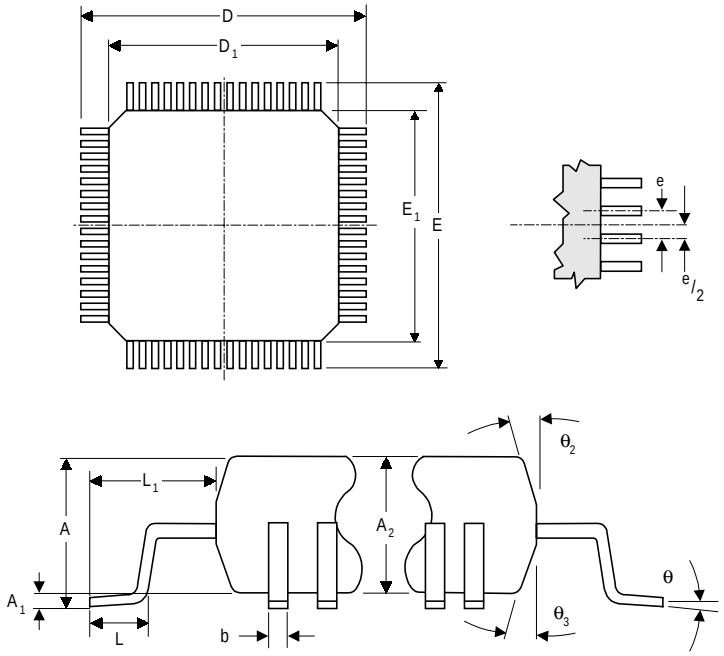
EPROM Addr 1	31:0	
	Bits(47:16) of the EPROM serial number	
EPROM Addr 2	31:16	15:0
	Zeros	Bits (15:0) of the EPROM serial number

MECHANICAL SPECIFICATIONS

Figure 35: LXT981 Package Specifications

208-Pin Plastic Quad Flat Package

- Part Number LXT981QC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

REVISION HISTORY

Table 71: Changes from Rev 1.0 to Rev 1.1 (12/98)

Section	Page	Change	Description
Cover Page Subtitle	1	Delete	Remove “and 10BASE-T Applications” from subtitle.
Features		Modify	Change 0 - 70° temperature range to “Case Temperature range: 0 - 115°.
Pin Assignments and Signal Descriptions Figure 1	4	Add	Add overscore bar to IRQ to correctly indicate as “Active Low”.
IRB Signals Table 6	8	Add	Add “Schmitt MOS PU” to IRSNGL, IRCOL, IRDV, IR100DAT<0:4>.
		Modify	Rewrite, expand $\overline{\text{IRCFS}}$, $\overline{\text{IRCFSBP}}$, and $\overline{\text{IRDV}}$ signal descriptions.
	9	Add	Add “PD” to IRCLK.
			Add a 1k pull-up resistor to IRCLK line.
SMI Signals Table 7			Add “PD” to SERCLK.
		Modify	Re-write Arbitration In/Out description.
	10		To Manager Present description, change first sentence to read: “This signal is sensed at power up *and hardware reset*.”
PROM Signals Table 9	11	Add	Add “PD” to PROM_CLK, PROM_DTN.
		Modify	Rewrite, expand PROM_CS and PROM_DTOUT signal descriptions.
Power Supply and Indication Signals		Add	Replace type “-” with appropriate “Digital” and “Analog” indications.
Power Supply & Indication Signals	12	Modify	Change value of resistor connected between RBIAS pin and ground from 22 kΩ to 22.1 kΩ.
Misc. Signals Table 11	12	Correct	Change IRQ to $\overline{\text{IRQ}}$ to correctly indicate as “Active Low”.
	13	Add	Add “PD” to CONFIG<0:7> Type column.
		Correct	Add Pin “1” to column indicating “NC”.
MII	17	Add	Add the following note: The MII does not auto-negotiate, auto speed select, auto-link, or partition.
Repeater Operation	18		Add “one collision approx. 575.2 µs long.”
Bias Current	19	Modify	Change value of resistor connected between RBIAS pin and ground from 22 kΩ to 22.1 kΩ
IRB Bus Pull-ups	20	Add	Add IRCLK.
100M IRB Signals Table 16	23	Modify	For IRCLK, change “No” under Pull-up Heading to “1 kΩ”.

Table 71: Changes from Rev 1.0 to Rev 1.1 (12/98)

Section	Page	Change	Description
100M IRB Signals Table 16	23	Modify	$\overline{\text{IRCFSBP}}$ Pull-up resistor = 82Ω.
MII Port Operation	25	Delete	Delete first sentence, second paragraph.
MII Port Timing	26	Modify	Rewrite, clarify section.
Figure 8			Modify to clarify MII-to-MII, PHY-to-MAC prop. delay.
Auto-Clearing Registers	28	Add	Add description/explanation of certain “Clear on Read” Registers.
SMI Message Fields	28	Modify	For Chip ID message: change “eight modules” to “eight LXT980 devices on a board or sub-system.
Chain Arbitration Mech.	31	Add	To second paragraph, add the following sentence: “Tie to ARBOUT of the SCC or to previous hub in the daisy chain. The first hub ARBIN can also be grounded.”
General Design Guidelines	33	Modify	Update entire section and remove references to separate analog & digital ground planes and associated ferrite bead filter.
RBIAS Pin Para 4	34		Change value of resistor connected between RBIAS pin and ground from 22 kΩ to 22.1 kΩ.
Magnetics Information Table 21-22	35	Delete Modify	Delete Suggested Magnetics List. Update Magnetics Specifications. Move differential to CMR from “Min” to “Max” column; indicate as -40 and -35 for.1 to 60 MHz and 60 to 100 MHz, respectively.
Power and Gnd. Connections Figure 17	38	Modify	Change value of resistor connected between RBIAS pin and ground from 22 kΩ to 22.1 kΩ.
Twisted-Pair Interface Figure 19	40	Modify	Reverse RJ45 connections to show repeater I/F, not NIC. Should be: TPOP = 3, TPON = 6 TPIP = 1, TPIN = 2
100M IRB Signals Figure 21	41	Add	Add two 1K pull-up resistors to IRCLK line, on both sides of the ‘245 buffer.
		Modify	$\overline{\text{IRCFSBP}}$ Pull-up Resistor = 82Ω.
Test Specifications	43	Modify Delete	Re-write “NOTE”; Delete “Over Recommended Range” from all Table titles (25-40).
Absolute Max Ratings Table 22		Modify	Increase Max Case Temp to 130.
		Modify	Revise Warning to address immediate EOS damage.
100 Mbps IRB Elect. Char. Table 26	44	Modify	$\overline{\text{IRCFSBP}}$ current test conditions: RL = 82Ω.

Table 71: Changes from Rev 1.0 to Rev 1.1 (12/98)

Section	Page	Change	Description
Test Spec Tables 29 - 40	46-56	Modify	Clarify definition of Bit times (BT) for both 10 and 100BASE-TX. This appears as a note to the "Unit" column.
			Change Timing Parameter Symbol convention.
Test Spec Figures 23 - 34			Modify figures to correspond to Timing Parameter convention changes.
100 IRB Timing Table 38 Figure 32	55	Delete Modify	Delete IR100ENA asserted to TPOP/N or FIBOP/N active and corresponding figure element.
Port Counter Register Table 43	58	Modify	rptrMonitorPortShortEvents counter should increment as follows: Counts events ≤ 88 bit times.
			rptrMonitorPortRunts counter should increment as follows: Counts events > 92 and ≤ 504 bit times.
RMON Counter Registers Table 44	60	Add	To "etherStatsBroadcastPkts" description add: "Counter is not cleared by ZeroCount bit. To "rptrMonitorTotalOctets" description add: "Counter is not cleared by ZeroCount bit.
Repeater Reset Register Table 62	69	Correct	Rewrite "Repeater Reset Register" and Software Reset Register description.
LED Timer Control Register Bit Assn.	72	Correct	Bit Assignments 15:8 = Slow Blink Frequency; 7:0 = Fast Blink Frequency.
Throughout	All	Modify	Replace "module" with "board" where appropriate.
All	All	Modify	Light editing throughout.
Backpage	80	Modify	Update

NOTES

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Revision	Date	Status
1.1	12/98	Additions to Signal Descriptions; correct Pin Assignments; correct Twisted-Pair I/F figure; change Max. Case temperature.
1.0	02/98	Initial Release, Preliminary Information.

DS-T981-R1.1-1298