SHARP®

Integrated Circuits Group

LR38539

PLL Frequency Synthesizer

1.2 GHz/500 MHz

(Model No.: LR38539)

Issue Date: April 7, 1998

CONTENTS

1. Description

This IC of monolithic, a low power Phase Locked Loop (PLL) Frequency Synthesizers, is designed to be used as a local oscillator for the RF and the IF of a dual conversion transceiver. It is fabricated using Sharp's CMOS process.

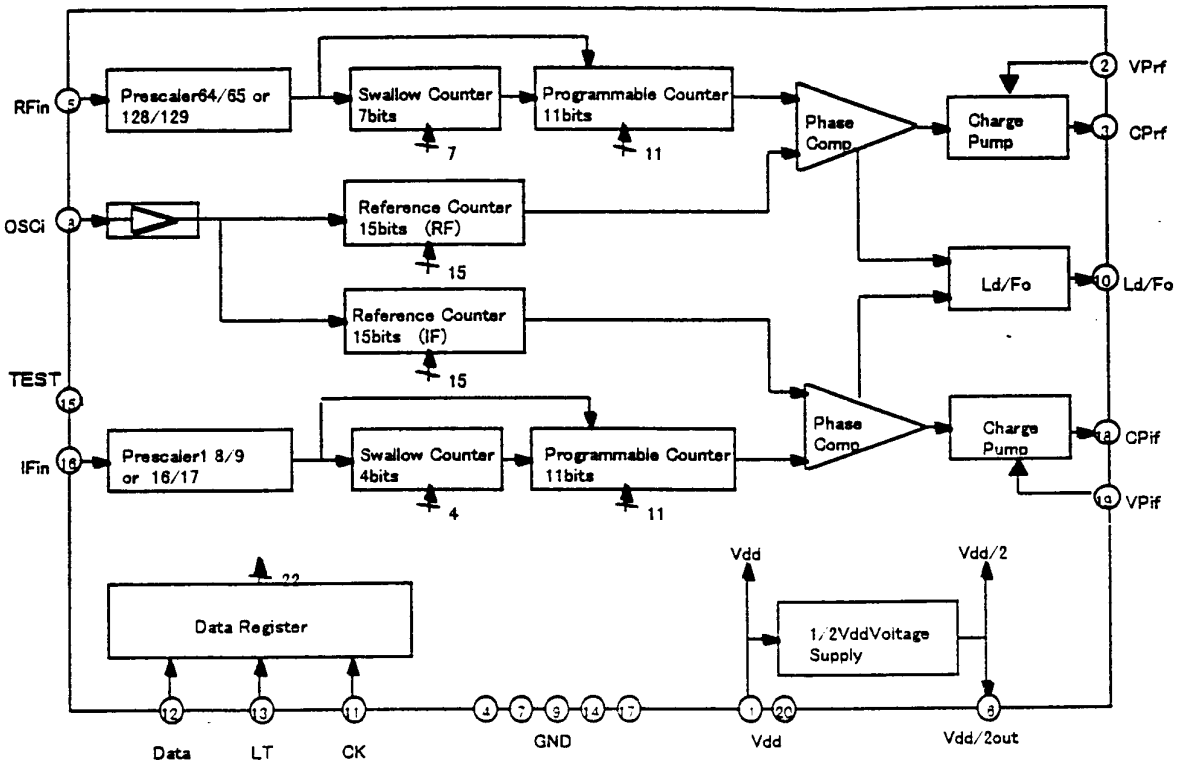
This Chip is integrated two dual modulus prescalers. One is a 64/65 or a 128/129 prescaler for the RF synthesizer, and Another one is a 8/9 or a 16/17 prescaler for the IF synthesizer. The RF synthesizers have 7bits A (IF synthesizers have 4bits) and 11bits N pulse swallow counters. The Reference counter is 15bits Programmable counter. It contains two digital phase comparator, for the RF and IF, with charge pump. PLL synthesizer is controlled by serial data. That is transferred into this IC via a three wire interface(Data, LT, CK). This IC is very low current consumption;2.8mA at 3V. This is available in a 20-pin SSOP surface mount plastic package.

2. Features

Process(structure)	CMOS
Chip Material	Silicon
Wafer substrate type	SOI
Package Type	20pin TSSOP
Package Material	Plastic
Maximum Operating Frequency	RF−PLL 1.2GHz
	IF−PLL 500MHz
Current Consumption	2.8mA (Type)
Operating Voltage Range	2.70～3.30V

Not designed or rated as radiation hardened.

3. Block Diagram

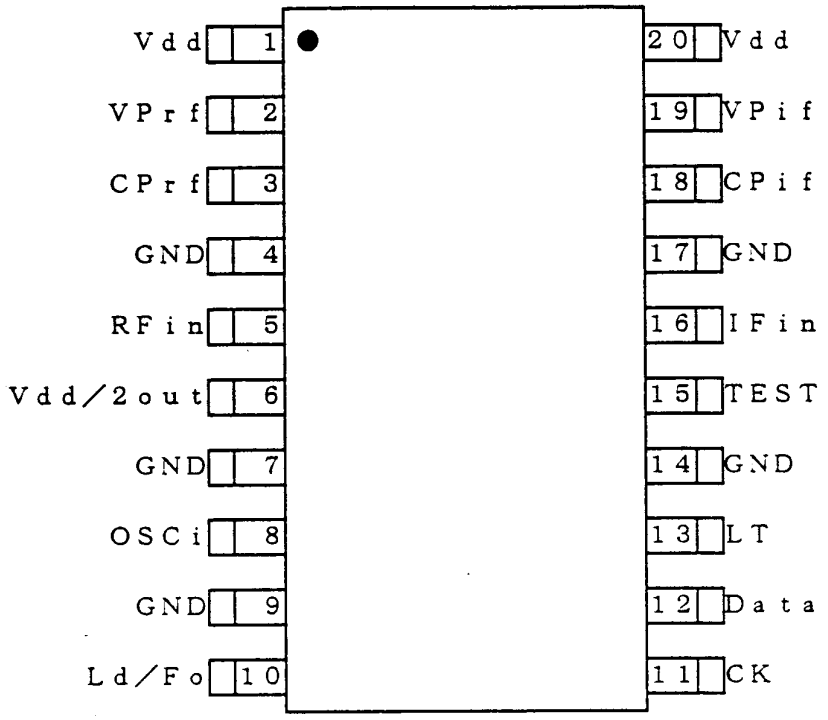


4. Pin Connections

4－1 Pin Table

PinNo.	I/O	Pin Name	PinNo.	I/O	Pin Name
1	—	Vdd	11	I	CK
2	—	VPrf	12	I	Data
3	—	CPrf	13	I	LT
4	—	GND	14	—	GND
5	—	RFin	15	I	TEST
6	—	Vdd/2out	16	I	IFin
7	—	GND	17	—	GND
8	I	OSCi	18	O	CPif
9	—	GND	19	—	VPif
10	O	Ld/Fo	20	—	Vdd

4－2 Pin Diagram



TOP VIEW

5. Pin Description

PinNo.	Pin Name	I/O	Description
1	Vdd	—	Power Supply Voltage Input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	VPrf	—	Power Supply Input for RF Charge pump.
3	CPrf	O	RF Charge pump output. Constant current output.
4	GND	—	Ground.
5	RFin	I	RF prescaler input from the RF VCO.
6	Vdd/2out	O	Vdd/2 Voltage supply output. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
7	GND	—	Ground.
8	OSCi	I	Reference Oscillator input.
9	GND	—	Ground.
10	Ld/Fo	O	Multiplexed output to the RF/IF Lock detect and RF/IF or reference dividers.
11	CK	I	Serial clock input.
12	Data	I	Serial data input.
13	LT	I	Serial strobe input.
14	GND	—	Ground.
15	TEST	I	TEST pin. Connected to ground with 0.1uF capacitor.
16	IFin	I	IF prescaler input from the IF VCO.
17	GND	—	Ground.
18	CPif	O	IF Charge pump output. Constant current output.
19	VPif	—	Power Supply Input for IF Charge pump.
20	Vdd	—	Power Supply Voltage Input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

6. Functional Description

(1) Serial Input Programming

The serial input is a 3-wire input (Data, CK, LT) to program all counter ratios, polarity of the phase detector, and other function of this IC. The programming data is structured into 22bit words. Figure1 shows the timing diagram of the serial input. When the LT= 'L' , the CK driver is enabled and Data shifted into register on the CK rising edge. Register data stored into each counter or function register LT rising edge.

(NOTE) Data is shifted in MSB first.

SERIAL DATA INPUT TIMING

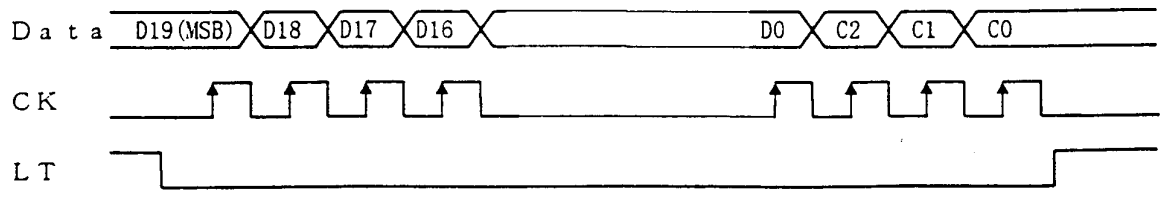


figure 1

(2) Serial Input Word Format

Data Shift Direction →

← Control bits ← Data bits →

C1	C2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
LSB	MSB	LSB																			MSB

(3) Control bits description

C2	C1	mode
0	0	IF Reference Divider (15bits programmable counter) Ratio setup
0	1	RF Reference Divider (15bits Programmable counter) Ratio setup
1	0	IF Divider (Swallow Counter A and Programmable Counter N) Ratio setup
1	1	RF Divider (Swallow Counter A and Programmable Counter N) Ratio setup

(4) Reference Divider Setup

C1	C2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17	R18	R19	R20

C1～C2 : Control bits

R1～R15 : 15bits Programmable Reference Counter Divide Ratio

R16～R20 : Programming bits

15bits Programming Counter Divide Ratio

R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	Divide Ratio
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	32767

(NOTE) Divide ratio less than 3 are prohibited

(5) Programmable Divider Setup

C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	N18	N19	N20

C1～C2 : Control bits

N1～N7 : 7bits Swallow Counter (A) Divide Ratio

N8～N18 : 11bits Programmable Counter (N) Divide Ratio

N19～N20 : Programming bits

7bits Swallow Counter Divide Ratio

(A Counter) (RF)

N7	N6	N5	N4	N3	N2	N1	Ratio
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	127

(A Counter) (IF)

N7	N6	N5	N4	N3	N2	N1	Ratio
×	×	×	0	0	0	0	0
×	×	×	0	0	0	1	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
×	×	×	1	1	1	1	15

(Note) ×: (N7, N6, N5) = (0, 0, 0) or (1, 1, 1) Normal Operation.
Other conditions are prohibited.

11bits Programmable Counter Divide Ratio

(N Counter)

N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Ratio
0	0	0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	1	1	2047

(Note) Divide ratio less than 3 are prohibited.

(6) Programmable Mode Control Setup

Following mode controlled by R16～R20, N19～N20bits

C 1	C 2	R 16	R 17	R 18	R 19	R 20
0	0	IF Phase Detector polarity	IF Charge Pump Output Current	IF Charge Pump Hi-Z	MD 3 (IF-Ld)	MD 1 (IF-Fo)
0	1	RF Phase Detector polarity	RF Charge Pump Output Current	RF Charge Pump Hi-Z	MD 4 (RF-Ld)	MD 2 (RF-Fo)

C 1	C 2	N 19	N 20
1	0	IF Prescaler Ratio	IF Power ON/OFF
1	1	RF Prescaler Ratio	RF Power ON/OFF

Mode Control Table

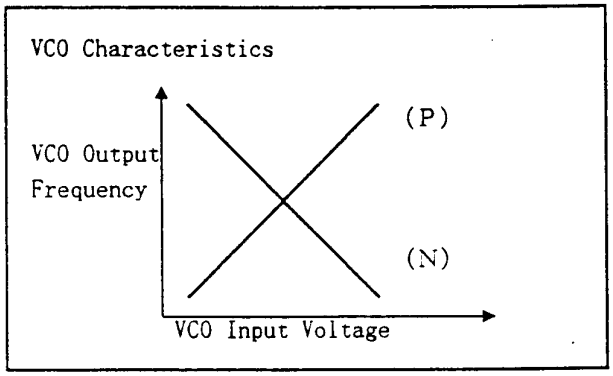
	Phase Detector Polarity	Charge Pump Current	Charge Pump Hi-Z	IF Prescaler	RF Prescaler	Power ON/OFF
0	Negative	1/4×High	Normal Operation	8/9	64/65	Power ON
1	Positive	High Current	Hi-Z	16/17	128/129	Power OFF

(Note) Phase Detector Polarity

Depending upon VCO characteristics.

When VCO characteristics are positive like(P):R16=1

When VCO characteristics are negative like(N):R16=0



VCO Characteristics Positive : (P)

VCO Characteristics Negative : (N)

Ld/Fo Output Mode Select Control

MD4	MD3	MD2	MD1	Ld/Fo Output State
0	0	0	0	Disabled (It is actively pulled to a Low logic state.)
0	1	0	0	IF Lock Detect Signal output
1	0	0	0	RF Lock Detect Signal output
1	1	0	0	RF/IF Lock Detect Signal output
×	0	0	1	IF Reference Divider output
×	0	1	0	RF Reference Divider output
×	1	0	1	IF Programmable Divider output
×	1	1	0	RF Programmable Divider output
0	0	1	1	It is actively pulled to a Low logic state.
0	1	1	1	IF counter reset. (IF charge pump output is Hi-Z)
1	0	1	1	RF counter reset. (RF charge pump output is Hi-Z)

× : DON'T CARE condition

Expect the above-mentioned states are prohibited.

TEST Mode Control

(IF)

N7	N6	N5	operation state
0	0	0	Normal operation
0	0	1	Normal operation
0	1	0	Normal operation
0	1	1	TEST Mode
1	0	0	TEST Mode
1	0	1	TEST Mode
1	1	0	TEST Mode
1	1	1	Normal operation

TEST Mode are prohibited.

(7) Pulse Swallow Function

VCO frequency, Prescaler ratio, and Counter divide ratios(A,N and R),are determined follows.

$$f_{vco} = [\,(P \times N) + A\,] \times f_{OSC} / R$$

f_{vco} : Output frequency of external VCO(Voltage Controlled Oscillator)
P : Divide ratio of dual modulus prescaler(RF:64/65 or 128/129, IF:8/9 or 16/17)
N : Divide ratio of Binary 11bits programmable counter ($3 \leqq N \leqq 2047$)
A : Divide ratio of Binary 7bits swallow counter ($0 \leqq A \leqq 127$、$A \leqq N$)
f_{OSC} : Output frequency of external reference frequency oscillator
R : Divide ratio of Binary 15bits programmable reference counter ($3 \leqq R \leqq 32767$)

7. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply voltage	Vdd, VPrf, VPif	−0.3～+4.0	V
Input Voltage	Vin	−0.3～Vdd+0.3	V
Operating temperature	Topr	−40～ +85	℃
Storage temperature	Tstg	−40～+150	℃

8. Electrical Characteristics

8－1 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Units
Supply voltage	Vdd, VPrf, VPif	2.70	3.00	3.30	V
Input H Voltage	VIH	0.7Vdd		Vdd+0.3	V
Input L Voltage	VIL	−0.3		0.3Vdd	V

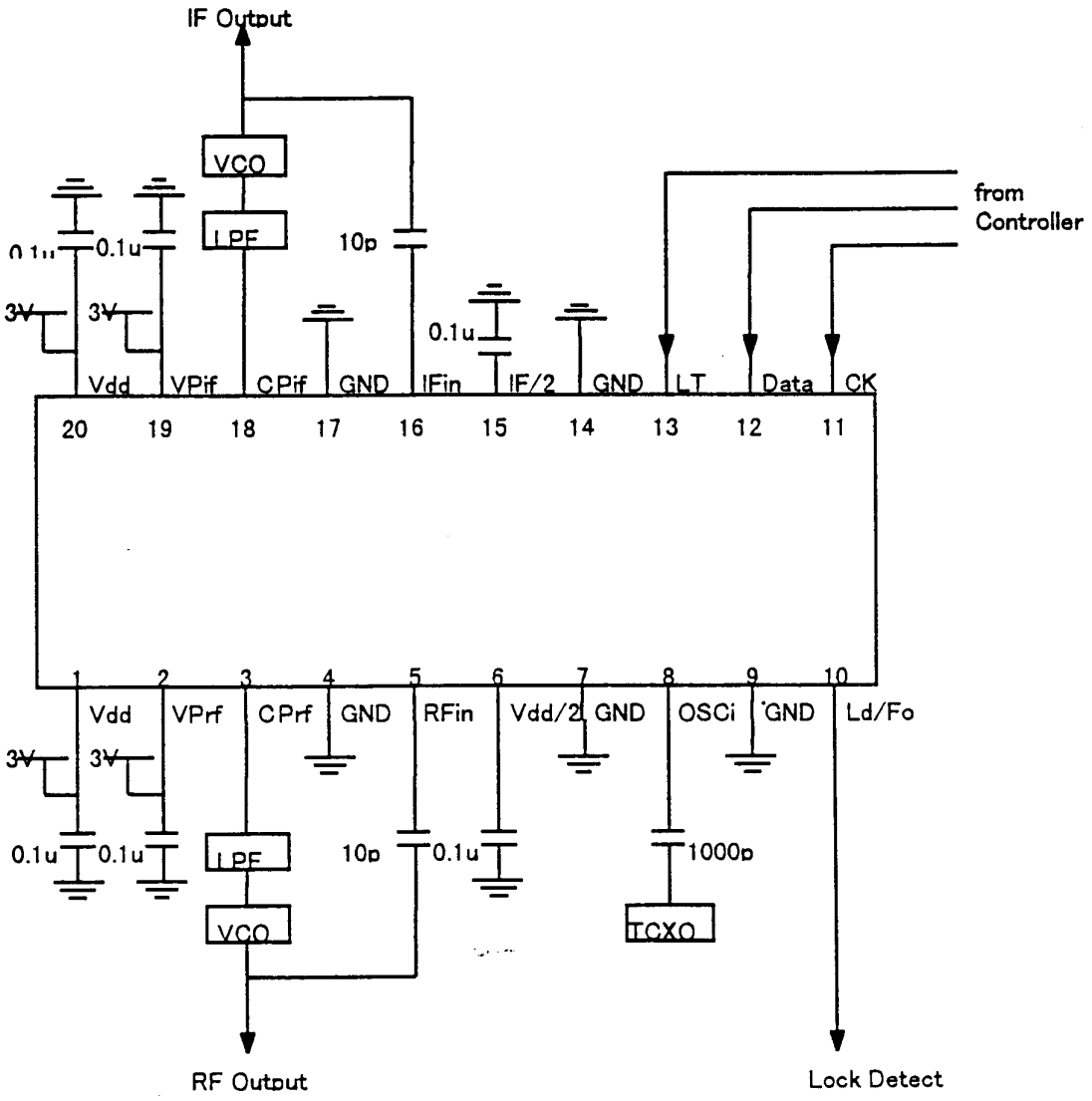
8－2 Electrical Characteristics

(Vdd=3.0V, VPrf=3.0V, VPif=3.0V, Ta=25℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Power Supply Voltage		Vdd	2.70	3.00	3.30	V
Power Supply Current (Note1)	Idd	RF+IF Operated		2.80		mA
	Idd(RF)	RF Only Operated				
	Idd(IF)	IF Only Operated				
	Idd-Pdwn	Power Down		1.00		μA
Operating Frequency	RFin	-10dBm			1200	MHz
	IFin	-10dBm			500	MHz
	OSCi				23	MHz
Input Sensitivity	RFin		−10			dBm
	IFin		−10			dBm
"H" Level Input Voltage	VIL		0.7Vdd			V
"L" Level Input Voltage	VIH		0.3Vdd			V
Charge pump Output Current (RF)	I-source			−4.0		mA
	I-sink			4.0		mA
Charge pump Output Current (IF)	I-source			−4.0		mA
	I-sink			4.0		mA
Charge pump Supply Voltage	VPrf, Vpif		2.70	3.00	3.30	V

Note1: [Conditions] Rfin=690MHZ, Ifin=257.6MHz, OSCi=14.4MHz)

9. Typical Application Example



Compatibility of LR38539(Sharp) and LMX2332L(National Semiconductor)

LR38539(Sharp) and LMX2332L(NS) are basically compatible and can exchange each other. However, please confirm the following difference.

1.Pin compatibility

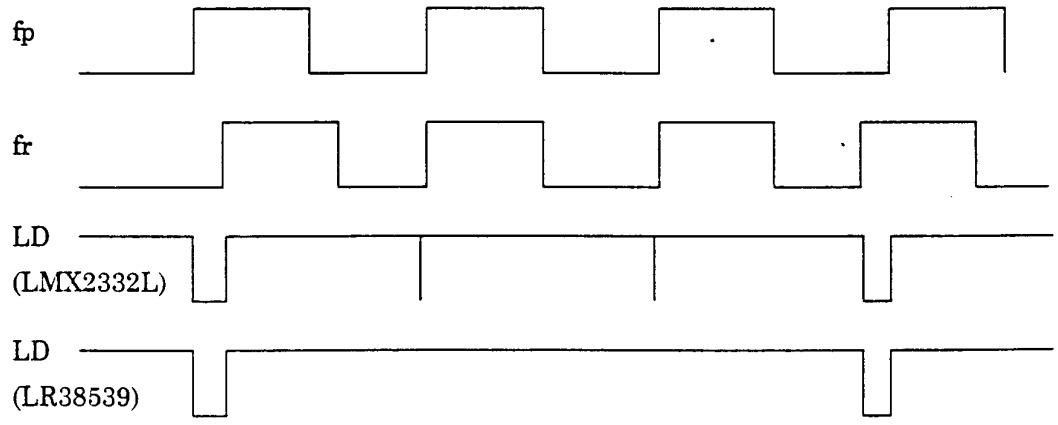
Each of these two ICs can be used on the same board in the conventional case.

Part Number	# Pin	Function	Condition
LR38539	6	Vdd/2out	Connected to GND via bypass capacitor (more than 0.1 μ F)
	15	Test	Either connected to GND via bypass capacitor or free
LMX2332L	6	finRF	Connected to GND via bypass capacitor
	15	finIF	

2.Functional differences

1)LD(Lock detect) Signal

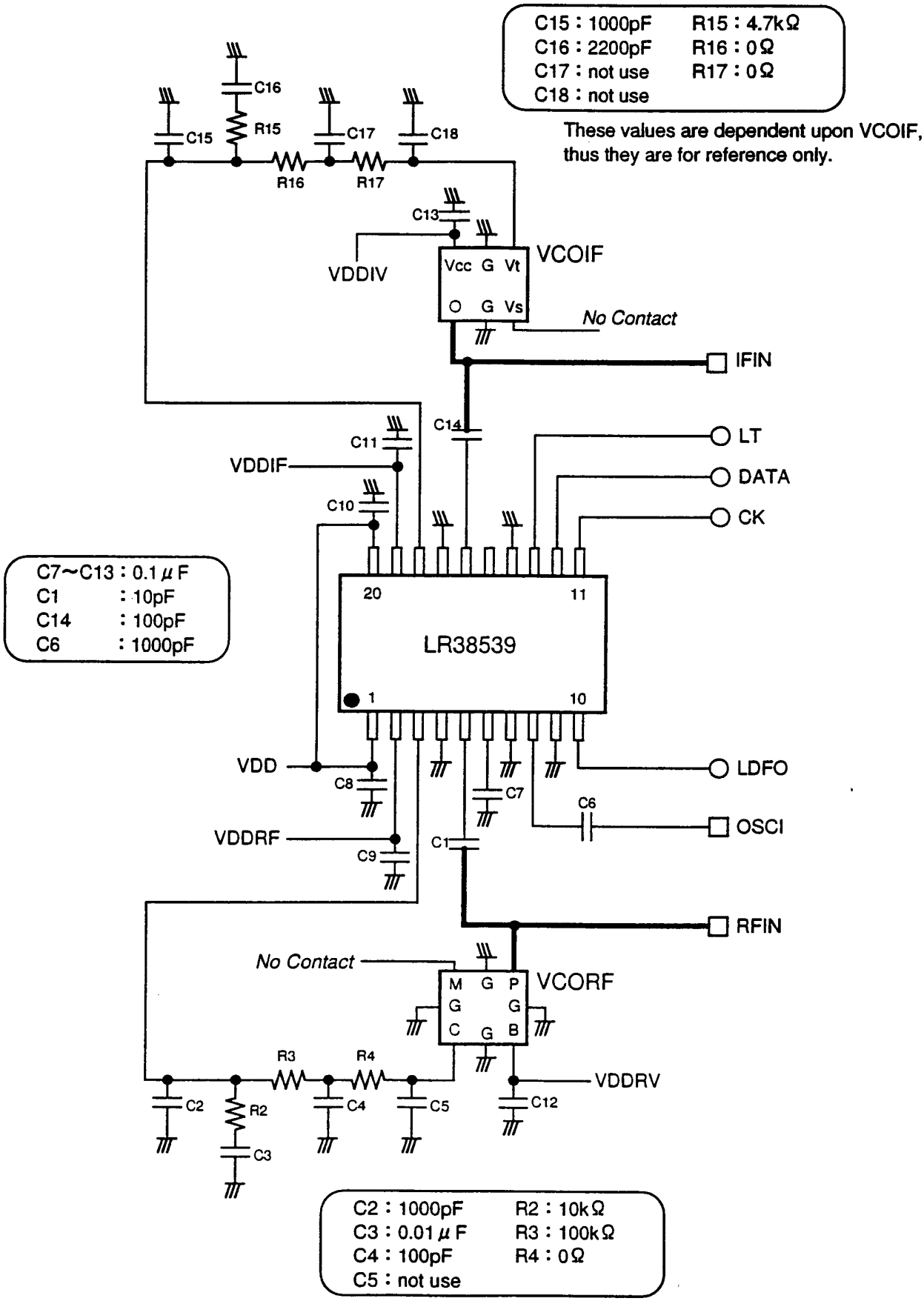
In LR38539 "H" level output voltage are detected in the "Lock" condition. In this point LR38539 is similar to LMX2332L but the latter has "L" spike as shown in the following figure.



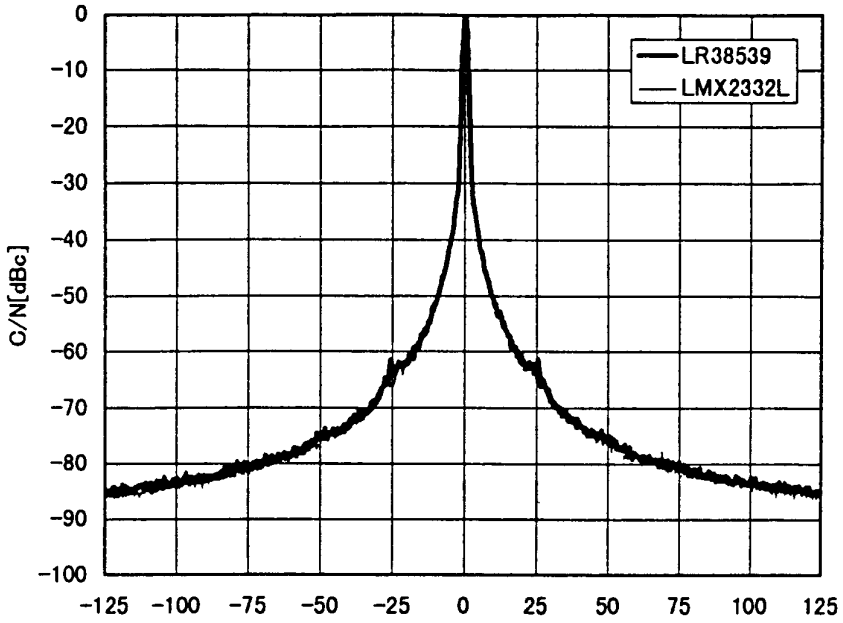
2)

	LR38539(Sharp)	LMX2332L(NS)
Fast lockup mode	N	Y
IF swallow counters (N7,N6,N5)	Should be set either (0,0,0) or (1,1,1)	Don't care
Powerdown operation	Asynchronous powerdown mode	Selectable synchronous or asynchronous powerdown mode
Power for internal counter in powerdown mode	OFF	ON

LR38539 Eva. Board



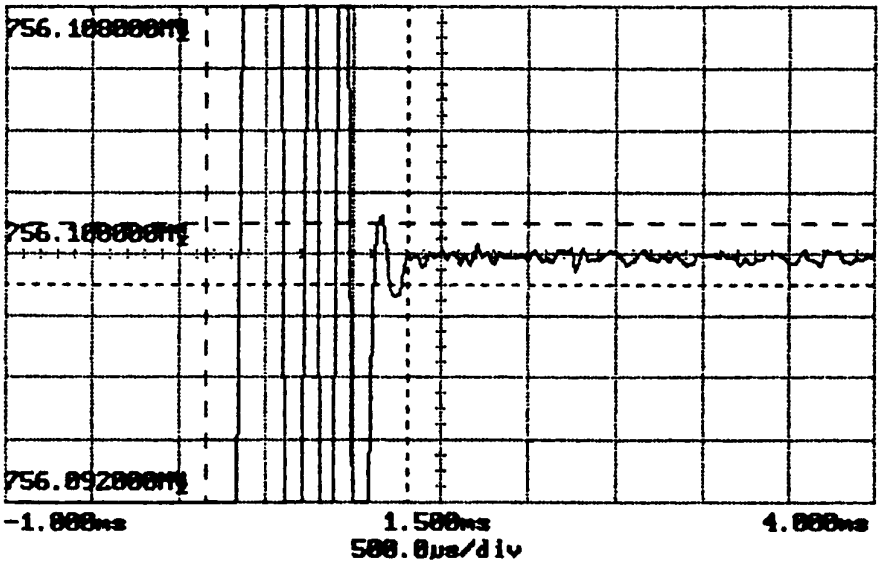
Phase Noise



CENTER:756.1MHz SPAN:250kHz RBW:1kHz VBW:10Hz

REFERENCE FREQUENCY:25kHz

Lock Up Time 741.1MHz→756.1MHz 1.151msec



Phase Lock Loop, PLL, RF, IF, Cellular Phone, LR38539