

MNLM124-X REV 1A2

Original Creation Date: 07/07/95

Last Update Date: 05/24/01

Last Major Revision Date: 05/21/01

LOW POWER QUAD OPERATIONAL AMPLIFIER

General Description

The LM124 consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 can be directly operated off of the standard +5Vdc power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ± 15 Vdc power supplies.

Industry Part Number

LM124

Prime Die

LM1902

NS Part Numbers

 LM124E/883
 LM124J/883
 LM124W/883
 LM124WG/883

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Internally frequency compensated for unity gain.
- Large DC voltage gain. 100dB
- Wide bandwidth (unity gain) 1MHz
(temperature compensated)
- Wide power supply range:
 - Single supply 3V or 32V
 - or dual supply $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (700uA) - essentially independent of supply voltage.
- Low input biasing current 45nA
(temperature compensated)
- Low input offset voltage 5mV
and offset current 5nA
- Input common-mode voltage range includes ground.
- Differential input voltage range equal to the power supply voltage.
- Large output voltage swing. 0V to $V+ - 1.5V$

CONTROLLING DOCUMENTS:

LM124E/883	77043012A
LM124J/883	7704301CA
LM124WG/883	7704301XA

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage V+	32Vdc or ± 16 Vdc
Differential Input Voltage	32Vdc
Input Voltage	-0.3Vdc to +32Vdc
Input Current (Note 4) Vin < -0.3Vdc	50mA
Power Dissipation (Note 2)	
CERDIP	1260mW
CERPACK	700mW
LCC	1350mW
CERAMIC SOIC	700mW
Output Short-Circuit to GND (Note 3) (One Amplifier) V+ \leq 15Vdc and TA = 25 C	Continuous
Operating Temperature Range	-55 C \leq Ta \leq +125 C
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C \leq Ta \leq +150 C
Lead Temperature Soldering, (10 seconds)	260 C
Thermal Resistance	
ThetaJA	
CERDIP (Still Air)	103 C/W
(500LF/Min Air flow)	51 C/W
CERPACK (Still Air)	176 C/W
(500LF/Min Air flow)	116 C/W
LCC (Still Air)	91 C/W
(500LF/Min Air flow)	66 C/W
CERAMIC SOIC (Still Air)	176 C/W
(500LF/Min Air flow)	116 C/W
ThetaJC	
CERDIP	19 C/W
CERPACK	18 C/W
LCC	24 C/W
CERAMIC SOIC	18 C/W
Package Weight (Typical)	
CERDIP	TBD
CERPACK	TBD
LCC	TBD
CERAMIC SOIC	410mg
ESD Tolerance (Note 5)	250V

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
- Note 3: Short circuits from the output to V_+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40mA independent of the magnitude of V_+ . At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
- Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc (at 25 C).
- Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{cc}	Power Supply Current	V ₊ = 5V				1.2	mA	1, 2, 3
		V ₊ = 30V				3.0	mA	1
						4.0	mA	2, 3
I _{sink}	Output Sink Current	V ₊ = 15V, V _{out} = 200mV, +V _{in} = 0V, -V _{in} = +65mV			12		μA	1
		V ₊ = 15V, V _{out} = 2V, +V _{in} = 0V, -V _{in} = +65mV			10		mA	1
					5		mA	2, 3
I _{source}	Output Source Current	V ₊ = 15V, V _{out} = 2V, +V _{in} = 0V, -V _{in} = -65mV				-20	mA	1
						-10	mA	2, 3
I _{os}	Short Circuit Current	V ₊ = 5V, V _{out} = 0V			-60		mA	1
V _{io}	Input Offset Voltage	V ₊ = 30V, V _{cm} = 0V			-5	5	mV	1
					-7	7	mV	2, 3
		V ₊ = 30V, V _{cm} = 28V			-5	5	mV	1
					-7	7	mV	2, 3
		V ₊ = 5V, V _{cm} = 0V			-5	5	mV	1
					-7	7	mV	2, 3
		V ₊ = 30V, V _{cm} = 28.5V			-5	5	mV	1
CMRR	Common Mode Rejection Ratio	V ₊ = 30V, V _{in} = 0V to 28.5V			70		dB	1
±I _{ib}	Input Bias Current	V ₊ = 5V, V _{cm} = 0V			-150	10	nA	1
±I _{ib}	Input Bias Current	V ₊ = 5V, V _{cm} = 0V			-300	10	nA	2, 3
I _{io}	Input Offset Current	V ₊ = 5V, V _{cm} = 0V			-30	30	nA	1
					-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	V ₊ = 5V to 30V, V _{cm} = 0V			65		dB	1
V _{cm}	Common Mode Voltage	V ₊ = 30V	1			28.5	V	1
			1			28	V	2, 3
A _{vs}	Large Signal Gain	V ₊ = 15V, R _L = 2K Ohms, V _o = 1V to 11V			50		V/mV	4
					25		V/mV	5, 6

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
 DC: All voltages referenced to device ground.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Output Voltage High	V+ = 30V, Rl = 2K Ohms			26		V	4, 5, 6
		V+ = 30V, Rl = 10K Ohms			27		V	4, 5, 6
Vol	Output Voltage Low	V+ = 30V, Rl = 10K Ohms				40	mV	4, 5, 6
		V+ = 30V, Isink = 1uA				40	mV	4
						100	mV	5, 6
		V+ = 5V, Rl = 10K Ohms				20	mV	4, 5, 6
	Channel Separation Amp to Amp Coupling	1KHz, 20KHz	2		80		dB	4

Note 1: Guaranteed by Vio tests.

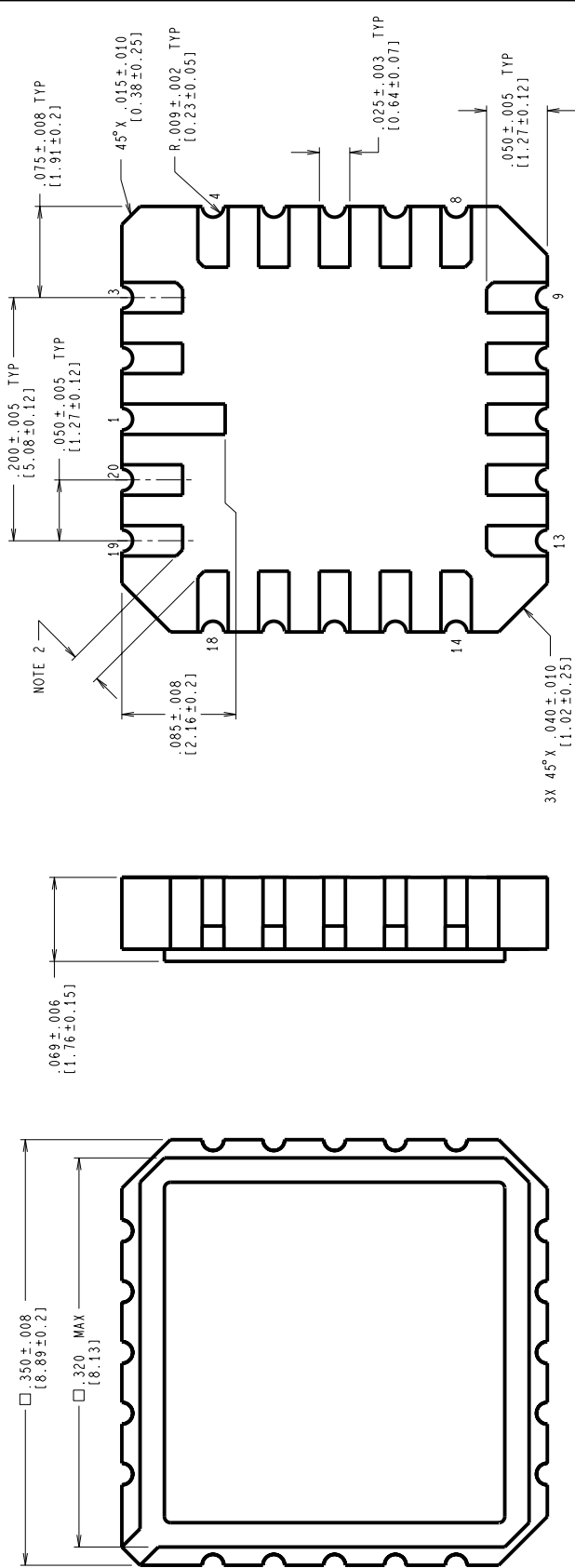
Note 2: Guaranteed, not tested

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05275HRA3	CERPACK (W), 14 LEAD (B/I CKT)
05819HRA2	LDLESS CHIP CARRIER,TYPE C,20 TERMINAL(B/I CKT)
09173HRA2	CERDIP (J), 14 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000254A	(blank)
P000288A	CERDIP (J), 14 LEAD (PINOUT)
P000318B	LCC (E), 20 LEAD (PINOUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

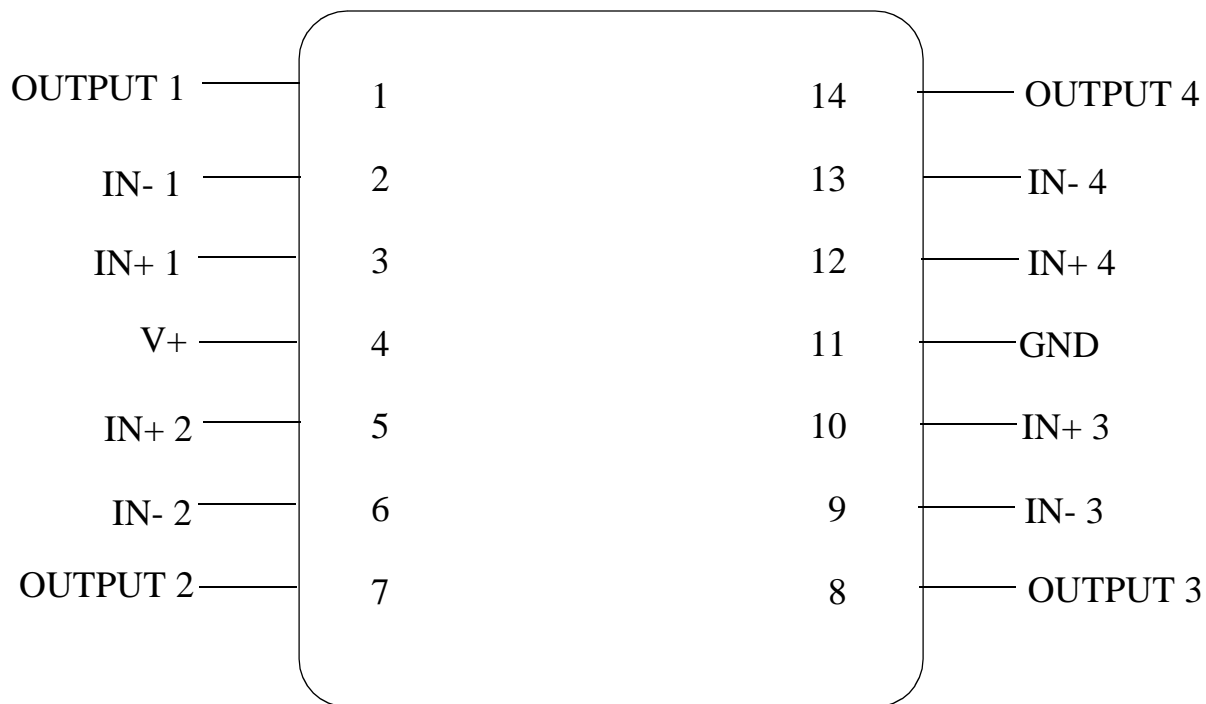
NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

- 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
- SOLDER DIP.
SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
- CORNER PADS MAY HAVE A $45^\circ \times .020 \text{ IN}/0.51 \text{ mm}$ MAXIMUM CHAMFER TO ACCOMPLISH THE $.015 \text{ IN}/0.38 \text{ mm}$ DIMENSION.
- REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO CONFIGURATION CONTROL

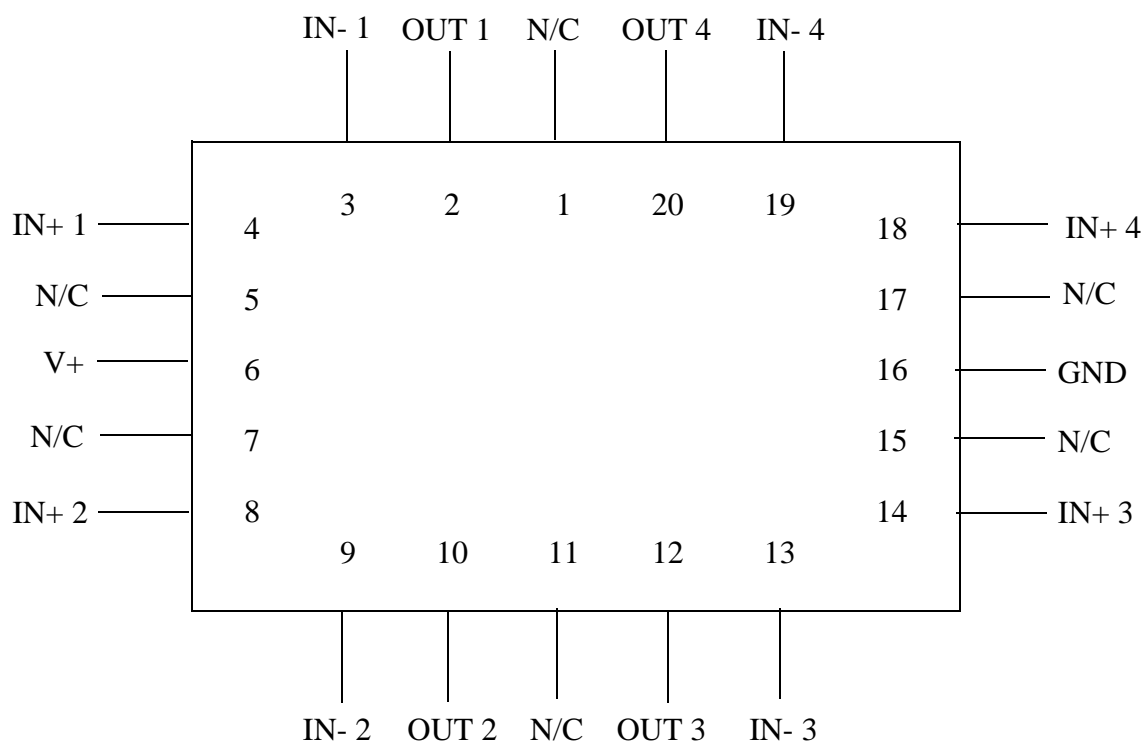
APPROVALS		DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DESIGN	Design Grady	02/10/94	2000 Semiconductor Drive, Santa Clara, CA 95052-8000	
ESTG	CHK		LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL	
ENGR	CHK			
APPROVAL				
PROJECTION			SCALE	SIZE
			N/A	C
			DO NOT SCALE	DRAWING
			MKT-E20A	REV
				E
				SHEET 1 of 1



LM124AJ, LM124J
 14 - LEAD DIP
 CONNECTION DIAGRAM
 TOP VIEW
 P000288A



National Semiconductor™
 MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



LM124AE, LM124E
 20 - LEAD LCC
 CONNECTION DIAGRAM
 TOP VIEW
 P000318B

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
	REVISE AND REDRAW P	10513	07/26/94	DEG/AEP

V .385 MAX
[9.78]

- .005 MIN TYP
[0.12]

14

8

A

.320 ± .010
[8.13 ± 0.25]

X

.250 ± .010
[6.35 ± 0.38]

X

.320 ± .010
[8.13 ± 0.25]

V

.006 ± .002 TYP
[0.15 ± 0.05]
NOTE 2

.045 MAX TYP
[1.14]

.017 ± .002 TYP
[0.43 ± 0.05]
NOTE 2

.009 ± .004
[0.23 ± 0.10]

.050 ± .005 TYP
[1.27 ± 0.12]

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63
SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM
THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS.
SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.

2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS
AFTER LEAD FINISH APPLIED.

3. LEAD 1 IDENTIFICATION SHALL BE:
a) A NOTCH OR OTHER MARK WITHIN THIS AREA
b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

PIN #1 IDENT
NOTE 3

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0002731	08/24/98	Barbara Lopez	Update MDS: MNL124-X Rev. 0B1 to MNL124-X Rev. 0A0. Added WG Package to MDS. Added all required graphics and thermal data.
0B1	M0003008	12/15/98	Rose Malone	Updated MDS: MNL124-X Rev. 0A0 to MNL124-X Rev. 0B1. Updated Burn-In graphics for all packages. Update Pinout for E package. Added Package Weight section.
0B2	M0003114	05/24/01	Rose Malone	Update MDS: MNL124-X, REV. 0B1 to MNL124-X, REV. 0B2.
1A2	M0003809	05/24/01	Rose Malone	Update MDS: MNL124-X, Rev. 0B2 to MNL124-X, Rev. 1A2. Moved Controlling Document information to Features Section. Updated Absolute Maximum Ratings Section. CHANGED Electrical Section: Isink Conditions FROM: V+ = 15V, Vout = 200V, TO: V+ = 15V, Vout = 200V, +Vin = 0mV, -Vin = +65mV AND: V+ = 15V, Vout = 2V, TO: V+ = 15V, Vout = 2V, +Vin = 0mV, -Vin = +65mV. Isource Condition FROM: V+ = 15V, Vout = 2V, TO: V+ = 15V, Vout = 2V, +Vin = 0V, -Vin = -65mV.