Dual High Efficiency Synchronous Step-Down Switching Regulators

NOT RECOMMENDED FOR NEW DESIGNS
Contact Linear Technology for Potential Replacement

FEATURES

- **Dual Outputs: 3.3V and 5V, Two Adjustables or Adjustable and 5V**
- **Wide V_{IN} Range: 4V to 40V**
- **Ultra-High Efficiency: Up to 95%**
- **Low Supply Current in Shutdown: 20μA**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over a Wide Output Current Range
- Independent Micropower Shutdown
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Available in Standard 28-Pin SSOP

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC®1267 series are dual synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. The LTC1267 is composed of two separate regulator blocks, each driving a pair of external complementary power MOSFETs at switching frequencies up to 400kHz. The LTC1267 uses a constant off-time current-mode architecture to provide constant ripple current in the inductor and provide excellent line and load transient response.

A separate pin and on-board switch allow the MOSFET driver power to be derived from the regulated output voltage, providing significant efficiency improvement when operating at high input voltage. The output current level is user-programmable via an external current sense resistor.

The LTC1267 series is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

TYPICAL APPLICATION

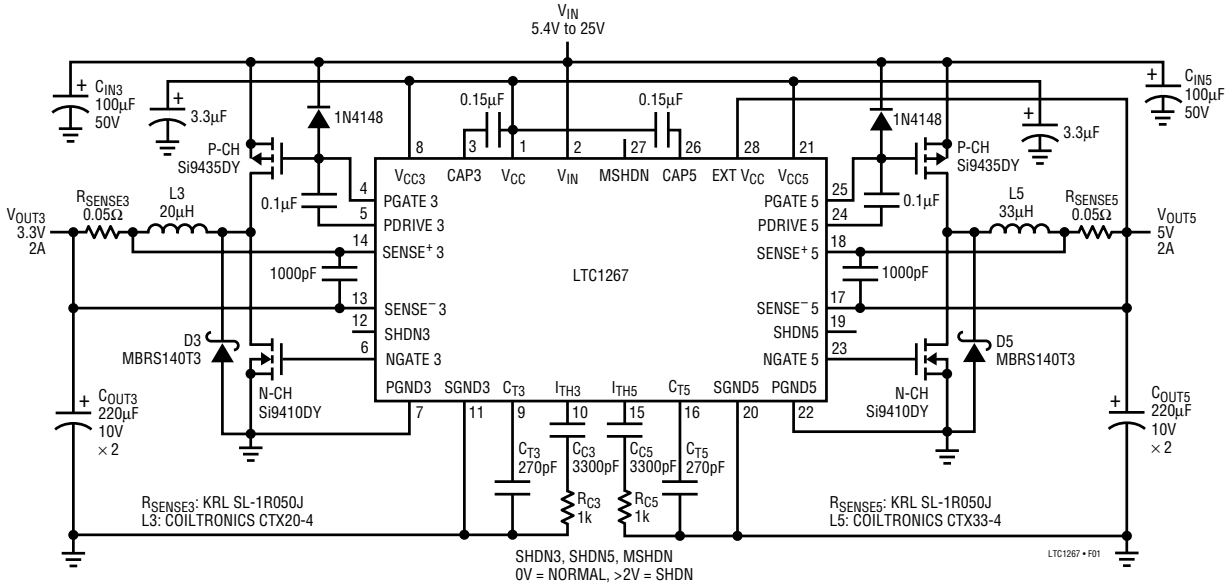
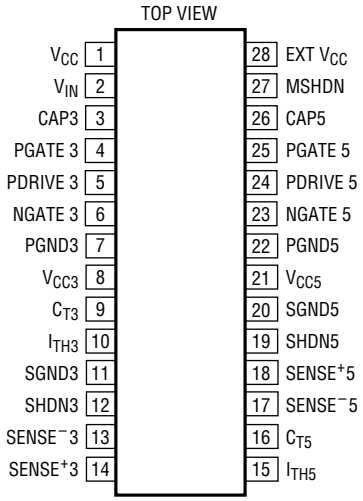


Figure 1. High Efficiency Dual 3.3V, 5V

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –0.3V to 40V
V_{CC} Output Current (Pin 1) 50mA
EXT V_{CC} Input Voltage (Pin 28) 10V
Continuous Output Current (Pins 5, 6, 23, 24) 50mA
Sense Voltages
  LTC1267 (Pins 13, 14, 17, 18) ..... V_{CC} to –0.3V
  LTC1267-ADJ (Pins 12, 13, 17, 18) ..... V_{CC} to –0.3V
  LTC1267-ADJ5 (Pins 12, 13, 17, 18) ... V_{CC} to –0.3V
Shutdown Voltages
  LTC1267 (Pins 12, 19, 27) 7V
  LTC1267-ADJ (Pins 11, 27) 7V
  LTC1267-ADJ5 (Pins 11, 19, 27) 7V
Operating Ambient Temperature Range..... 0°C to 70°C
Extended Commercial
  Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1)..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

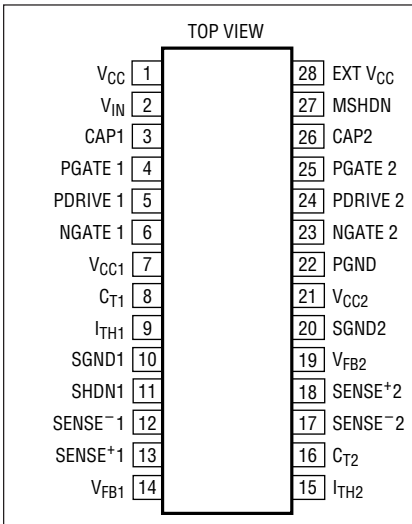


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1267CG

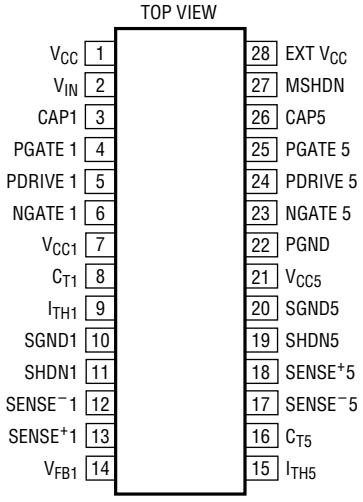


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1267CG-ADJ



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1267CG-ADJ5

Consult factory for Industrial and Military grade parts.
The LTC1267 demo circuit board is now available. Consult factory.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{MSHDN}, $V_{SHDN1,3,5}$ = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FB1,\ 2}$	Feedback Voltage	LTC1267-ADJ, LTC1267-ADJ5: V_{IN} = 9V	●	1.21	1.25	1.29	V
$I_{FB1,\ 2}$	Feedback Current	LTC1267-ADJ, LTC1267-ADJ5	●		0.2	1	µA
V_{OUT}	Regulated Output Voltage						
	3.3V Output	LTC1267: V_{IN} = 9V, I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	5V Output	LTC1267, LTC1267-ADJ5: V_{IN} = 9V, I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 40V		–40	0	40	mV
	Output Voltage Load Regulation	Figure 1 Circuit					
	3.3V Output	5mA < I_{LOAD} < 2.0A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2.0A	●		60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 30V, EXT V_{CC} = 0V, I_{CC} = 10mA	●	4.25	4.5	4.75	V
$V_{IN} – V_{CC}$	V_{CC} Dropout Voltage	V_{IN} = 4V, EXT V_{CC} = Open, I_{CC} = 10mA			200	300	mV
I_{EXTVCC}	EXT V_{CC} Pin Current (Note 3)	EXT V_{CC} = 5V, Sleep Mode			360		µA
I_{IN}	V_{IN} Pin Current (Note 3)						
	Normal	V_{IN} = 12V, EXT V_{CC} = 5V			320		µA
		V_{IN} = 40V, EXT V_{CC} = 5V			550		µA
	Shutdown	V_{IN} = 12V, V_{MSHDN} = 2V			15		µA
		V_{IN} = 40V, V_{MSHDN} = 2V			25		µA
$V_{EXTVCC} – V_{CC}$	EXT V_{CC} Switch Drop	V_{IN} = 12V, EXT V_{CC} = 5V, I_{SWITCH} = 10mA			200	300	mV
$V_{PGATE} – V_{IN}$	PGate to Source Voltage (Off)	V_{IN} = 12V		–0.2	0		V
		V_{IN} = 40V		–0.2	0		V
$V_{SENSE^+_{1,\ 2}} – V_{SENSE^-_{1,\ 2}}$	Current Sense Threshold Voltage	LTC1267-ADJ, LTC1267-ADJ5					
		$V_{SENSE^-_{1,\ 2}}$ = 5.1V, $V_{FB1,\ 2} = V_{OUT}/4$ + 25mV (Forced)			25		mV
		$V_{SENSE^-_{1,\ 2}}$ = 4.9V, $V_{FB1,\ 2} = V_{OUT}/4$ – 25mV (Forced)	●	130	155	180	mV
$V_{SENSE^+_{3,\ 5}} – V_{SENSE^-_{3,\ 5}}$	Current Sense Threshold Voltage	LTC1267					
		$V_{SENSE^-_{3,\ 5}} = V_{OUT}$ + 100mV (Forced)			25		mV
		$V_{SENSE^-_{3,\ 5}} = V_{OUT}$ – 100mV (Forced)	●	130	155	180	mV
V_{SHDN}	Shutdown Threshold						
	MSHDN			0.8	1.4	2.0	V
	SHDN1, 3, 5			0.6	0.8	2.0	V
I_{MSHDN}	MSHDN Input Current	V_{MSHDN} = 5V			12	20	µA
I_{CT}	C_T Pin Discharge Current	V_{OUT} in Regulation		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (PDrive and NGate Pins), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, V_{IN} = 12V, V_{MSHDN}, $V_{SHDN1,3,5}$ = 0V (Notes 2, 5), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FB1,\ 2}$	Feedback Voltage	LTC1267-ADJ, LTC1267-ADJ5: V_{IN} = 9V		1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage 3.3V Output 5V Output	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA		 3.17 4.85	 3.30 5.05	 3.48 5.25	 V V
I_{IN}	V_{IN} Pin Current (Note 3) Normal Shutdown	 V_{IN} = 12V, EXT V_{CC} = 5V V_{IN} = 40V, EXT V_{CC} = 5V V_{IN} = 12V, V_{MSHDN} = 2V V_{IN} = 40V, V_{MSHDN} = 2V		 	 320 550 15 25	 	 µA µA µA µA
I_{EXTVCC}	EXT V_{CC} Pin Current (Note 3)	EXT V_{CC} = 5V, Sleep Mode			360		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, EXT V_{CC} = 0V, I_{CC} = 20mA			4.5		V
$V_{SENSE}^+ - V_{SENSE}^-$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)		 130	25 160	 185	mV mV
V_{MSHDN}	Shutdown Threshold MSHDN			0.8	1.4	2.0	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		3	5	7	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1267/LTC1267-ADJ/LTC1267ADJ5: $T_J = T_A + (P_D \times 95°C/W)$

Note 2: On LTC1267 versions which have MSHDN and SHDN1, 3, 5 pins, they must be at ground potential for testing.

Note 3: The LTC1267 V_{IN} and EXT V_{CC} current measurements exclude MOSFET driver currents. When V_{CC} power is derived from the output via EXT V_{CC}, the input current increases by ($I_{GATECHG}$ × Duty Cycle)/Efficiency. See Typical Performance Characteristics and Applications Information.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

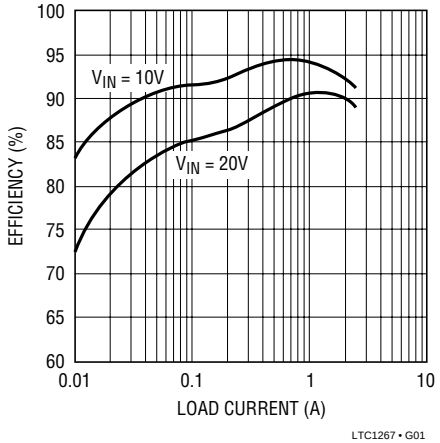
Note 5: The LTC1267/LTC1267-ADJ/LTC1267-ADJ5 are not tested and quality-assurance sampled at –40°C to 85°C. These specifications are guaranteed by design and/or correlation.

Note 6: The logic level power MOSFETs shown in Figure 1 are rated for $V_{DS(MAX)}$ = 30V. For operation at V_{IN} > 30V, use standard threshold MOSFETs with EXT V_{CC} powered from a 9V supply. See applications information.

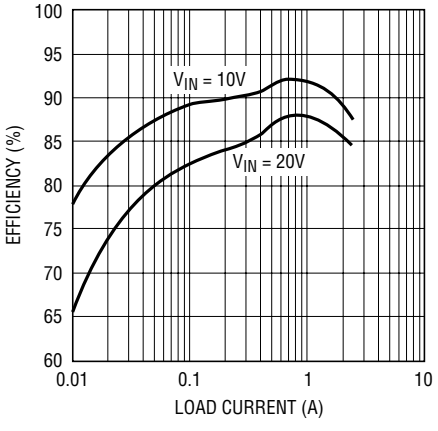
Note 7: LTC1267-ADJ and LTC1267-ADJ5 are tested at an output of 3.3V

TYPICAL PERFORMANCE CHARACTERISTICS

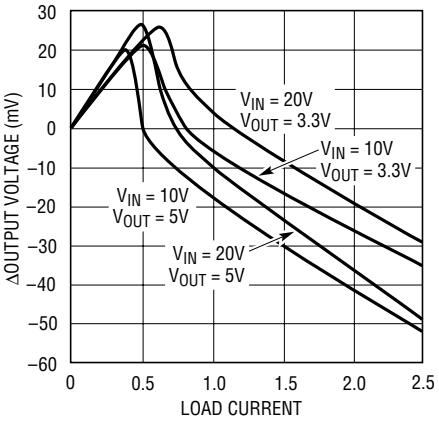
5V Output Efficiency vs Load Current



3.3V Output Efficiency vs Load Current

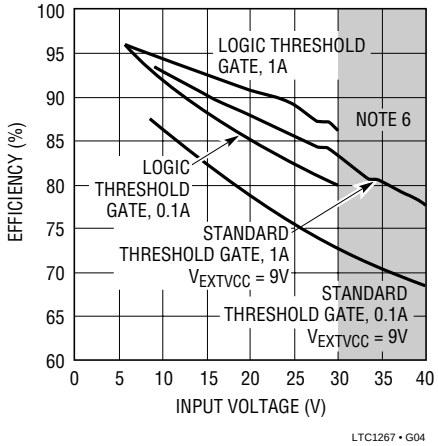


Load Regulation

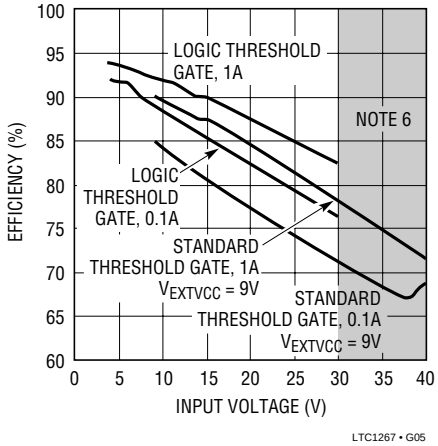


TYPICAL PERFORMANCE CHARACTERISTICS

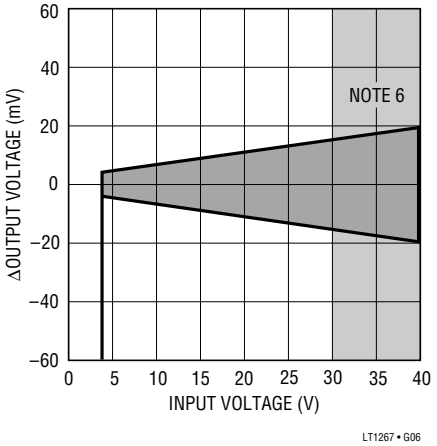
5V Output Efficiency vs Line Voltage



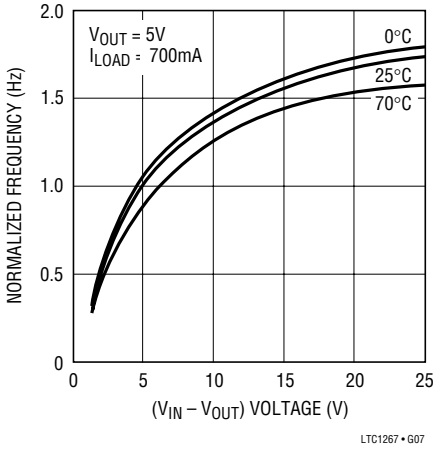
3.3V Output Efficiency vs Line Voltage



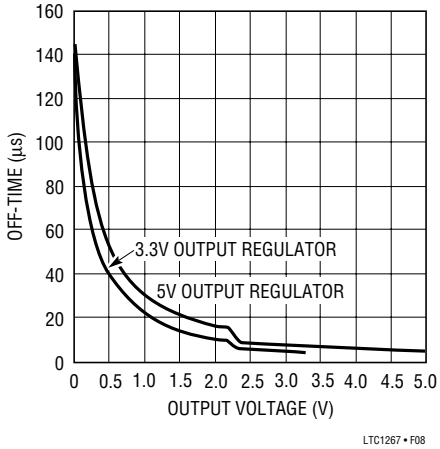
Line Regulation



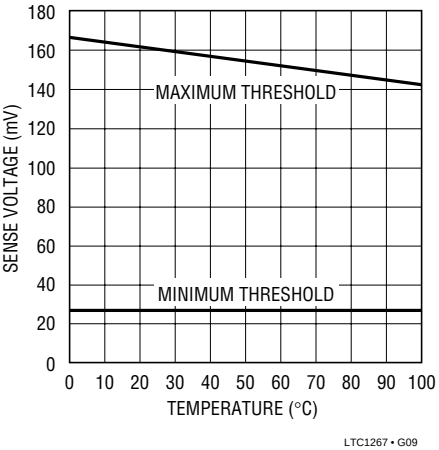
Operating Frequency vs ($V_{IN} - V_{OUT}$)



Off-Time vs Output Voltage



Current Sense Threshold Voltage



PIN FUNCTIONS (Applies to both regulator sections)

V_{IN}: Main Supply Input Pin.

EXT V_{CC}: External V_{CC} Supply for the Regulators. See EXT V_{CC} Pin Connection.

V_{CC}: Output of the Internal 4.5V Linear Regulator, EXT V_{CC} Switch, and Supply Inputs for Driver and Control Circuits. The driver and control circuits are powered from the higher of the 4.5V regulator or EXT V_{CC} voltage. Must be closely decoupled to the power ground.

PGND: Power Ground. Connect to the source of N-channel MOSFET and the (–) terminal of C_{IN}.

SGND: Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGATE: Level Shifted Gate Drive for the Top P-channel MOSFET. The voltage swing at the PGate pin is from V_{IN} to ($V_{IN} - V_{CC}$).

PDRIVE: High Current Gate Drive for the Top P-channel MOSFET. The PDrive pin swings from V_{CC} to GND.

NGATE: High Current Drive for the Bottom N-channel MOSFET. The NGate pin swings from GND to V_{CC}.

PIN FUNCTIONS

CAP: Charge Compensation Pin. A capacitor to V_{CC} provides charge required by the PGate level shift capacitor during supply transitions. The charge compensation capacitor must be larger than the gate drive capacitor.

C_T: External Capacitor. From this pin to ground sets the operating frequency. (The frequency is also dependent upon the ratio V_{OUT}/V_{IN}).

I_{TH} : Gain Amplifier Decoupling Point. The regulator current comparator threshold increases with the I_{TH} pin voltage.

SENSE$^-$: Connects to internal resistive divider which sets the output voltage. The Sense$^-$ pin is also the (–) input of the current comparator.

SENSE$^+$: The (+) Input for the Current Comparator. A built-in offset between the Sense$^+$ and Sense$^-$ pins, in conjunction with R_{SENSE}, sets the current trip threshold.

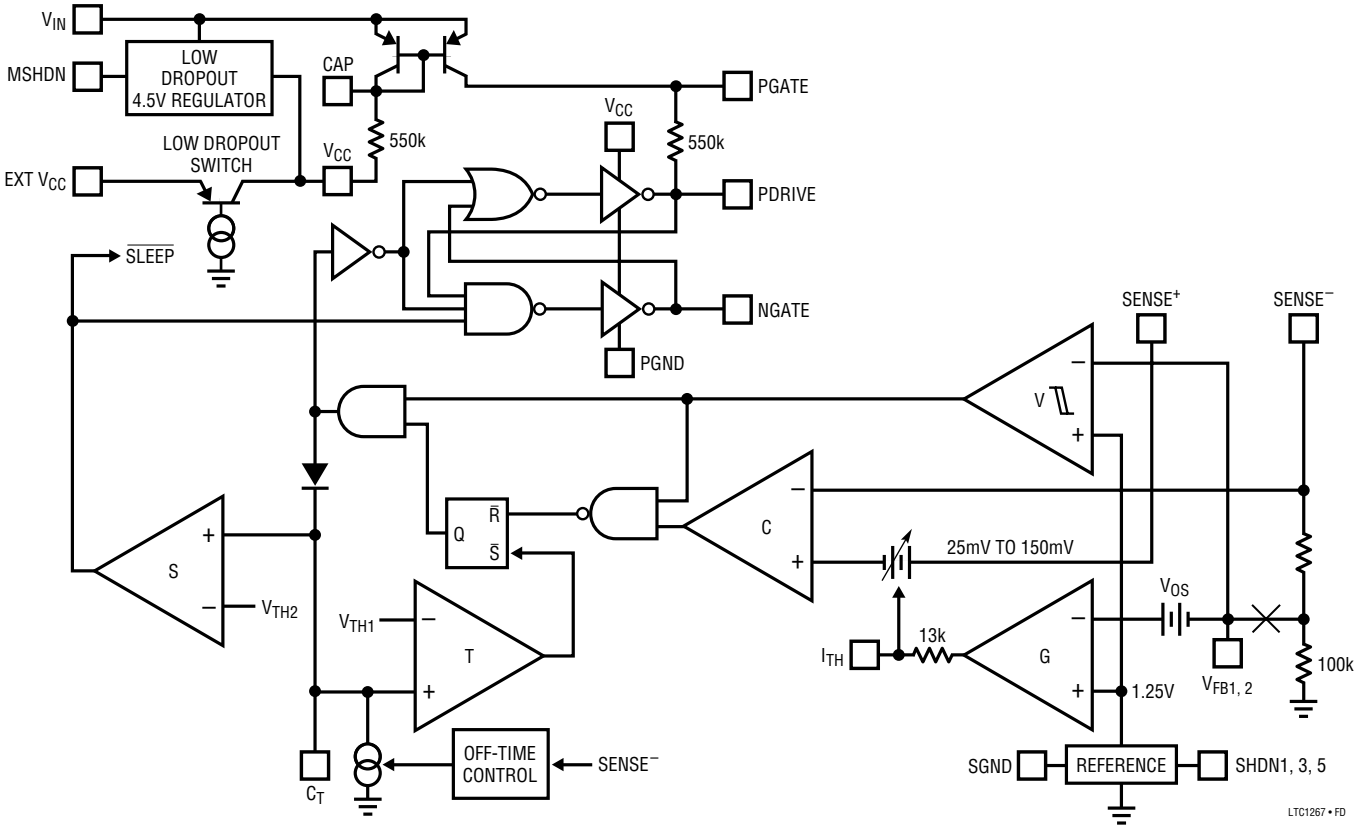
$V_{FB1, 2}$: These pins receive the feedback voltage from an external resistive divider used to set the output voltage of the adjustable section.

MSHDN: Master Shutdown Pin. Taking MSHDN high shuts down V_{CC} and all control circuitry.

SHDN1, 3, 5: These pins shut down the individual regulator control circuitry (V_{CC} is not affected). Taking SHDN1, 3, 5 pins high turns off the control circuitry of adjustable 1, 3.3V, 5V sections and holds both MOSFETs off. Must be at ground potential for normal operation.

FUNCTIONAL DIAGRAM

(Internal divider broken at $V_{FB1,2}$ for adjustable versions. Only one regulator block shown.)



OPERATION (Refer to Functional Diagram)

The LTC1267 series consists of two individual regulator blocks, each using current mode, constant off-time architectures to synchronously switch an external pair of complementary power MOSFETs. The two regulators are internally set to provide output voltages of 3.3V and 5V for the LTC1267. The LTC1267-ADJ is configured to provide two adjustable output voltages, each set by their individual external resistor dividers. The LTC1267-ADJ5 has adjustable and 5V output voltages. Operating frequency is individually set on each section by the external capacitors attached to the C_T pin.

The output voltage is sensed by an internal voltage divider connected to the Sense$^-$ pin or external divider returned to the V_{FB} pin (LTC1267-ADJ, LTC1267-ADJ5). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1267 series automatically switches between two modes of operation, Burst Mode and continuous mode. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

A low dropout 4.5V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry during start-up. During normal operation, the LTC1267 family powers the drivers and control from the output via the EXT V_{CC} pin to improve efficency. The NGate pin is referenced to ground and drives the N-channel MOSFET gate directly. The P-channel gate drive must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the PDrive signal via an internal 550k resistor and an external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Sense$^+$ and Sense$^-$ pins connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the PGate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor C_T is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage to model the inductor current, which decays at a rate that is also proportional to the output voltage. While the timing capacitor is discharging, the NGate output is high, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the NGate output to go low (turning off the N-channel MOSFET) and the PGate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats. As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode a majority of the circuitry is turned off, dropping the quiescent current from several mA (with the MOSFETs switching) to 360μA. The load current is now being supplied by the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the NGate output can go high, the PDrive output must also be high. Likewise, the PDrive output is prevented from going low while the NGate output is high.

APPLICATIONS INFORMATION

The LTC1267 Compared to the LTC1159, LTC1149 and LTC1142 Family

The LTC1267 family is a dual LTC1159. Identical to the LTC1159, the LTC1267 can reduce the quiescent and shutdown currents by making use of an internal switch which allows the driver and control sections to be powered from an external source to improve efficiency.

The basic LTC1267 application circuit shown in Figure 1 is limited to a maximum input voltage of 30V due to external MOSFET breakdown. If the application does not require greater than 18V operation the LTC1142HV should be used.

Component Selection

The basic LTC1267 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and diode are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the adjustable, 3.3V and 5V sections in the LTC1267 are identical, the process of component selection is the same for both sections.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1267 current comparators have a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1267 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1267 works well with values of R_{SENSE} from 0.02Ω to 0.2Ω. Figure 2 shows the selection of R_{SENSE} vs maximum output current.

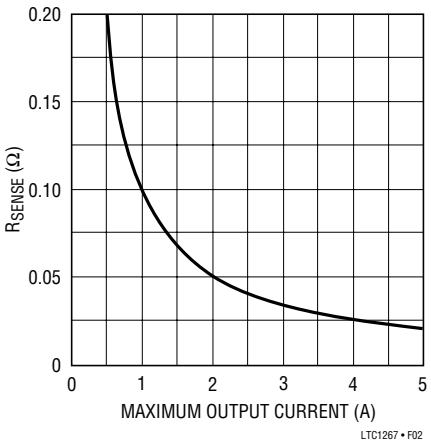


Figure 2. Selecting R_{SENSE}

The load current below which Burst Mode operation commences, I_{BURST} and the peak short-circuit current $I_{SC(PK)}$ both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1267 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

C_T and L Selection for Operating Frequency

Each regulator section of the LTC1267 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. The value of C_T is calculated from the desired continuous mode operating frequency (f_O):

$$C_T = \frac{7.8 \times 10^{-5}}{f_O}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T vs frequency including the effects of input voltage is given in Figure 3.

APPLICATIONS INFORMATION

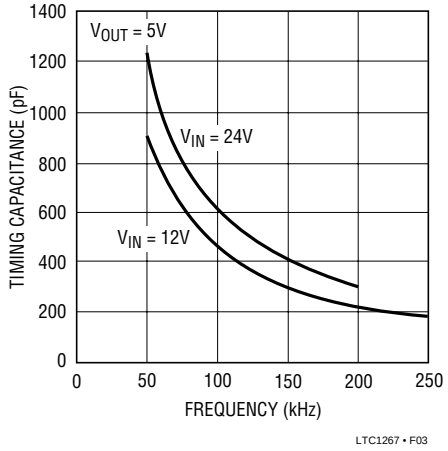


Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

$$f_O = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T$$

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $0.025V/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{OUT}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the LTC1267 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy (MPP), or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down but copper I^2R losses increase. For additional information regarding inductor selection, please refer to the LTC1159 data sheet.

Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with each section of the LTC1267: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch.

The peak-to-peak gate drive levels are set by the V_{CC} voltage on the LTC1267. This voltage is typically 4.5V during start-up and 5V to 7V during normal operation (see EXT V_{CC} Pin Connection). Consequently, *logic-level threshold MOSFETs must be used in most LTC1267 family applications*. The only exceptions are applications in which EXT V_{CC} is powered from an external supply greater than 8V, in which standard threshold MOSFETs ($V_{GS(TH)}$ > 4V) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1267 is operating in continuous mode, the duty cycles for the two MOSFETs are given by:

$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Channel Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET dissipations at maximum output current are given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta_P) R_{DS(ON)} + k (V_{IN})^2 (I_{MAX}) (C_{RSS}) f_O$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta_N) R_{DS(ON)}$$

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Where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses, while the P-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The N-channel MOSFET losses are the greatest at high input voltage or during a short circuit when the N-channel duty cycle is nearly 100%.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.007/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant k = 5 can be used for the LTC1267 to estimate the relative contributions of the two terms in the P-channel dissipation equation.

The Schottky diodes D3 and D5 shown in Figure 1 only conduct during the dead-time between the conduction of the respective power MOSFETs. The sole purpose of D3 and D5 is to prevent the body diode of the N-channel MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D3 and D5 are omitted). Therefore, D3 and D5 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$ where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF ceramic capacitor is also required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required Effective Series Resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1267:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon, United Chemicon, and Sprague should be considered for high performance capacitors. In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. For additional information regarding capacitor selection, please refer to the LTC1159 data sheet.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip

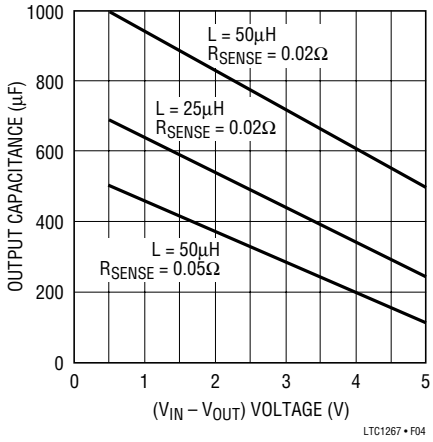

Figure 4. Minimum Suggested C_{OUT}

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the voltage comparator. This causes Burst Mode operation to be activated when the LTC1267 would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

EXT V_{CC} Pin Connection

The LTC1267 contains an internal PNP switch connected between the EXT V_{CC} and V_{CC} pins. The switch closes and supplies the V_{CC} power whenever the EXT V_{CC} pin is higher in voltage than the 4.5V internal regulator. This allows the MOSFET driver and control power to be derived from the output during normal operation and from the internal regulator when the output is out of regulation (start-up, short circuit).

Significant efficiency gain can be realized by powering V_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For LTC1267, LTC1267-ADJ or LTC1267-ADJ5 this simply means connecting the EXT V_{CC} pin directly to V_{OUT} of the 5V regulator.

The following list summarizes the four possible connections for EXT V_{CC}:

1. EXT V_{CC} left open. This will cause V_{CC} to be powered only from the internal 4.5V regulator, resulting in reduced MOSFET gate drive levels and an efficiency penalty of up to 10% at high input voltages.
2. EXT V_{CC} connected directly to highest V_{OUT} of the two regulators. This is the normal connection for LTC1267/LTC1267-ADJ/LTC1267-ADJ5 and provides the highest efficiency.
3. EXT V_{CC} connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXT V_{CC} to an output-derived voltage which has been boosted to greater than 4.5V. This can be done either with the inductive boost winding shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics and generally provides the highest efficiency at the expense of a slightly higher parts count.

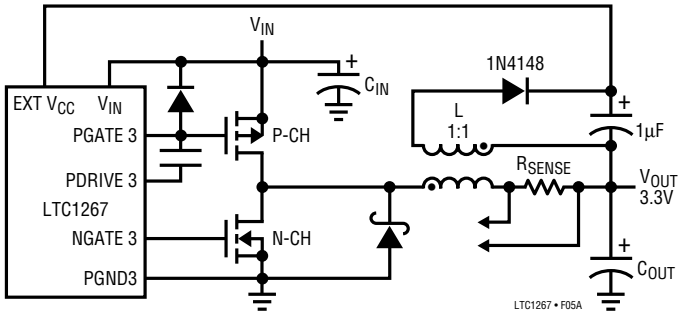

Figure 5a. Inductive Boost Circuit for EXT V_{CC}

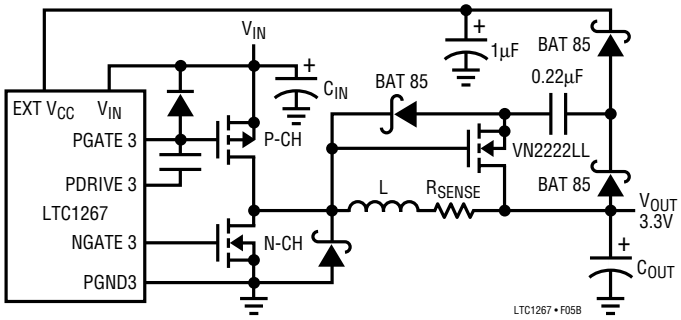

Figure 5b. Capacitive Charge Pump for EXT V_{CC}

4. EXT V_{CC} connected to an external supply. If an external supply is available in the 5V to 10V range it may be used to power EXT V_{CC} providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.

   Under the condition that EXT V_{CC} is connected to V_{OUT1} which is greater than 5.5V, to power down the whole regulator, both the pins MSHDN and SHDN1 have to be pulled high. If SHDN1 is left floating or grounded the EXT V_{CC} may self-power from V_{OUT1}, preventing complete shutdown.

LTC1267 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1267-ADJ and LTC1267-ADJ5 adjustable versions are used with an external resistive divider from V_{OUT} to the $V_{FB1,2}$ pins. This is shown in Figure 6. The regulated voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) 1.25V$$

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The $V_{FB1, 2}$ pin is extremely sensitive to pickup from the inductor switching node. Care should be taken to isolate the feedback network from the inductor and a 100pF capacitor should be connected between the $V_{FB1, 2}$ and SGND pins next to the package.

The circuit in Figure 6 cannot be used to regulate a V_{OUT} which is greater than the maximum voltage allowed on the LTC1267 EXT V_{CC} pin (10V). In applications with $V_{OUT} > 10V$, R_{SENSE} must be moved to the ground side of the output capacitor and load. This operates the current sense comparator at 0V common mode, increasing the off-time approximately 40% and requiring the use of a smaller timing capacitor C_T.

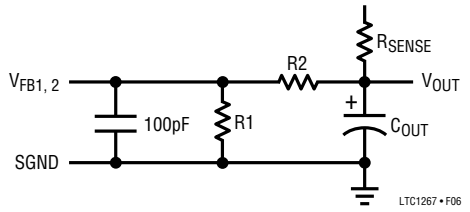

Figure 6. LTC1267-ADJ/LTC1267-ADJ5 External Feedback Network

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits, only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1267 circuits:

1. LTC1267 V_{IN} current
2. LTC1267 V_{CC} current
3. I^2R losses
4. P-channel transition losses

1. LTC1267 V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} currents results in a small (<1%) loss which increases with V_{IN}.

2. LTC1267 V_{CC} current is the sum of the MOSFET driver and control circuits currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} which is typically much larger than the control circuit current. In continuous mode $I_{GATECHG} \approx f_O(Q_P + Q_N)$, where Q_P and Q_N are the gate charges of the two MOSFETs.

   By powering EXT V_{CC} from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of V_{CC} current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.1\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4. Transition losses apply only to the P-channel MOSFET and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 5 \times V_{IN}^2 \times I_{MAX} \times C_{RSS} \times f_O$$

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time,

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and inductor core losses, generally account for less than 2% total additional loss.

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1267 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 7. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

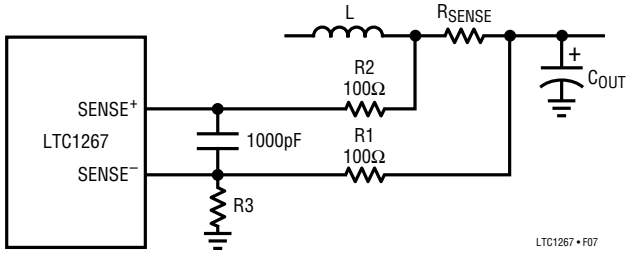


Figure 7. Suppressing Burst Mode Operation

With the addition of R3 a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be reduced:

$$R_{SENSE} \approx \frac{75}{I_{MAX}}\ m\Omega$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Sense$^+$ and Sense$^-$ pins.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1267. These items are also illustrated graphically in the layout diagram of Figure 8. In general each block should be self-contained with little cross coupling for best performance. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1267 signal ground must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1267 Sense$^-$ pin connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications the resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between the two Sense pins should be as close as possible to the LTC1267. Up to 100Ω may be placed in series with each Sense lead to help decouple the Sense pins. However, when these resistors are used the capacitor should be no larger than 1000pF.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1μF ceramic capacitor between V_{IN} and power ground may be required in some applications.
5. Is the V_{CC} decoupling capacitor connected closely between the V_{CC} pins of the LTC1267 and power ground? This capacitor carries the MOSFET driver peak currents.

APPLICATIONS INFORMATION

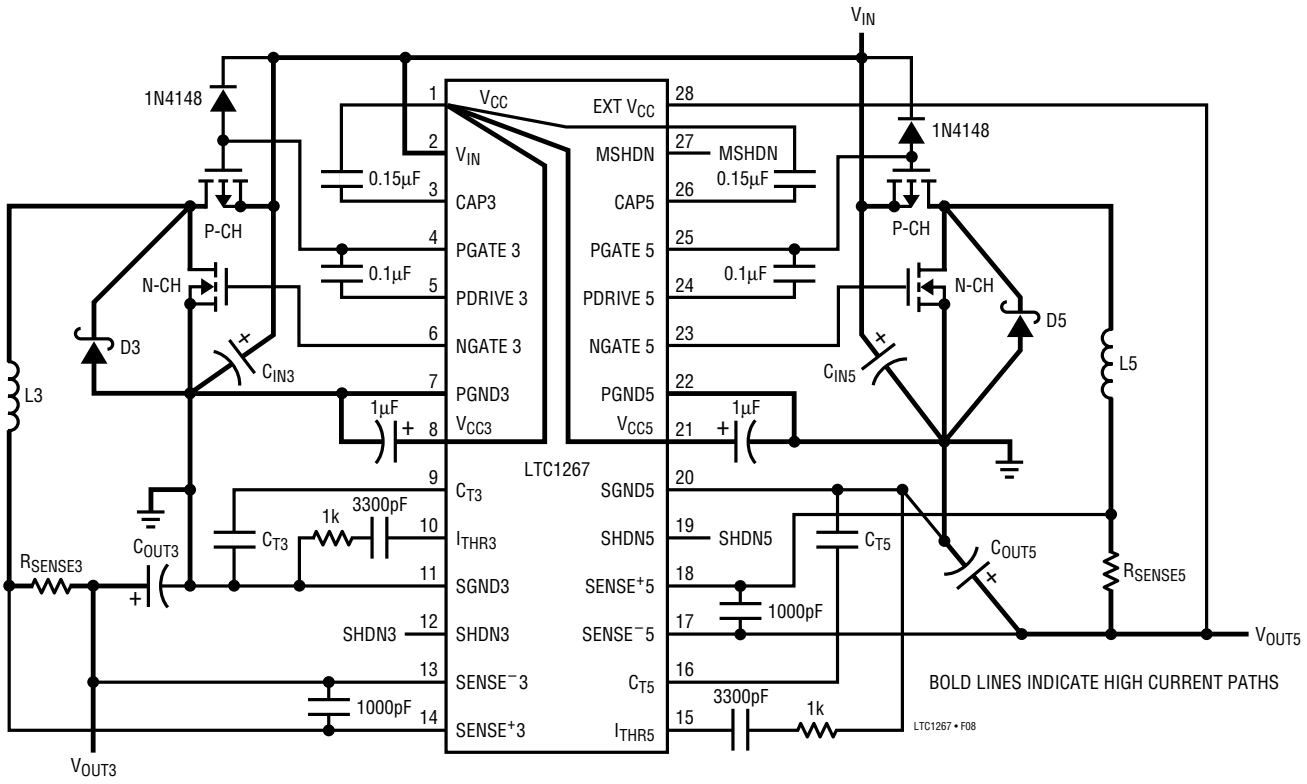


Figure 8. LTC1267 Layout Diagram

6. In adjustable versions, the feedback pin is very sensitive to pickup from the switch node. Care must be taken to isolate $V_{FB1, 2}$ from possible capacitive coupling of the inductor switch signal.
7. Are MSHDN and SHDN1, 3, 5 actively pulled to ground during normal operation? These shutdown pins are high impedance and must not be allowed to float.

Troubleshooting Hints

Since efficiency is critical to LTC1267 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pin.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 9b.

If the C_T is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

Inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

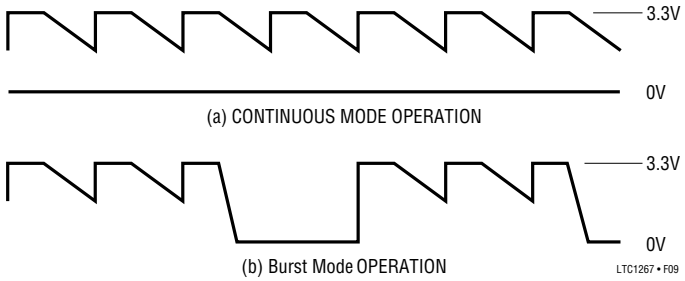
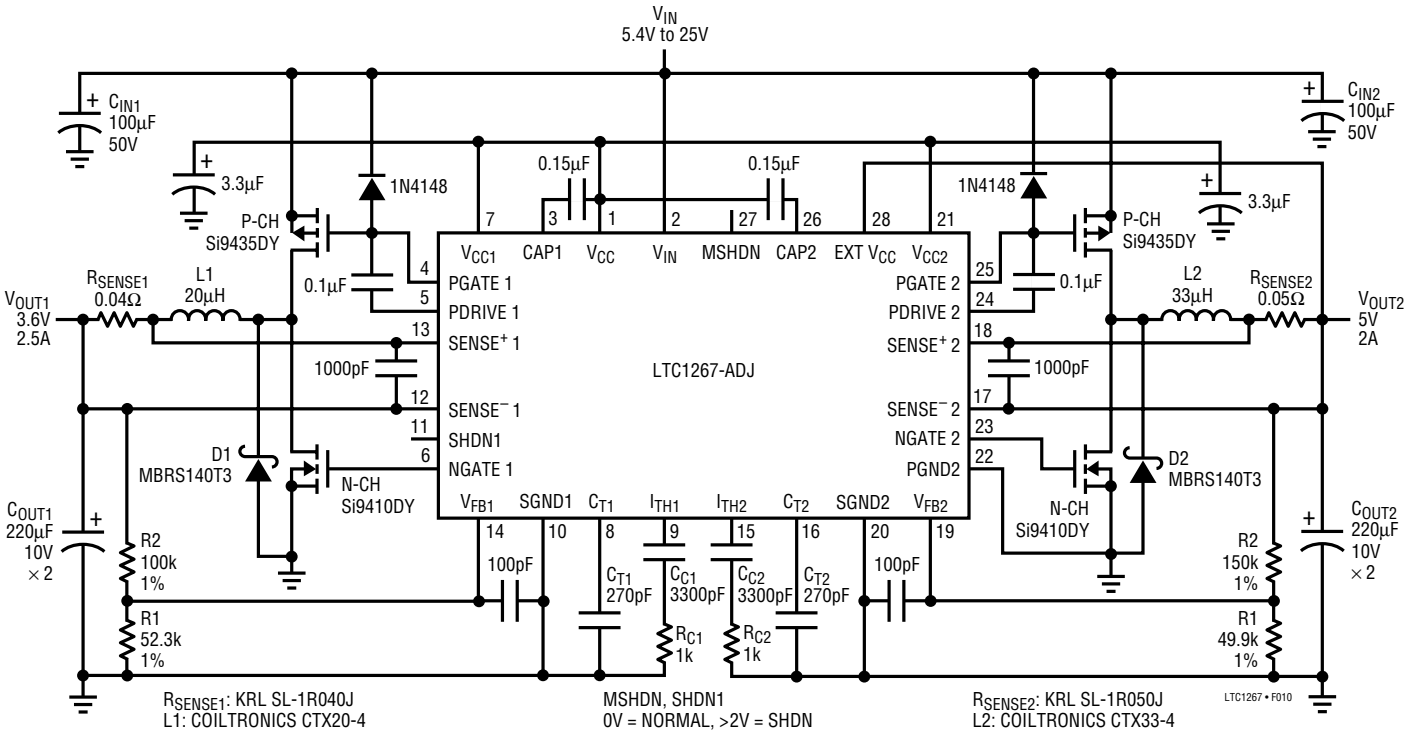


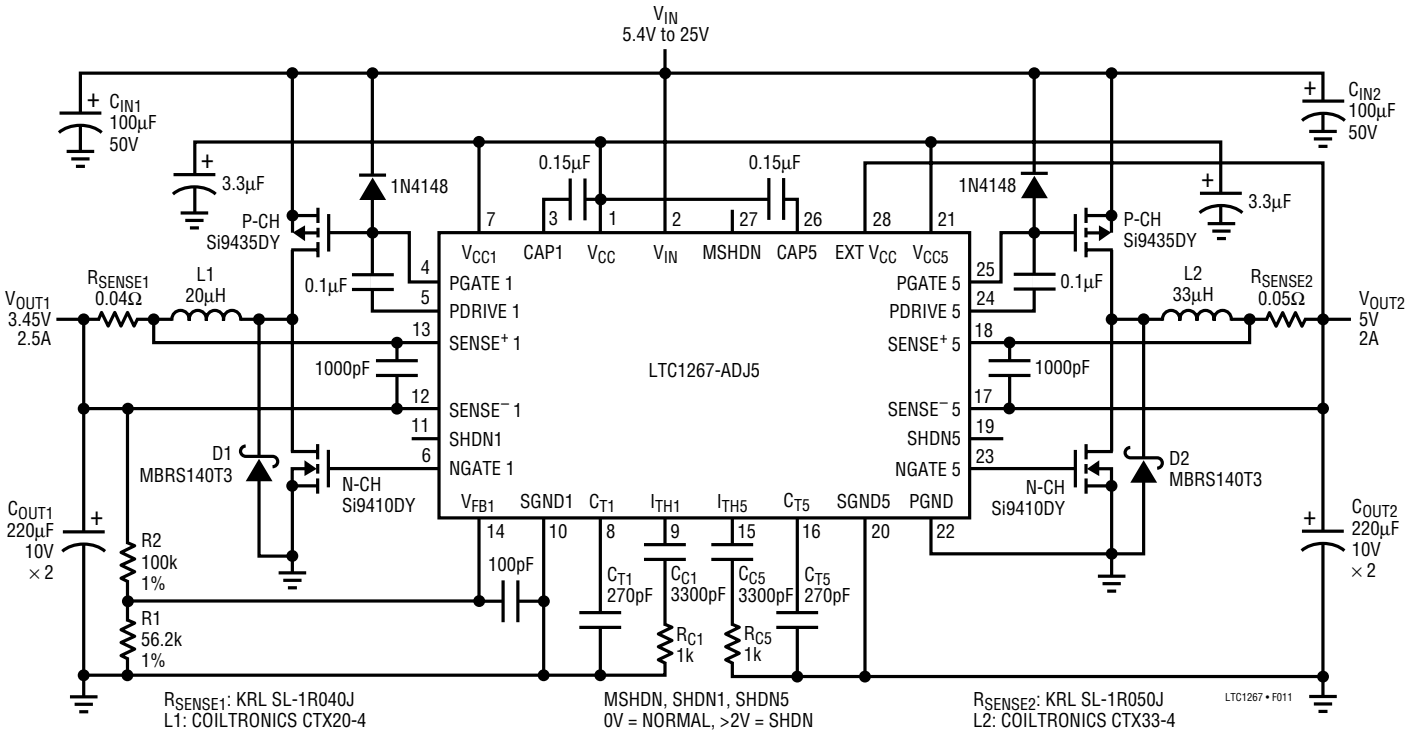
Figure 9. C_T Waveforms

TYPICAL APPLICATIONS

LTC1267-ADJ Dual Regulator with 3.6V/2.5A and 5V/2A Outputs



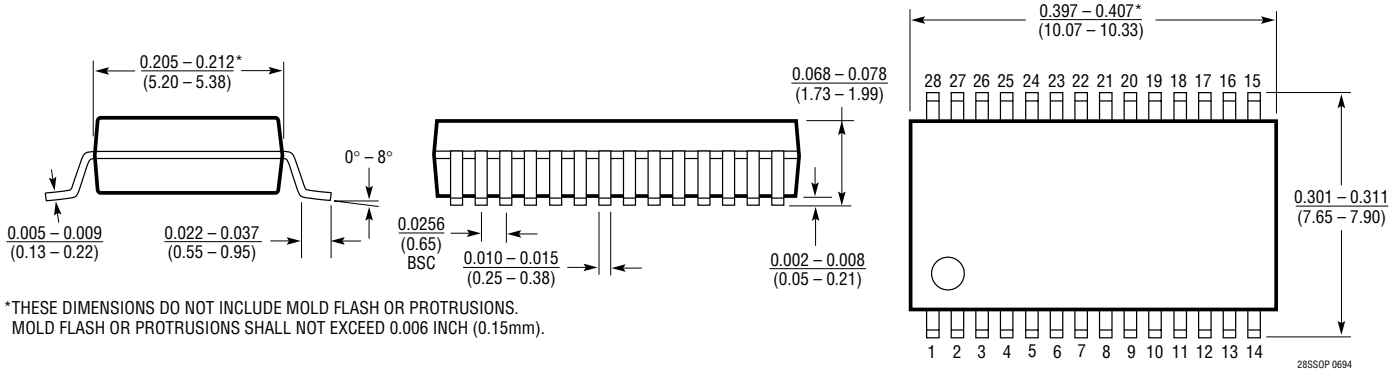
LTC1267-ADJ5 Dual Regulator with 3.45V/2.5A and 5V/2A Outputs



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1148
LTC1143	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	Step-Down Switching Regulator Controller	Nonsynchronous, 8-Pin, $V_{IN} \leq 16V$
LTC1148	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
LTC1159	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, for Logic Level FETs
LTC1174	Step-Down Switching Regulator with Internal 0.5A Switch	$V_{IN} \leq 18.5V$, Comparator/Low Battery Detector
LTC1265	Step-Down Switching Regulator with Internal 1A Switch	$V_{IN} \leq 13V$, Comparator/Low Battery Detector
LTC1266	Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/Low Battery Detector
LTC1574	Step-Down Switching Regulator with Internal 0.5A Switch and Schottky Diode	$V_{IN} \leq 18.5V$, Comparator

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