L64021
MPEG-2 Digital Video Disk Decoder

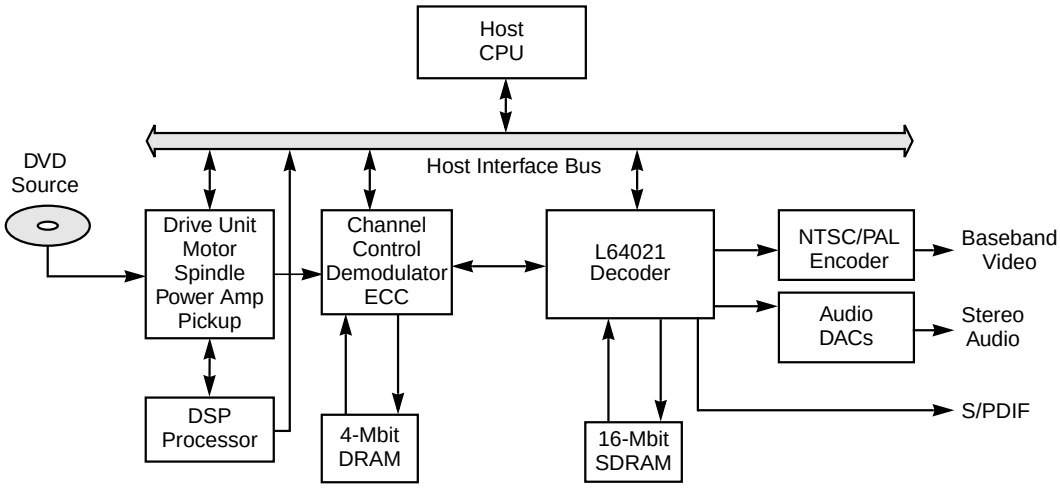
Preliminary Datasheet

The L64021 DVD Audio/Video Decoder balances high integration and low cost in a single chip design that delivers quality and performance for DVD systems. LSI Logic's integrated MPEG-2, Dolby Digital (AC-3) core provides full support for both consumer-based DVD players and DVD PC applications. Backward compatible with both existing CD-ROM and Video CD formats, the L64021 enables designers to develop low-cost next generation DVD systems.

The L64021 extends the capabilities of LSI Logic's time-tested and market-proven MPEG-2 decoders by integrating licensed Content Scrambling System (CSS) technology. The integrated CSS unit provides secure authentication and descrambling of protected DVD content. At the same time, the L64021 maintains low processor overhead and low system cost.

The L64021 DVD A/V Decoder receives coded audio, video, and private data to produce decoded audio/video output with subpicture graphics overlay. LSI Logic has optimized the input/output interfaces for low cost integration into any number of DVD system architectures. The block diagram in Figure 1 illustrates an L64021 DVD system implementation.

Figure 1 DVD System Block Diagram



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LSI Logic's digital video architecture for the L64021 incorporates many unique features and capabilities. These architectural elements include flexible preparsing for system streams, processing up to the sequence layer, a flexible display controller, 24-bit/96-kHz Linear PCM support, and a multitap filter. Video features include a host of programmable, high quality trick play modes. LSI Logic's programmable trick play provides system designers the flexibility to develop unique features for easy product differentiation.

The L64021 Decoder is available in a 160-pin plastic quad flat package (PQFP) that is compatible with the other members of the LSI Logic decoder family. The L64021 is manufactured using a 0.25 micron low-power CMOS process and is available in a 3.3-V version.

Features

Video Decoding

- Includes an embedded RISC Processor
- Integrates studio quality MPEG-2 video decoder
- Fully complies with Main Profile at Main Level MPEG-2 standard, ISO 13818-2
- Decodes MPEG-2 bitstreams, including MPEG-2 program stream, with private stream support
- Decodes an MPEG-1 bitstream as defined in ISO IS 11172, including the MPEG-1 system layer
- Operates at image sizes up to CCIR601 resolution of 720 x 480 pixels @ 30 fps for NTSC and 720 x 576 @ 25 fps for PAL

Audio Decoding

- Several audio output options available:
  - PCM through the CD Bypass (2 ch.)
  - Decoded PCM from MPEG, LPCM, or AC-3 (2 ch.)
  - AC-3 coded stream with multichannel extensions (5.1 ch.)
  - MPEG coded stream with multichannel extensions (7 ch.)

- Combines MPEG and Dolby Digital audio decoding with support for Linear PCM data
- Decodes dual channel MPEG audio, Layer I and II ISO 11172-3 supporting bit rates of 8–448 Kbps and sampling rates of 16, 22.05, 24, 32, 44.1, and 48 kHz
- Decodes 5.1 channel Dolby Digital, downmixing to 2 outputs over the entire range of compliant bit rates and sampling rates
- Supports Linear PCM streams with sample rates of 48 and 96 kHz
- Supports Dolby Pro Logic downmix

Data and Error Handling Capabilities

- Up to 20-Mbits/s sustained input channel Adata rate
- Input data format: 8-bit parallel through dedicated channel interface output: 8-bit (Y, Cb, Cr) in slave mode
- Complete on-chip channel buffer and display buffer controls
- Error concealment maintains display of images during channel errors
- Mute on error for concealment in audio decoder
- No external microcode or external logic required

Video Display and Graphics Support

- Integrates a flexible 4, 16, or 256-color on-screen display (OSD) controller
- Allows connection to an external OSD generator
- Programmable display management
- Programmable channel buffer and display buffer size
- Slave video timing operation
- Supports trick modes commonly needed in DVD systems
- Integrates postprocessing filters for image resizing (horizontal and vertical)
- Integrates vertical filter for letterbox format display
- Implements subpicture data processing on-chip
- Implements 3:2 pulldown directly from the bitstream

- Supports pan and scan with 1/8 pixel accuracy from the bitstream
- Supports 4:2:0 to 4:2:2 sampling filters
- 16-level alphablending for OSD

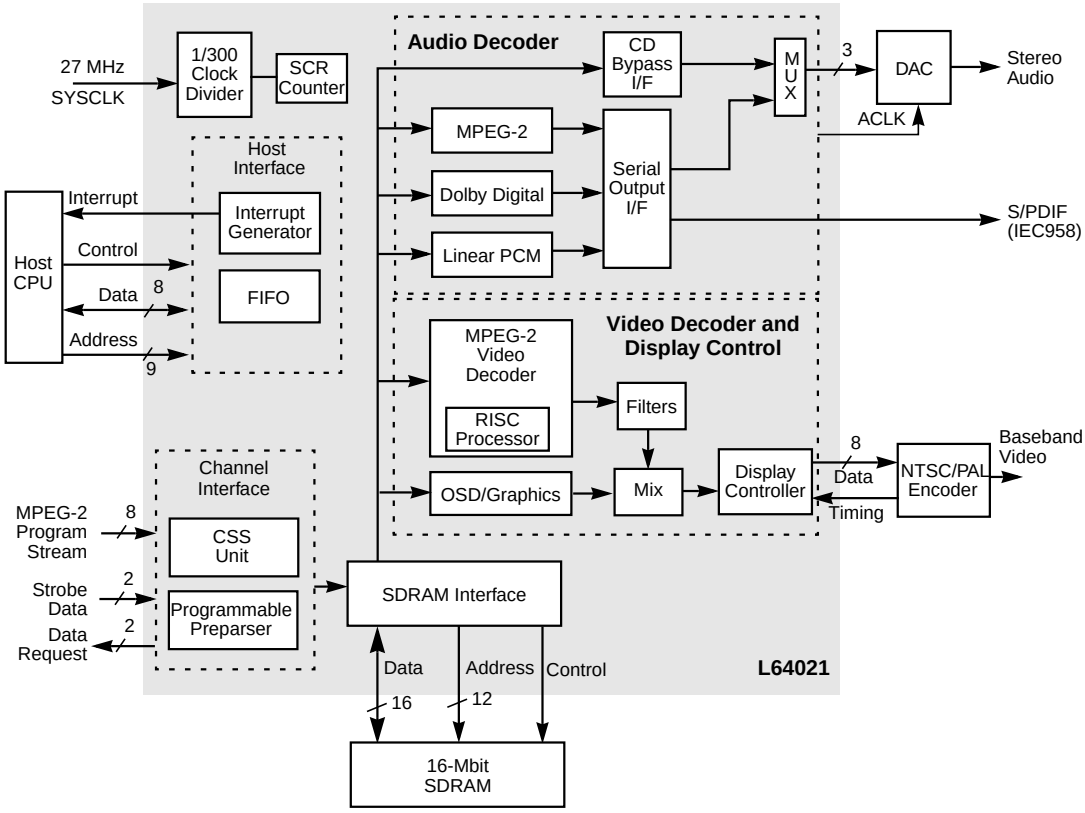
Cost Effective System Implementation

- Programmable preparser accepts PES, ES, and PS streams
- Directly connects to commodity SDRAM
- Input/output interfaces are optimized for glueless integration into consumer video systems
- Channel interface includes an embedded Content Scramble System (CSS) Unit for A/V descrambling and key authentication.
- Operates from a single 27-MHz clock, with additional audio sample clock input
- Total external memory required for audio and video decoding: 16-Mbit SDRAM for CCIR601 resolution
- Interfaces to Intel or Motorola 8-bit Host CPU for initialization, testing, and status monitoring
- Directly interfaces to off-the-shelf NTSC/PAL encoders
- Directly interfaces to off-the-shelf audio DACs
- 160-pin PQFP package
- Low power 3.3-V process
- TTL-compatible I/O pins

Functional Description

Figure 2 provides a block diagram of the L64021's major functional units. An overview of the major functions of the L64021 follows the diagram.

Figure 2 L64021 Block Diagram



Video and Audio Decoding

The L64021 can decode separate video and audio elementary streams, A/V PES streams (from transport decoders), and program elementary stream (PES) containing both audio, video, and private 1 and 2 streams. In addition, the PES decoding can parse critical headers for both Presentation Time Stamp (PTS) and Decoding Time Stamp (DTS) information necessary for video and audio synchronization.

Video Decoding

This section includes a description of the major components involved in handling and decoding video:

- Video Decoder
- Video Postprocessing Filters and Letterbox Display
- On-Screen Display with Graphics Support and SPU Decoder

Video Decoder

The L64021 operates optimally at image sizes up to 720 x 480 pixels, with a frame rate of 30 fps for NTSC (or 720 x 576 @ 25 fps for PAL). The L64021 can also decode MPEG-1 sequences. The coded data channel may have a sustained bit rate of up to 20 Mbit/s. The L64021 also supports images with resolution lower than 720 x 480 pixels (see Video Postprocessing Filters).

Video Postprocessing Filters and Letterbox Display

Images with resolutions below 720 x 480 pixels are interpolated to full size using on-chip filters. This allows programming produced at different resolutions to be decoded and displayed on televisions with standard NTSC or PAL timing, and it allows the use of digital or analog NTSC or PAL encoders operating at standard television frequencies (typically 27 MHz). In addition, the filters provide the capability to pan and scan the MPEG image to 1/8-pixel accuracy. The L64021 also supports letterbox display format with an integrated vertical filter for 3/4 decimation (720 x 480 images are decimated to 720 x 360 pixels).

On-Screen Display Controller with Graphics Support and SPU Decoder

The L64021 integrates an on-screen display (OSD) controller capable of overlaying an image up to 720 x 480 pixels (720 x 576 for PAL) at up to 8 bits/pixel on top of an MPEG video sequence while it is being decoded. In addition, the L64021 contains an on-chip Subpicture Unit (SPU) decoder for cost-effective integration of the graphics function. The SPU decodes the bit map for graphic overlay and executes SPU instructions so the graphic display can be changed on the fly without CPU intervention.

Audio Decoding

The L64021 integrates an MPEG (Musicam) and Dolby Digital audio decoder with support for Linear PCM audio. It can decode two channels of MPEG audio Layer I or Layer II over the full range of compliant bit rates and sample rates. It also can decode 5.1 channels of Dolby Digital and downmix this information to two channels of audio output over the full range of compliant bit rates and sample rates. The audio decoder uses the same memory as the video decoder for its channel buffers—which eliminates the need for extra SDRAM found in other nonintegrated audio solutions.

External Interfacing

The L64021 includes the following external interfaces:

- Host Interface
- Channel Interface
- Memory Interface
- Video Output
- Audio Output
- Audio Input

Host Interface

A stand-alone, dedicated host interface allows the user to program a variety of options and monitor the operation of the L64021. In addition, through this port you can read user data that is present in the data channel and read errors flagged by the L64021. The device does not maintain unread user data indefinitely. The host interface includes a FIFO to which no more data can be written once the FIFO becomes full. Subsequent data will be lost. The system controller must read data transmitted in the user data records of the MPEG bitstream, even if that data is subsequently used to control some aspect of the video display subsystem. The controller must read this data, then write it to the L64021 internal state registers, if necessary. The host interface also allows you to read and write data into the memory for OSD and channel buffer access.

Channel Interface

The L64021 includes an independent parallel interface for direct connection to upstream error correction devices. The interface uses simple signal handshaking for compressed stream transfer to the decoder.

The L64021's channel interface handles the incoming coded data, which is assumed to be an MPEG-2 compliant bitstream, and provides error detection, reporting, CSS content descrambling, and disk/title key authentication. The channel interface detects data in the bitstream that does not meet MPEG-2 or Dolby Digital syntax or grammar rules and can flag the data for exception processing.

Hardware error handling includes error masking and the application of concealment vectors in video. Audio error concealment includes muting on errors and searching for error-free frames. The channel interface flags gross errors in the bitstream that are due to channel buffer overrun or underrun or to nonconformance in the bitstream. The error flagging is done so the errors can be masked in the display or in the audio output. To handle gross errors, you can program an external microcontroller with an error recovery mechanism.

The L64021 channel interface also includes a fully integrated CSS unit that provides on-core disk/title key authentication and A/V descrambling. The CSS unit can be run in one of five modes: bypass, data key extraction, A/V descrambling, authentication and disk key extraction, or authentication and title key decryption mode.

Memory Interface

The L64021 supports direct connection to commercial SDRAM for use as frame stores, channel buffers, and overlay memory. The L64021 uses frame stores for intermediate frame reconstruction and display, separate video and audio channel buffers for rate matching, and zero or more regions for graphic overlays. This storage is combined into a single, contiguous memory space accessed over a 16-bit wide bus. In most cases, this is one 1M x 16-bit SDRAM, for a total memory space of 2 Mbytes.

The interface between the L64021 and SDRAM requires no external components. The L64021 pinout allows connection to the SDRAM to be made on a single PCB layer. During normal operation, the L64021

exclusively controls the SDRAM frame stores. However, it is possible to access the SDRAM through the host port on the L64021 for test, for verification, and for access to the overlay stores and channel information.

Video Output

The L64021 provides a digitized video output for subsequent display. This data is in the CCIR601 (Y, Cb, Cr) color space. The video output operates with a luminance sample rate that is always exactly half the device clock—nominally 13.5 MHz from a 27-MHz input clock. The L64021 can accept external synchronization signals in slave mode. The L64021 supports a number of trick modes specific to the needs of DVD systems, including freeze frame, skip B pictures, skip B and P pictures, and search for GOP.

Audio Output

The audio decoder produces a serial PCM output that is compatible with most commercial audio DACs. The audio decoder includes circuitry to maintain the correct audio output sample rate based upon an external audio clock. The decoder also provides an audio oversampling output clock to the external audio DAC; this audio output clock is selected from one of the audio clock inputs. In addition, the decoder supports the IEC958 output format for PCM samples, transporting compressed Dolby Digital bitstreams, and MPEG-2 multichannel extensions.

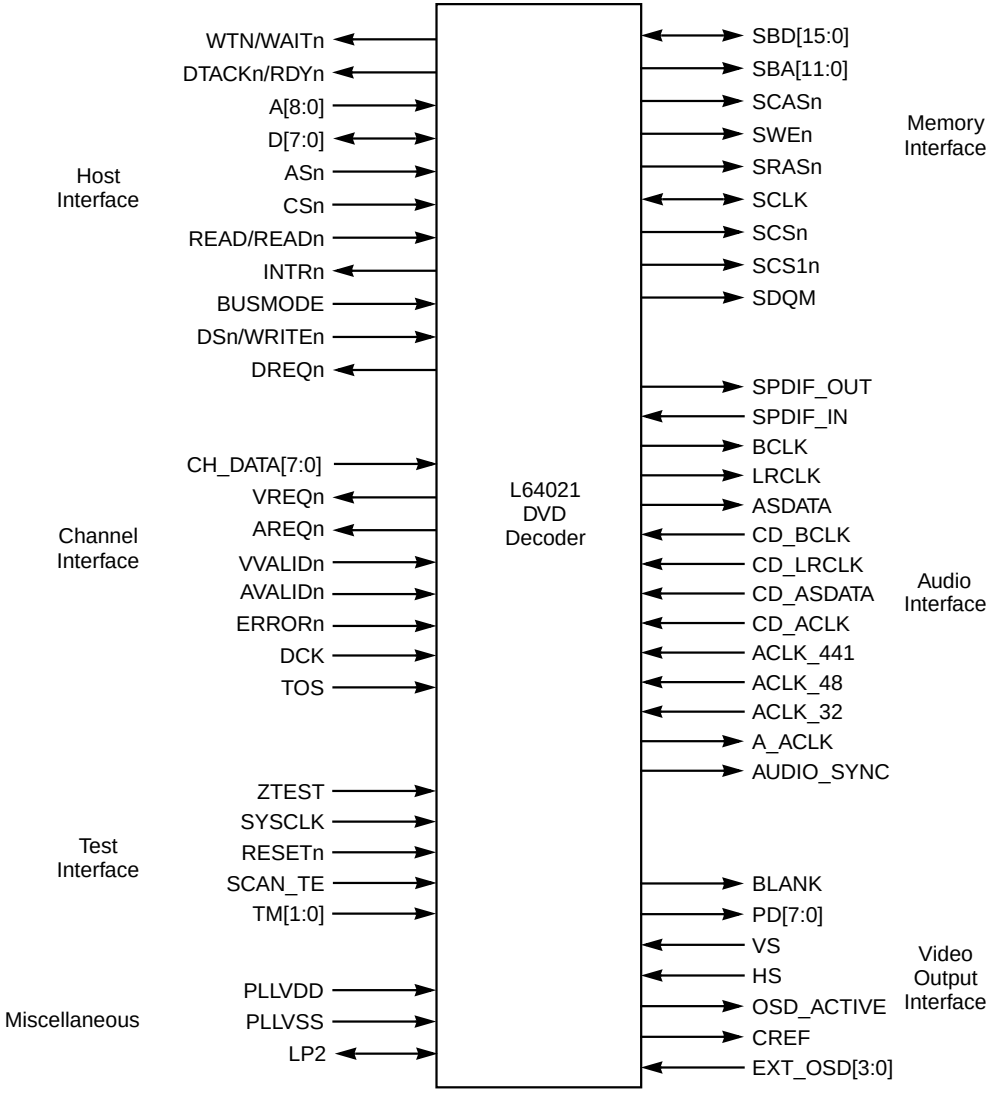
Audio Input

The L64021 supports several audio input modes. It supports connection to a Sony/Philips Digital Interface Format (S/PDIF) input that can be routed directly to the S/PDIF output. The device also handles input signals that can be connected directly from a CD-ROM player to the PCM output.

Signal Descriptions

This section provides detailed information on the L64021 signals. The signal descriptions are useful for hardware designers who are interfacing the L64021 with other devices. Figure 3 shows the logic symbol for the L64021. Signals that end in an “n” are active LOW. Otherwise, it is active HIGH.

Figure 3 L64021 Logic Symbol



The L64021 has six major signal interfaces:

- Host Interface on page 11
- Channel Interface on page 14
- Memory Interface on page 15
- Video Output Interface on page 16
- Audio Interface on page 17
- Miscellaneous and Test Interfaces on page 19

Host Interface

A[8:0] **Address Bus** **Input**
This 9-bit address line provides access to the L64021's internal registers. The address value on these lines is latched on the falling edge of ASn (Motorola) or on the falling edge of READn/WRITEn (Intel).

ASn **Address Strobe (Motorola Mode only)** **Input**
This signal latches (in the L64021) the address currently on the A[8:0] bus. The address latches on the falling edge of the ASn signal. ASn also indicates the start and end of a bus cycle transaction. ASn LOW and CSn LOW indicate the start of a bus transaction. The rising edge of ASn indicates the end of a bus transaction.

BUSMODE **Controller Select Pin** **Input**
This signal specifies whether the Host CPU is an Intel or a Motorola microprocessor. When HIGH, the Motorola mode is selected. When LOW, the Intel mode is selected. The Motorola processor uses one pin to specify read and write transfers. The Intel processor uses two separate pins to specify read and write transfers. Please see the DSn signal definition below.

CSn **Chip Select (Motorola and Intel Mode)** **Input**
This active-LOW signal indicates an attempt by an external host CPU to access the L64021 either for a read or a write bus cycle. The event of CSn LOW and ASn LOW indicates the start of a bus transaction in Motorola mode. The CSn LOW and READn LOW or WRITEn LOW indicates the start of a bus cycle in Intel mode. The actual transaction type (either read or write) is determined by

the READ polarity (Motorola type interface) or by READn and WRITEn polarity (Intel type interface). The end of a bus cycle is determined by the rising edge of ASn (Motorola) or the rising edge of READn or WRITEn (Intel). CSn may stay active LOW for more than one bus transaction cycle.

D[7:0] **Host Data Bus** **Bidirectional**

This host data bus is an 8-bit bidirectional data line used for data communication between the host CPU and the L64021. During a read bus cycle, D[7:0] carries valid information from an internal L64021 register. DTACK or WAITn indicate when the data on the host data bus is valid. The rising edge of WRITEn (Intel) or DSn (Motorola) indicates to the L64021 when to strobe the data into the chip.

DREQn **DMA Transfer Request** **Output**

This signal is an active-LOW output that indicates when the decoder is ready to receive a new byte of DMA data. The decoder is considered ready when the interface is ready and the internal write FIFO is not full, or if the internal read FIFO is not empty. If these conditions are not met, DREQn is not asserted. The maximum transfer rate over this interface is 20 Mbit/s.

DTACKn **Data Acknowledge (Motorola)**
RDYn **RDYn (Intel)** **3-State Output**

This signal is active LOW when used as DTACKn (Motorola mode). When used as RDYn (Intel mode), this signal is active LOW.

When used as DTACKn, the L64021 drives this signal LOW to indicate to the external host CPU that the current bus transaction can be completed. The signal is 3-stated if CSn is not active. L64021 drives DTACKn HIGH when it is not ready to end the bus cycle, and it drives DTACKn LOW when it is ready to end the bus cycle.

When used as RDYn, the L64021 drives this signal LOW to indicate to the external host CPU that the L64021 is ready to complete the current bus transaction. The L64021 drives RDYn HIGH when the L64021 is not ready. The signal is 3-stated if CSn is not active.

INTRn **Interrupt** **OD Output**

This signal is an active-LOW interrupt output. It has an open drain. The L64021's host interface drives this signal LOW to send an interrupt to the Host CPU.

DSn **Data Strobe (Motorola)**

WRITEn **WRITEn (Intel)** **Input**

DSn (Motorola mode) indicates when the CPU strobes the data in or out of the L64021. During a read bus cycle, the start of a read transaction is triggered when DSn, CSn, and ASn are all LOW. During a write bus cycle, the rising edge of DSn indicates when the L64021 latches the data present on D[7:0].

When WRITEn (Intel mode) is LOW it indicates that the external host CPU is performing a write bus cycle. READ/READn must be HIGH during a write cycle. CSn LOW indicates that the host CPU is attempting to write to the L64021's internal registers. The address is registered on the falling edge of READn. On the rising edge of WRITEn, the L64021 latches the data present on D[7:0].

READ **Read/Write Strobe (Motorola)**

READn **READn (Intel)** **Input**

READ (Motorola mode) indicates whether the current bus cycle is a read or write. When READ is HIGH, a read bus cycle is in progress. When READ is LOW, a write bus cycle is in progress. CSn must be LOW for the CPU to access the L64021.

READn (Intel mode) is LOW when the external CPU is performing a bus read cycle. WRITEn must be HIGH during a read cycle. When both CSn and READn are LOW, the host CPU is reading from the L64021's internal registers. The address is registered on the falling edge of READn.

WTN **Device Wait (Motorola)**

WAITn **Device Wait (Intel)** **3-State Output**

This signal is 3-state or active LOW when used as a WAITn signal. It may be used to interface to processors other than Motorola and Intel host CPUs. The signal's function is similar to DTACKn/RDYn (described earlier); however, the polarity is inverted. The L64021 drives this signal HIGH to indicate to the external host CPU that the current transaction can be completed. The signal is

3-stated if CSn is not active. The L64021 drives the signal LOW when it is not ready to end the bus cycle, and drives the signal HIGH when it is ready to end the bus cycle.

Channel Interface

AREQn **Audio Transfer Request** **Output**

When the L64021 asserts this signal LOW, it indicates that the L64021 is ready to receive a new byte of coded audio data (or system data in system mode). The L64021 is considered ready when both the interface is ready and there is room in the audio channel buffer. If this is not true, then AREQn is not asserted. The maximum transfer rate over this interface is 20 Mbit/s.

Note: In a DVD system, AREQn and AVALIDn input the program stream that is present on CH_DATA[7:0].

AVALIDn **Audio Data Valid** **Input**

The rising edge of AVALIDn writes the next byte of audio data or program stream data that is present on the CH[7:0] pins. AVALIDn can be used with the DCK data clock for synchronous input to the L64021's channel interface.

CH_DATA[7:0]

Channel Data Bus **Input**

CH_DATA[7:0] is an input bus that serves as a parallel path for incoming channel data.

DCK **Channel Data Clock** **Input**

The DCK is a free-running clock from the external channel. Together, the DCK and VALIDn signals can write data synchronously to the L64021 channel input.

ERRORn **Error** **Input**

ERRORn is an active-LOW input signal. The external channel device asserts this signal to indicate that the channel data contains an error. The ERRORn signal is latched with the data on the rising edge of AVALIDn or VVALIDn. ERRORn indicates uncorrectable errors in the channel, and invokes error handling in the L64021. ERRORn is not used for DMA transfers.

TOS **Top of Sector** **Input**
The external channel device asserts TOS during the pack start code at the top of a sector. The L64021 uses TOS for error detection and registers the TOS signal on the rising edge of AVALIDn.

VREQn **Video Transfer Request** **Output**
This signal is an active-LOW output. The L64021 asserts VREQn when it is ready to receive a new byte of coded video data. The L64021 is ready when both the interface is ready and there is room in the video channel buffer. If these conditions are not true, VREQn is not asserted. The maximum transfer rate over this interface is 20 Mbit/s.

Note: In a DVD system, the VREQn and VVALIDn pins are not used.

VVALIDn **Video Data Valid** **Input**
The rising edge of VVALIDn writes into the channel buffer the next byte of video data that is present on the CH[7:0] data bus. VVALIDn is not used in the system or program stream modes. VVALIDn can be used together with the DCK data clock for synchronous input to the L64021 channel.

Memory Interface

SBA[11:0] **SDRAM Address Bus** **Output**
This 12-bit output address bus specifies the row/column address and connects directly to an external SDRAM memory. The L64021 uses the external SDRAM memory for picture reconstruction and channel buffering.

SBD[15:0] **SDRAM Data Bus** **Bidirectional**
This 16-bit bidirectional data bus connects directly to an external 1M x 16-bit SDRAM memory. The L64021 uses the external SDRAM memory for picture reconstruction and channel buffering.

SCASn **SDRAM Column Address Select** **Output**
This is an active-LOW signal that drives the $\overline{\text{CAS}}$ pin on the attached SDRAM.

SCLK **SDRAM 81-MHZ Clock** **Bidirectional**
This 81-MHz clock signal drives the CLK pin on the attached SDRAM.

SCSn **Chip Select for SDRAM** **Output**
SCSn is an active-LOW signal that selects the low-address bank of the SDRAM, which is used for the first 16 Mbits of memory.

SCS1n **Chip Select for Second SDRAM** **Output**
SCS1n is an active-LOW signal that selects the high-address bank of the SDRAM. This signal is used in systems that have more than 16 Mbits of DRAM.

SDQM **SDRAM Control Pin** **Output**
SDQM is an active-HIGH output signal for the SDRAM data control mask.

SRASn **SDRAM Row Address Select** **Output**
This is an active-LOW signal that drives the $\overline{RAS}$ pin on the attached SDRAM.

SWEn **SDRAM Write Enable** **Output**
This is an active-LOW signal that drives the $\overline{WE}$ pin on the external SDRAM. The L64021 asserts this signal to enable an SDRAM write operation.

Video Output Interface

BLANK **Blank** **Output**
BLANK is a composite blank output from the L64021 display controller. Its polarity is active-HIGH.

CREF **Display Controller Output** **Output**
This display controller output signal serves as a Chroma reference. CREF is HIGH during the Cb component of Chroma.

EXT_OSD[3:0]
Palette Selection Bus **Input**
This four-bit input bus selects from the 16 colors in the on-chip color palette for an external OSD function. The EXT_OSD[3:0] data is sampled at SYSCLK/4 or 6.75 MHz, providing an OSD with a resolution of 352 pixels.

HS **Horizontal Sync** **Input**

HS is the horizontal sync signal, which resets the horizontal counters in the display controller. The horizontal sync signal must be synchronous to SYSCLK.

OSD_ACTIVE

On-Screen Display **Output**

This is an active-HIGH signal that indicates the on-chip OSD is active. This pin indicates which pixels have mixed OSD in the pixel port. Active output occurs at the pixel containing OSD mixed data.

PD[7:0] **Pixel Data Output Bus** **Output**

The data on the PD[7:0] bus represents the pixel data of the reconstructed picture. The pixel data is formatted in CCIR601 (Y, Cb, Cr) chromaticity.

VS **Vertical Sync / Odd-Even Field** **Input**

The host can program the L64021 so that VS is either a conventional Vertical Sync input or an even/odd field indicator. When in the even/odd field indicator mode, the internal display controller counters reset each time VS changes state (at the beginning of each field). The parity of the field is controlled by the timing of VS relative to HS. The odd/even field indicator should be synchronous to SYSCLK.

Audio Interface

A_ACLK **Audio Clock** **Output**

A_ACLK is an audio output clock that is selected from one of the audio input clocks (ACLK_32, ACLK_441, or ACLK_48).

ACLK_32 **Audio Clock (32)** **Input**

This audio clock is 32 kHz * N, where N equals 768, 512, 384, or 256.

ACLK_441 **Audio Clock (44.1)** **Input**

This audio clock is 44.1 kHz * N, where N equals 768, 512, 384, or 256.

ACLK_48 **Audio Clock (48)** **Input**

This audio clock is 48 kHz * N, where N equals 768, 512, 384, or 256.

ASDATA **Audio Serial Data Line** **Output**
ASDATA is the output for serial audio data. The host can program the format for either PCM or I^2S output mode.

AUDIO_SYNC
Audio Synchronization **Output**
This signal provides an audio sync indication for use in transport systems that require hardware sync controls. (Typically, this signal is used only in DSS systems.)

BCLK **Serial DAC Bit Clock** **Output**
This signal clocks the ASDATA bit into the DAC on BCLK's rising edge. BCLK has a programmable frequency that the host can set during initialization.

CD_ACLK **External Audio Clock** **Input**
This clock provides a reference source for the L64021's audio output stage that is used when the L64021 bypasses CD audio to the DAC output. Typically, the clock rate is either 256 * f_s or 384 * f_s.

CD_ASDATA **Audio Serial Data Line** **Input**
This signal is the serial audio data input that is used when the L64021 bypasses CD audio to the DAC output.

CD_BCLK **Serial DAC Bit Clock** **Input**
This signal clocks the ASDATA bit into the L64021 on the clock's rising edge. The L64021 uses this clock when bypassing CD audio to the DAC output.

CD_LRCLK **Serial DAC Left/Right Clock** **Input**
This input clock indicates which samples belong to the left and right stereo channels. The L64021 uses this clock when bypassing CD audio to the DAC output.

LRCLK **Serial DAC Left/Right Clock** **Output**
This output clock, which has a programmable frequency, indicates which samples belong to the left and right stereo channels.

SPDIF_IN **S/PDIF In** **Input**
This input signal is S/PDIF (IEC958) formatted data. During CD bypass mode, the L64021 routes the SPDIF_IN signal directly to the SPDIF_OUT pin.

SPDIF_OUT **S/PDIF Out** **Output**
This signal, whose frequency is programmable, contains audio data for Linear PCM samples in the IEC958 consumer format. The host can configure the L64021 to provide this signal as either an MPEG Audio or Dolby Digital compressed bitstream.

Miscellaneous and Test Interfaces

LP2 **PLL Loop Filter** **Bidirectional**
The system uses this pin to connect an external PLL loop filter to the L64021.

PLLVDD **PLL Power Supply Pin** **Input**
Phase-locked loop dedicated power input pin.

PLLVSS **PLL Ground Pin** **Input**
Phase-locked loop dedicated ground input pin.

RESETn **Reset** **Input**
This is an active-LOW input signal. When an external source asserts RESETn, the L64021 resets itself. The minimum RESET pulse width is eight cycles of SYSCLK. SYSCLK must be running during reset.

SCAN_TE **Scan Test Enable** **Input**
When asserted, this signal enables the scan test mode. This mode is used only during manufacturing test. During normal system operation, tie this pin LOW.

SYSCLK **Device Clock** **Input**
SYSCLK is the L64021's input system clock. The clock has a nominal frequency of 27 MHz. Picture reconstruction and video timing are referenced with respect to this clock.

TM[1:0] **Test Mode** **Input**
LSI Logic uses these two pins during manufacturing test. They are not intended for any other purpose. Tie both pins LOW during normal system operation.

ZTEST **Z Test Mode** **Input**
Z Test mode pin. This signal is used only for manufacturing test. Tie this pin HIGH during normal system operation.

Specifications

This section contains the electrical parameters for the L64021 DVD Decoder. Table 1 lists the absolute maximum ratings. Exceeding these values may cause damage to the L64021. Table 2 defines the recommended operating supply voltage and temperature. Table 3 shows the pin capacitance, and Table 4 lists the DC characteristics.

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Units
V_{DD}	DC Supply	–0.3 to +3.9	V
V_{IN}	5-V Compatible Input Voltage	–1.0 to +6.5	V
I_{IN}	DC Input Current	±10	mA
T_{STGP}	Storage Temperature Range (PQFP Package)	–40 to +125	°C

1. Referenced to V_{SS}.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	DC Supply	+2.15 to 3.6	V
T_A	Ambient Temperature	0 to +70	°C

Table 3 Capacitance

Symbol	Parameter[1]	Min	Units
C_{IN}	Input Capacitance	2.5	pF
C_{OUT}	Output Capacitance	2.0	pF

1. Measurement conditions are V_{IN} = 3.3 V (V_{IN} = 5.0 V for 5-V tolerant buffers), T_A = 25 °C, and clock frequency = 1 MHz.

Table 4 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{IL}	Voltage Input Low TTL CMOS		 — —	 — —	 0.8 0.2 V_{DD}	 V V
V_{IH}	Voltage Input High TTL CMOS 5-V Compatible		 2.0 0.7 V_{DD} 2.0	 — —	 — 5.5	 V V V
V_{OL}	Voltage Output Low 4-mA Output Buffers 8-mA Output Buffers	 I_{OL} = 4.0 mA I_{OL} = 8.0 mA	 — —	 0.2 0.2	 0.4 0.4	 V V
V_{OH}	Voltage Output High 4-mA Output Buffers 8-mA Output Buffers	 I_{OH} = –4.0 mA I_{OH} = –8.0 mA	 2.4 2.4	 — —	 — —	 V V
I_{IL}	Current Input Leakage[2] with Pulldown with Pullup	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS}	–10 35 –214	± 10 115 –115	 222 –35	µA µA µA
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	–10	± 1	+ 10	µA
I_{OSP}4	Current P-Channel Output Short Circuit (4-mA Output Buffers)[3, 4]	V_{DD} = Max, V_{OUT} = V_{SS}	–117	–75	–40	mA
I_{OSN}4	Current N-Channel Output Short Circuit (4-mA Output Buffers)[3, 4]	V_{DD} = Max, V_{OUT} = V_{DD}	37	90	140	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	—	10	—	mA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, f = 27 MHz	—	330	—	mA

1. Specified at V_{DD} equals 3.3 V ± 5% at ambient temperature over the specified range.
2. For CMOS and TLL inputs.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. These values scale proportionally for output buffers with different drive strengths.

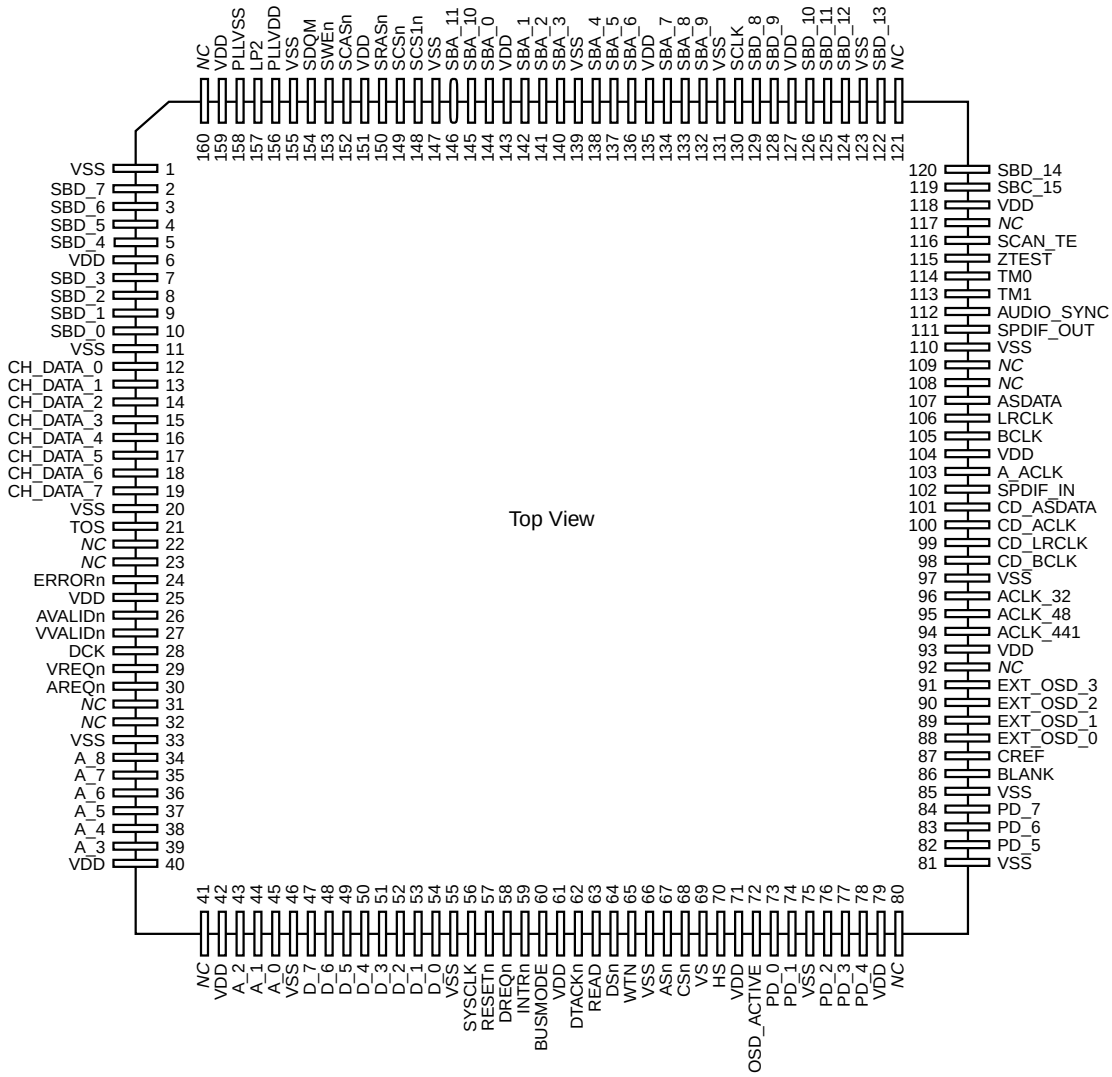
Pinout, Package, and Ordering Information

The L64021 is available in a 160-lead Plastic Quad Flat Package (PQFP). Table 5 provides the L64021 order number. Figure 4 supplies the L64021 DVD Decoder pinout diagram; Figure 5 and Figure 6 contain the package mechanical drawings.

Table 5 L64021 Ordering Information

Order Number	Clock Frequency	Package Type	Operating Range
65032A1	27 MHz	160-lead PQFP	Commercial

Figure 4 L64021 160-Lead PQFP Pinout Diagram

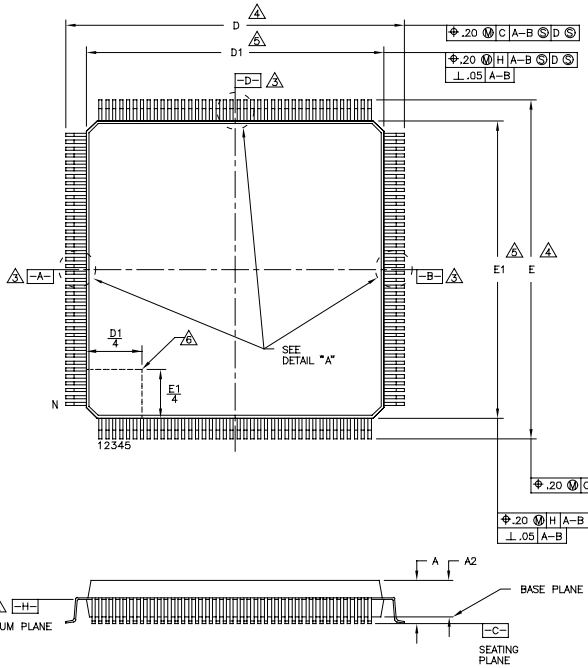


1. *NC* pins are not connected.

Figure 5 L64021 160-Lead PQFP Mechanical Drawing (Sheet 1 of 2)

For board layout and manufacturing, obtain engineering drawings from your LSI Logic marketing representative by requesting the outline

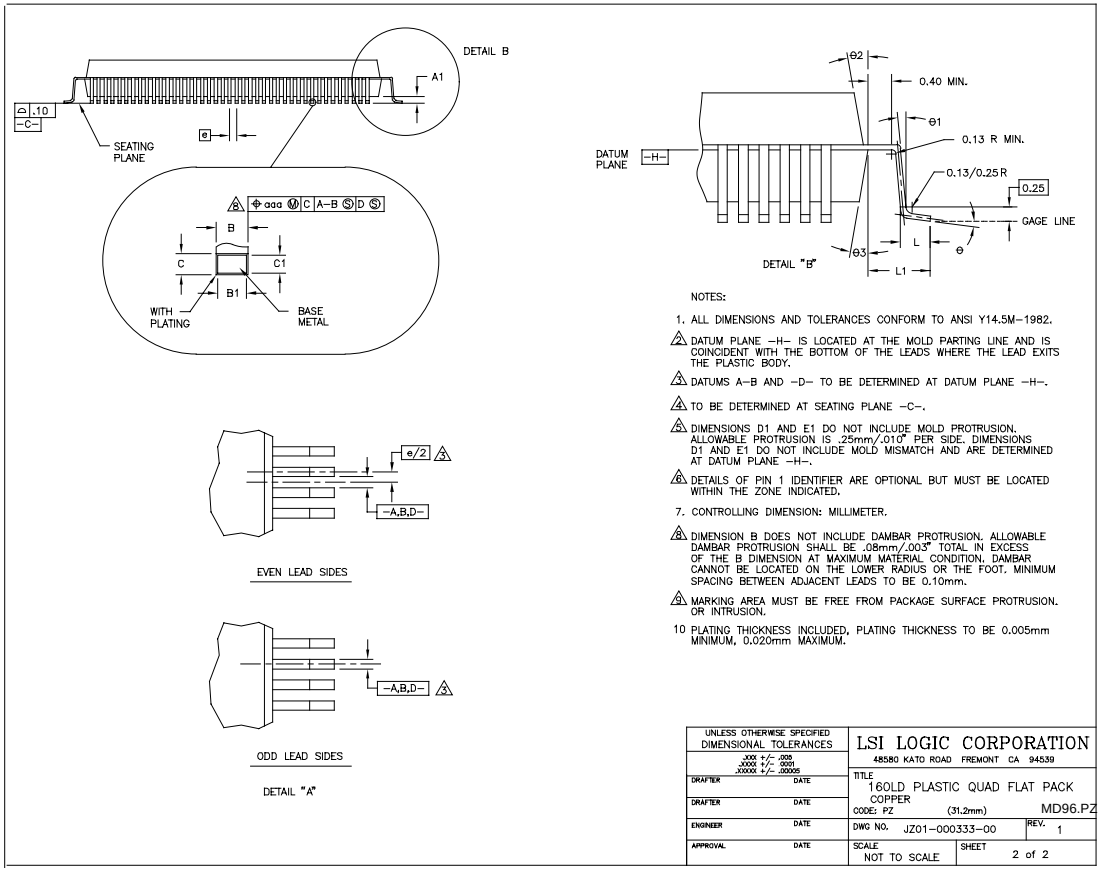
REVISIONS				
SIGNATURE AND DATE			DESCRIPTION	REV
APPROVAL	ECN NO.	DATE		
		02–15–91	INITIAL RELEASE	0
		08–09–93	REVISE DIMENSIONS	1



DIMENSIONS IN MM				
SYM	MIN	NOM	MAX	NOTE
A			4.01	
A1	0.25			
A2	3.17	3.42	3.65	
B	0.22		0.38	8
B1	0.22	0.30	0.33	
C	0.13		0.23	
C1		0.15±0.03		
D	31.00	31.20	31.40	4
D1		28.0±0.10		5
e		0.65 BSC		
E	31.00	31.20	31.40	4
E1		28.0±0.10		5
L	0.73	0.88	1.03	
L1		1.6 REF		
N		160		
θ	0		7	
θ1	0		8	
θ2	8		12	
θ3	8		12	
aaa			0.10	

UNLESS OTHERWISE SPECIFIED DIMENSIONAL TOLERANCES .XXX +/– .005 .XXXX +/– .0001 .XXXXX +/– .00005	LSI LOGIC CORPORATION 48580 KATO ROAD FREMONT CA 94539		
DRAFTER DATE	TITLE 160LD PLASTIC QUAD FLAT PACK COPPER		
DRAFTER DATE	CODE: PZ (31.2mm)	MD96.PZ	
ENGINEER DATE	DWG NO. JZ01–000333–00	REV. 1	
APPROVAL DATE	SCALE NOT TO SCALE	SHEET 1 of 2	

Figure 6 L64021 160-Lead PQFP Mechanical Drawing (Sheet 2 of 2)



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. DATUM PLANE –H– IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEADS WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
4. TO BE DETERMINED AT SEATING PLANE –C–.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .08mm/.003" TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACING BETWEEN ADJACENT LEADS TO BE 0.10mm.
9. MARKING AREA MUST BE FREE FROM PACKAGE SURFACE PROTRUSION. OR INTRUSION.
10. PLATING THICKNESS INCLUDED. PLATING THICKNESS TO BE 0.005mm MINIMUM, 0.020mm MAXIMUM.

UNLESS OTHERWISE SPECIFIED DIMENSIONAL TOLERANCES .XXX +/- .005 .XXXX +/- .0001 .XXXXX +/- .00005	LSI LOGIC CORPORATION 48580 KATO ROAD FREMONT CA 94539
DRAFTER DATE	TITLE 160LD PLASTIC QUAD FLAT PACK COPPER
DRAFTER DATE	CODE: PZ (31.2mm) MD96.PZ
ENGINEER DATE	DWG NO. JZ01–000333–00 REV. 1
APPROVAL DATE	SCALE NOT TO SCALE SHEET 2 of 2

Notes

Notes

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