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LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400 FAX (631) 271-0405

SELF-SCANNED CASCADE READOUT OF THE LS7060 AND LS7061

GENERAL DESCRIPTION

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The LS7060 and LS7061 are 32-bit binary counter-latch-output driver ICs designed to be used in system-oriented pulse counting applications. The data buffering provided by the latches allows data from one count interval to be saved quickly and later read out into a processor while the next count interval is proceeding.

The ICs are designed for self-scanned cascaded readout on an 8-bit wide three-state bus without external components. Figure 1 shows the appropriate connection. The COUNT input line from each package is brought out to its appropriate signal source, the ENABLE and CASCADE ENABLE pins are daisy-chained together and all other pins are bussed together. The TEST COUNT input may be used for system self-test functions or may be left unconnected. The ALTERNATE COUNT input may be used for system self-test or may be used as a common count-disable for all counters. In normal operation, the ALTERNATE-COUNT line is lowered to enable counting for the desired interval, then raised again when the interval ends. The SCAN RESET/LOAD line is then lowered to transfer the counter contents into the latches. One counter settling time after the last pulse was counted, the counter and latch contents are guaranteed stable and the transfer enable line can rise, isolating the latches again. The counter may then be cleared, and the next count interval may begin.

The SCAN RESET/LOAD pulse automatically resets the LS7060's internal scan counter so that when the output is enabled, the least significant data byte will be presented to the bus. The output is enabled whenever the ENABLE pin is low and the SCAN line is simultaneously high. When the SCAN line goes low after successfully enabling a package's output (i.e. the ENABLE line was also low), the scan counter is advanced so that the next more significant byte will be presented next. After a package's last byte has been output, the scan counter advances to an idle state. In this state the scan counter no longer advances, the output is always disabled and the CASCADE ENABLE output line is driven low. In the usual cascade connection, this enables the next package output and scan counter so that successive scan pulses fetch bytes from the next package in the cascade. When the data bus is dedicated to the counter readout and is not, for instance, simultaneously a processor memory bus, the SCAN line may be held normally high and pulsed downward briefly to advance the scan.

The LS7061 incorporates an additional 8-bit latch which may be used to read out the contents of a prescaler or other data. This additional data byte is treated as numerically less significant than the first byte of internally counted data and is presented first at the package output. The LS7061 readout scan thus yields five 8-bit data bytes, in contrast with four from the LS7060. Data readout from the two is otherwise identical.

OUTPUT SETTLING TIME: TTL BUS

The output of a single LS7060 or LS7061 is capable of driving a single TTL unit load with an external settling time which is small in comparison with its internal time delays. However, the cascade configuration discussed above is capable of reading out several hundred devices on a common data bus. When paralleling large numbers of outputs, the added capacitance of 15pF per output eventually slows the bus settling time until it becomes the major limit to readout rate.

The output circuit of the LS7060/7061 is shown in Figure 2. Throughout the range of TTL signal levels, the pull-down transistor may be treated as a resistor to ground when turned on, an open circuit when off. The maximum value of the equivalent resistor may be estimated from the specified minimum pull-down current of 6.2mA at 1.2V, Rd $\leq$ 200Ω. The pull-up device exhibits more complex quadratic behavior. Its output current when enabled may be approximated for output voltages Vout $\leq$ 3.5V by the relation:

$$\ddot{a}u = \ddot{a}ref \frac{(Vcc - 1.5 - Vout)^2}{(Vcc - 1.5 - Vref)^2}$$

where Vref is the output voltage (1.2V) at which minimum pull-up current is specified. Using values from LS7060 and LS7061 data sheets and assuming 5V operation:

$$\ddot{a}u = (3.5 - Vout)^2 \times 5 \times 10^{-4} \text{ Amps}$$

When the pull-up device of Figure 2 charges the bus capacitance C, the charging transient is described by the differential equation:

$$\frac{dV}{dt} = \frac{\ddot{a}out}{C} = \frac{(3.5 - V)^2 \times 5 \times 10^{-4}}{C}$$

which has the solution:

$$3.5 - V(t) = \frac{3.5 - V_0}{1 + t/R_0C}$$

where $1/R_0 = (3.5 - V_0) \times 5 \times 10^{-4}$, the effective source resistance at the initial output voltage V_0. Note that this corresponds to no actual ohmic resistor, but is merely the ratio of a voltage, 3.5 - V_0, to the the current delivered. For $V_0 = 0$, $R_0 = 570$ Volts/Ampere. Nonetheless, the quantity R_0C has the dimensions of time and sets the time scale for the non-exponential positive-going transient. The time required for the voltage to change from V = 0 to V = 2.4V is 2.2 R_0C. If each package contributes 18pF to the bus capacitance (15pF for the output plus 3pF for interconnections), the positive-going settling time will be 23ns per package or 2.3µs for a 100-package TTL bus.

Beginning from 3.5V, the highest voltage ever reached by the bus, a negative-going transient driven by the pull-down device of Figure 2 is initially an (approximate) exponential described by:

$$\frac{dV}{dt} = \frac{\ddot{a}}{C} = \frac{-V}{RC} \quad \text{or} \quad V = V_0 e^{-t/RC}$$

where R is the pull-down resistance and C the bus capacitance. The passage from 3.5V to a nominal TTL threshold of 1.5V takes a time equal to .85RC. Thereafter the pull-down current is diminished by the TTL input source current of 1.6mA. Thus:

$$\frac{dV}{dt} = \frac{\ddot{a}}{C} = \frac{\ddot{a}_{TTL} - V}{RC}$$

which leads to:

$$V - \ddot{a}_{TTL} R = (V_0 - \ddot{a}_{TTL} R) e^{-t/RC}$$

The decay is still (approximately) exponential with the same time constant, but has as its asymptote a voltage equal to $\ddot{a}_{TTL} R$, or about .32 Volts for R = 200Ω.

The remainder of the decay to a .4 Volt TTL drive level takes an additional 2.7RC, for a total of 3.6RC. Again, allowing 18pF per package, total settling time is 1.3ns per package, or 1.3 µs for a 100-package bus. This time can be decreased to 8ns/package if an LS type TTL receiver is used to reduce the bus receiver source current, but in any case the bus setting time is dominated by the positive-going transient which, as shown above, takes 23ns/package or 2.3µs per 100-package bus.

OUTPUT SETTLING TIME: CLAMPED BUS

The settling time calculated in the previous section can be reduced markedly by changing the properties of the bus receiver. The bus may be clamped to limit voltage excursions to only that necessary for adequate noise immunity and the clamp levels may be chosen to make rise and fall times nearly equal. The bus receiver shown in Figure 3 clamps the bus at a high level of 1.2V and a low level of .4V, with a sharp decision threshold at .8V provided by an MC 3430.

The threshold voltage is set by the emitter-base voltage of a silicon junction transistor and the clamp levels set at .8V ± .4V by the .4V standoff voltage of Schottky barrier signal diodes.

Within this restricted output voltage range, the LS7060 pull-up device may be approximated by a 2.7mA current source, leading to a linear positive-going transient. Thus:

$$\frac{dV}{dt} = \frac{\ddot{a}}{C} = \frac{2.7 \times 10^{-3}}{C} \quad \text{or } V = V_0 + t/370C$$

The transient from .4 to 1.2 Volts takes a time equal to 300C seconds, or 5.3ns per package at 18pF per package.

The negative-going transient from 1.2 to .4 Volts is exponential and with a 200 Ohm pull-down, takes 220C seconds, or 4.0ns per package. Again, the positive-going time is the longer and sets a settling time limit of 0.53µs for a 100-package bus.

MULTIPLE BUSSES

In the Digital Autocorrelator application (1) for which the LS7060 was originally developed, 553 packages, usually eight to a circuit card, were to be read out into a single processor. It proved convenient to divide the packages into two nearly equal groups, each group driving its own bus. Unclamped 267-package TTL busses would have required 6µs settling time, which would have slowed data readout unreasonably. Instead, two clamped busses were used, for a settling time below 1.5µs. All of the packages were arranged in a single readout cascade, with the two bus receiver outputs combined as shown in Figure 4. The cascading signals are used to enable the output of the appropriate receiver onto an inner data bus. This bus, too, was dedicated to data transfer only although in other applications it could be identical with one of the processor busses. In such a case, the Inner Bus Enable line shown could be driven low to free the bus for other uses.

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FIGURE 1. ARRANGEMENT FOR CASCADE READOUT

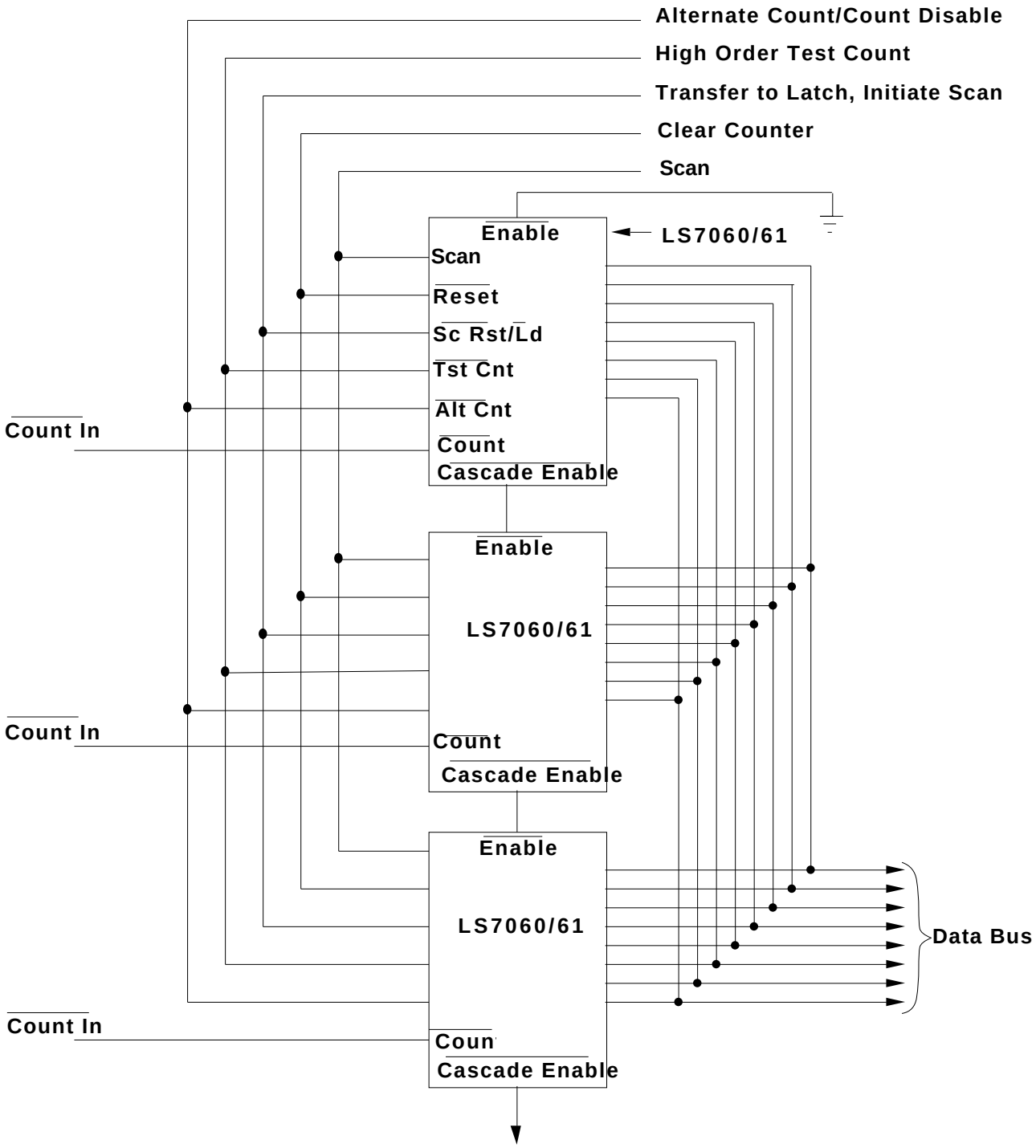

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FIGURE 2. LS7060/LS7061 OUTPUT CIRCUIT

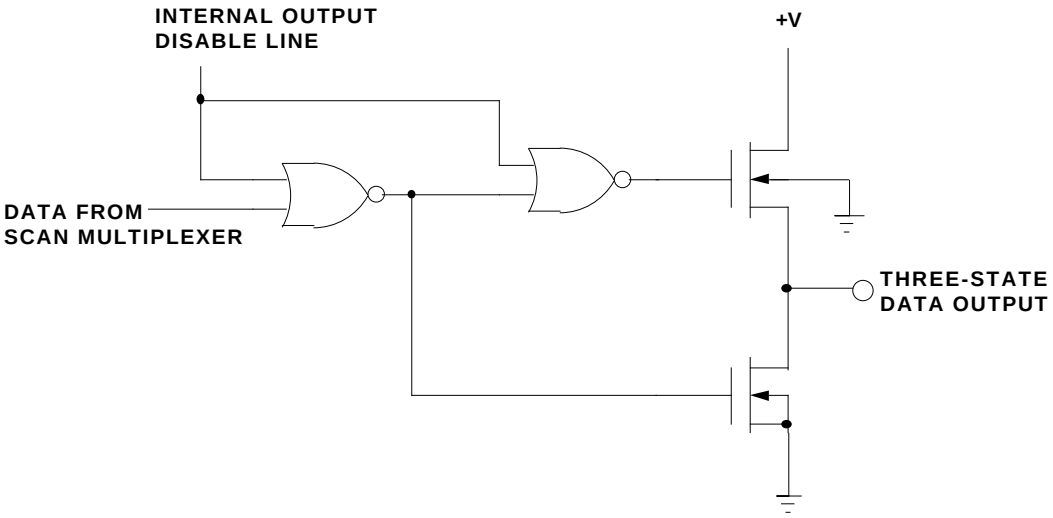

FIGURE 3. CLAMPED DATA RECEIVER

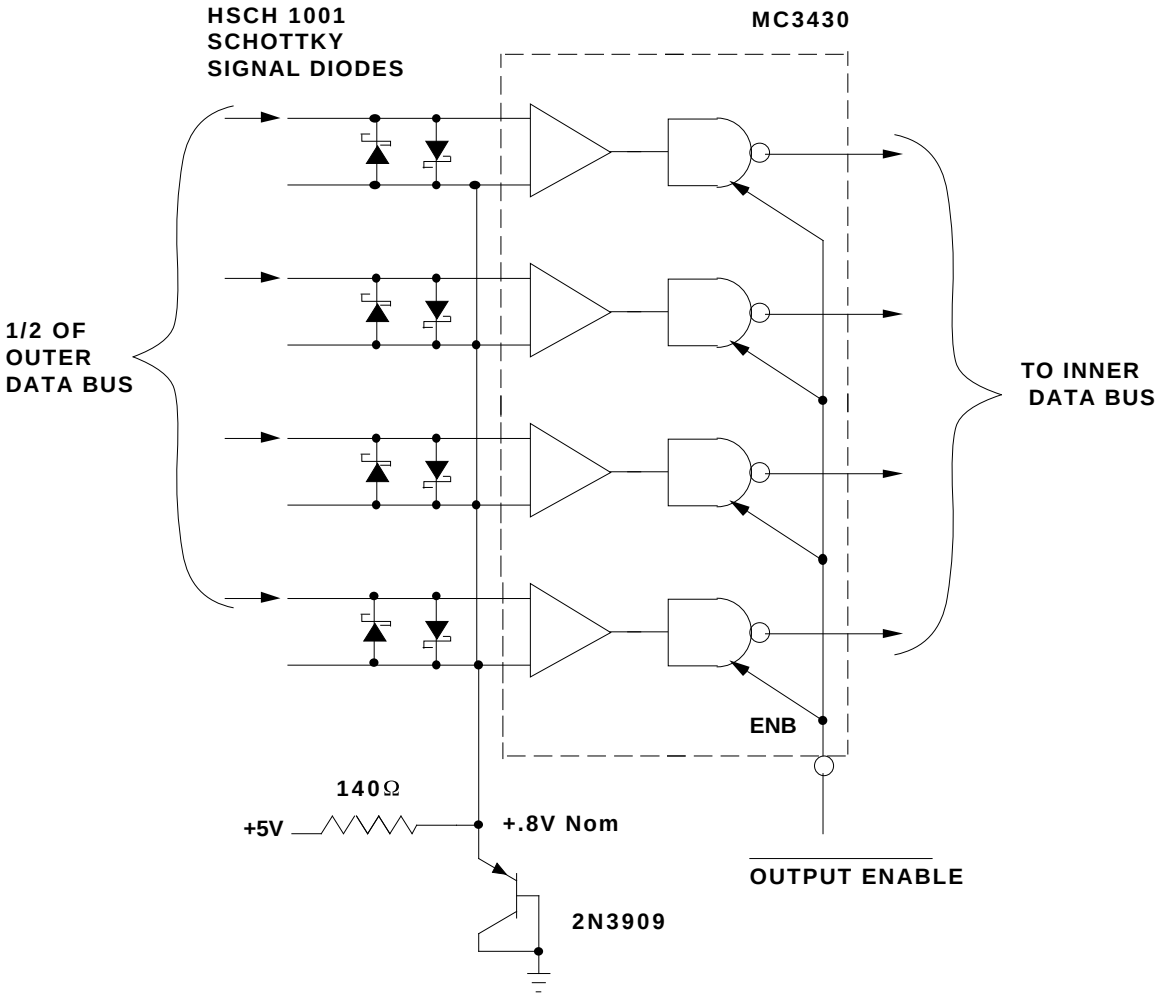

FIGURE 4. A MULTIPLE CASCADE

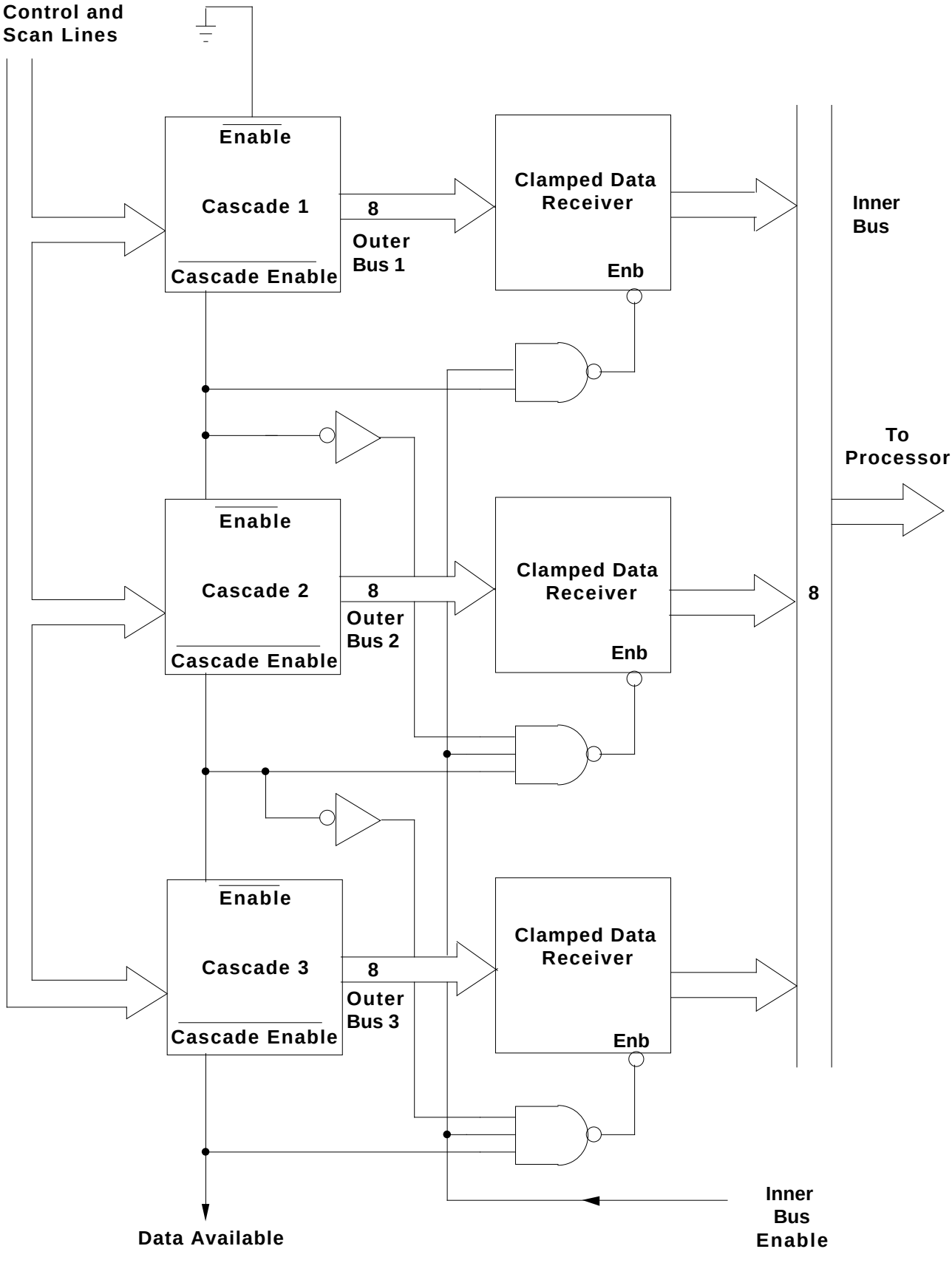

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FIGURE 5

SETTLING TRANSIENTS FOR A NOMINAL 100-PACKAGE BUS