LSI/CSI

APPLICATION NOTE 501

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FILTERING THE QUADRATURE INPUTS TO THE LS7166

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The filter shown in Figure 1 is used to eliminate noise on the input quadrature signals and thereby prevent an erroneous count from accumulating in the LS7166 up/down counter. Both Common Mode and Differential Mode noise is eliminated.

The filter operates using a clocked three stage shift register followed by a J-K Flip-Flop for each quadrature input signal. Quad A and Quad B represent the quadrature input signals. The Q outputs of the three D Flip-Flops are applied to a 3 input AND gate and a 3-input NOR gate whose outputs are used to drive the J and K inputs of a J-K Flip-Flop. Filtering occurs since the input quadrature clock must be at the same level for three consecutive clock samples before that level becomes the new output. If a noise spike occurs causing the input level to change during one of the three consecutive samples, then the J-K Flip-Flop will not change and the noise spike will be filtered out. In this case, three new samples must occur before a new output level can be generated.

For proper operation of this filter, at least eight clock pulses should be used for every count input cycle to insure proper synchronization and detection. This corresponds to a sampling clock frequency which is at least eight times the count input frequency. Actually, the sampling frequency should be made larger to insure that three consecutive correct samplings can be achieved in the presence of noise. The output of this filter produces quadrature signals A and B which are delayed from the input quadrature signals by at least three clock sample periods. The A and B signals are brought to the Count Input A and Count Input B inputs, respectively, of the LS7166.

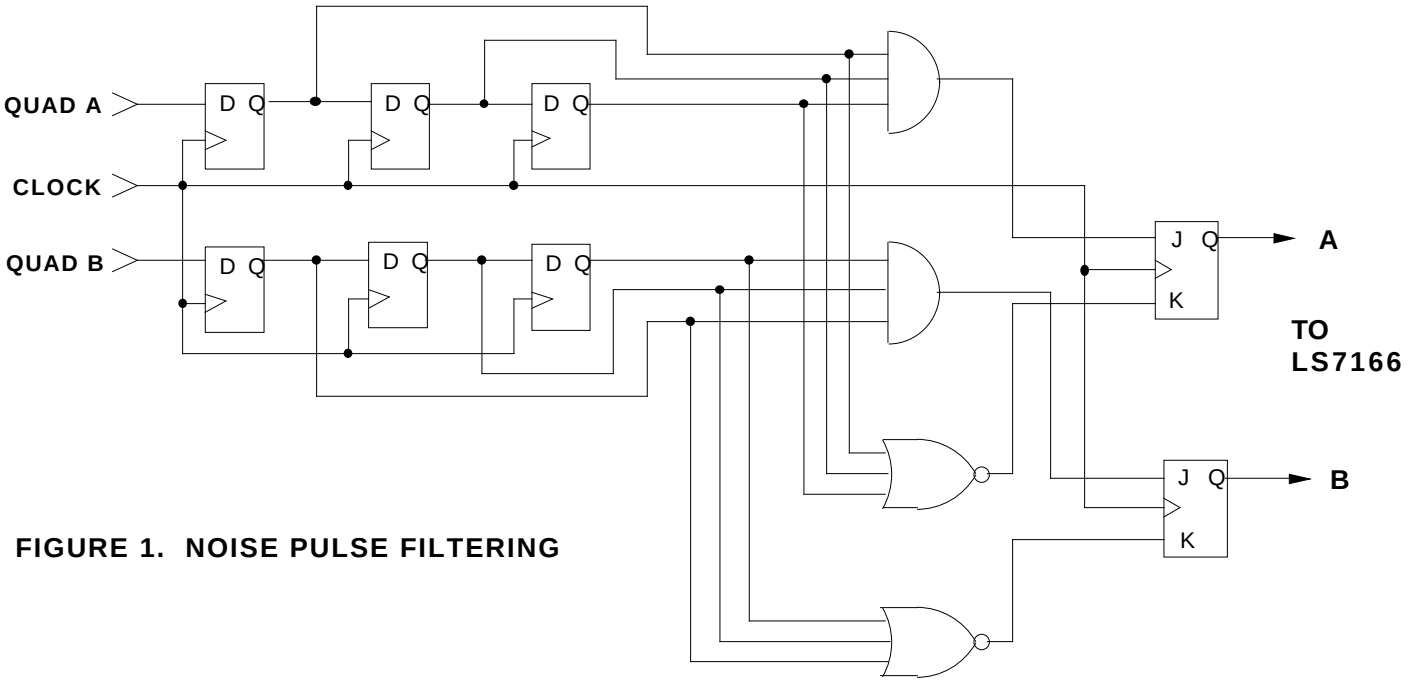

FIGURE 1. NOISE PULSE FILTERING