# N+1 Protection Without Relays Using Intel® Protection Interface Units (Intel® PIUs) - Intel® LXT3008 for T1/E1/J1

## Application Note

*April 2001*

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**Application Note**

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# Revision History

| Revision | Date | Description |
|---|---|---|
| -002 | 4/5/2001 | Title change and graphics improvements |
| | | |
| | | |

# 1.0 Abstract

This application note shows how to implement an N+1 protection architecture without relays for T1/E1/J1 applications. It starts by presenting the traditional, relay based implementation and discussing its disadvantages. In section 3, a “relay-less” N+1 system architecture based on Intel® Protection Interface Unit (Intel® PIU) ICs is introduced. The following section explains the implementation details from a technical perspective. Finally, section 5 summarizes the information presented in the previous sections and lists the advantages and disadvantages of the proposed solution over the traditional relay-based implementation.

# 2.0 Introduction

In today’s high speed internet economy, the reliability of critical network infrastructure elements is a primary concern. Down time in a critical communications link can cost the operator thousands of dollars per minute. To address this reliability concern, telecom equipment manufacturers commonly include redundancy protection in their systems. In a 1+1 protection scheme, there is a protection board for each active board in the system. This approach offers the highest reliability level but is obviously expensive. A more common approach is the N+1 protection scheme where a single protection board can replace any of N primary boards.

Traditionally, T1/E1/J1 N+1 protection has been implemented using electromechanical relays. Figures 1 and 2 show a simplified diagram of such an implementation. An independent protection card (P) can replace any of N primary line cards. The relay based protection matrix has access to all the input and output signals. A control board (not shown in these diagrams) constantly monitors the primary boards. When a failure is detected in one of the boards, a command is sent to the protection matrix to re-route the corresponding signals to the protection board. These simplified diagrams do not show the additional control circuitry used to decide on the board to switch. They also do not include the circuitry needed to drive the relay coils.

**Figure 1. Relay Based N+1 Protection- Transmit Path**

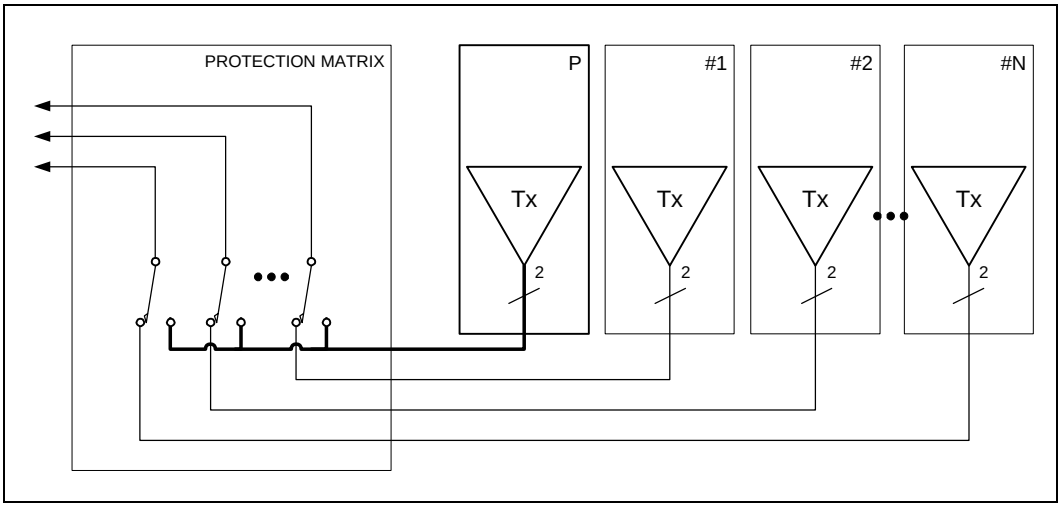
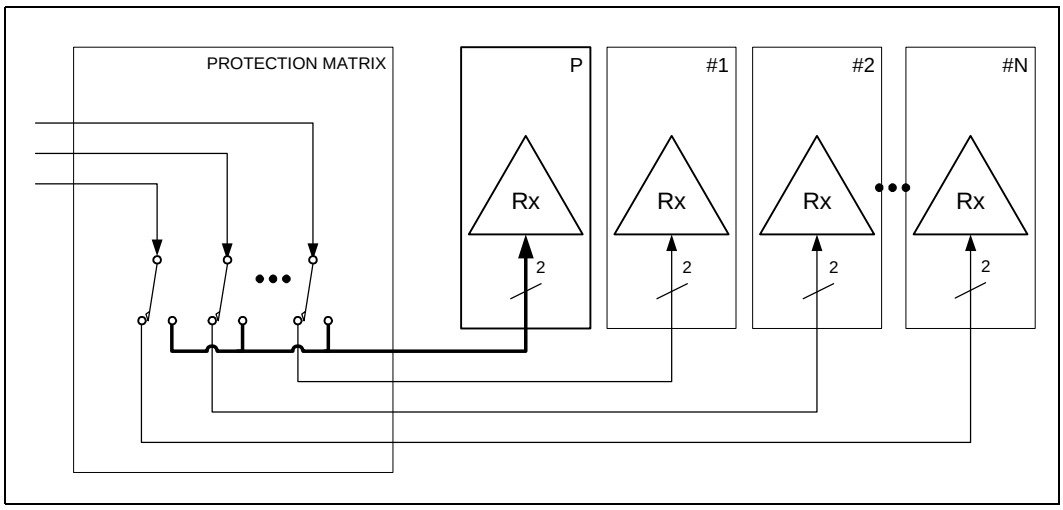


**Figure 2. Relay Based N+1 Protection- Receive Path**




The relay implementation is very simple from an architectural standpoint but unfortunately, there are many disadvantages to it:

- **Parts count**

  As an example, let's suppose each line card has 8 T1/E1/J1 ports (Transmit and Receive) and that the system includes one protection board for 7 active boards (7+1 protection). Assuming a DPDT (Dual Pole Double Throw) relay for each TIP/RING pair, this results in a total of 7*8*2 = 112 relays.

- **Space**

  Typical size for a miniature DPDT low signal relay is 15 x 7.5 mm. With a total of 112 relays, you will not have much space left for additional circuitry in the protection matrix.

- **Power Consumption**

  With 8 T1/E1/J1 ports per board you will need to activate a total of 16 DPDT relays in case of failure. Even efficient DPDT relays require about 140 mW each for coil activation. That accounts to a total power consumption of 16 * 140 = 2.26 W.

- **Switching Speed**

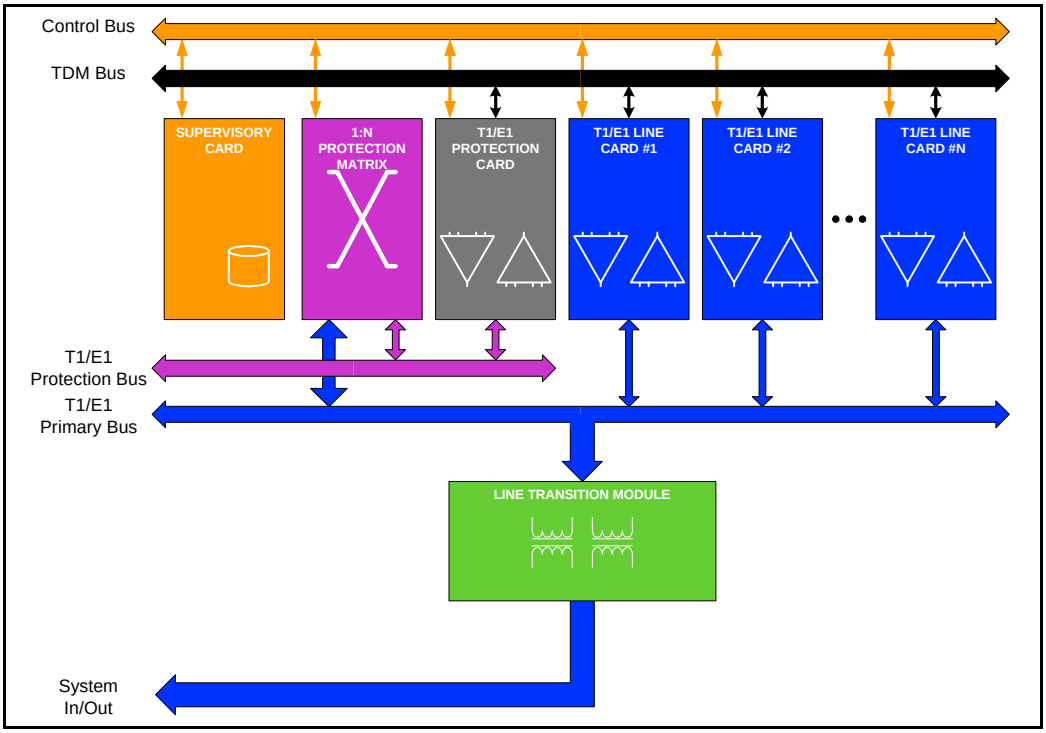
  Typical set time for relays is in the 2 to 4 ms range plus a bounce time of approximately 0.5ms. With a T1 link running at 1.544 Mbps, that set time corresponds to over 3000 bits of lost information. This is more than enough to trigger a red alarm (it only takes 175 contiguous bit periods of lost signal according to ANSI T1.231). This problem is accentuated with higher speed E1 links running at 2.048 Mbps.

As it can be concluded from the discussion above, there are a number of issues with relay based N+1 protection schemes. In the following paragraphs we will introduce a solution based on Intel® PIU ICs that will address these problems.

# 3.0 System Architecture

Figure 3 is a detailed view of a possible system architecture with N+1 protection.

**Figure 3. System Architecture**




With this architecture, there is a primary T1/E1/J1 bus running across the backplane. The primary bus carries all the analog TIP/RING signals from each of the N line cards. The protection matrix connects to all these signals and is normally set to a high impedance, non-intrusive state. There is a bus connecting the protection switching matrix to the protection board. Whenever one of the line cards is deemed to be faulty by the supervisory card, its output drivers are switched to a high impedance state. At this point, the protection matrix replaces the missing signal in the primary T1/E1/J1 bus with the signal from the protection card. A common line transition module contains all the isolation transformers, line side protection and receive side termination.

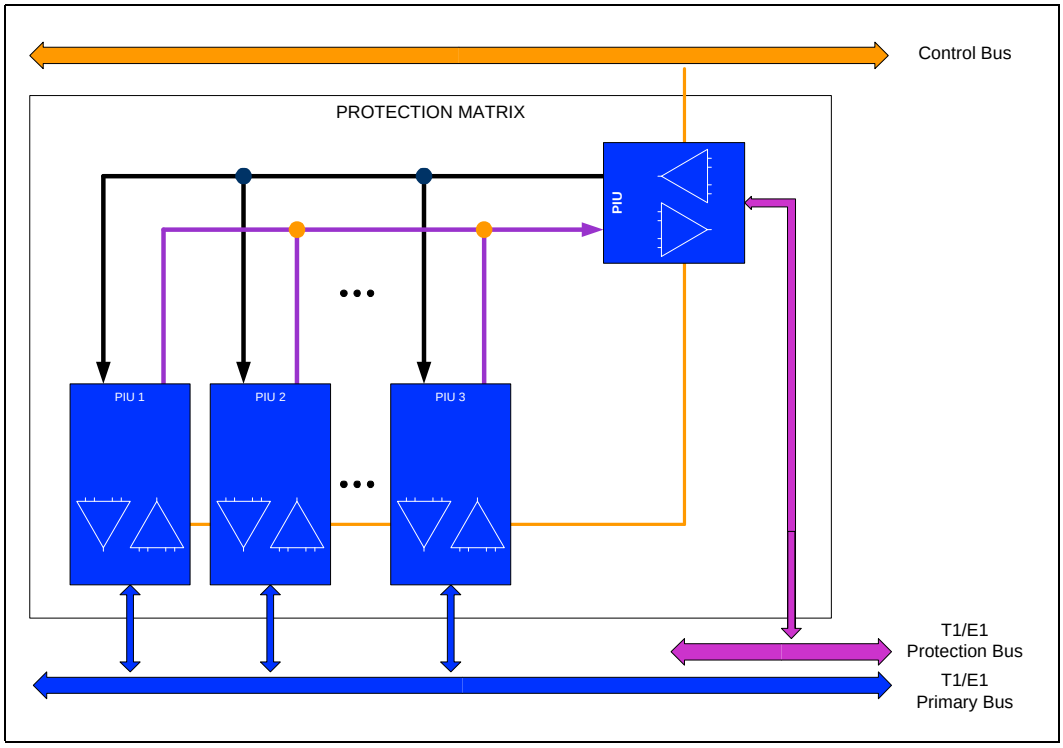
At the core of this system architecture is the protection matrix implementation. As we have seen in the previous section, this matrix is traditionally implemented using electromechanical relays. In the proposed architecture however, tri-state drivers and high impedance receivers are combined within the protection matrix to achieve the same objective. The following section looks at the protection matrix implementation in further detail.

## 3.1 Protection Matrix

The protection matrix in Figure 3 must be able to replace a T1/E1/J1 pair from any of the primary line cards with the T1/E1/J1 pair from the protection card. In the receive direction (input to the system) the matrix must tap on the corresponding signal in the primary bus and reproduce it at the

input to the protection card. In the transmit direction (output from the system) the matrix must replace the missing T1/E1/J1 signal with the signal coming from the protection card. A possible implementation that meets these requirements is shown in Figure 4.

**Figure 4. Protection Matrix**




The building block in this protection matrix is the Intel PIU, a simplified T1/E1/J1 multiplexing element (see Figure 7). Each PIU contains multiple tri-state drivers and high impedance receivers. On the analog side, these devices interface to the primary T1/E1/J1 bus and can either drive it or stay in a non-intrusive, high impedance state. On the digital side, the PIU provides recovered clock and data and also accepts transmit input clock and data. The receive output clock and data signals can be tri-stated. Therefore, multiple PIU elements can be connected in parallel as shown in Figure 4. An additional PIU interfaces to the protection card through the T1/E1/J1 protection bus.

Figure 5 and Figure 6 illustrate the backup data paths in case of failure in one of the line cards (card #2 in this example). In the transmit path, one PIU receives the signal from the protection board. The recovered clock and data are distributed to the other N PIUs. Since all PIUs' drivers with exception of #2 will be tri-stated, the transmit signal from the protection board is effectively routed to the T1/E1/J1 primary bus (see Figure 5).

In the receive path, PIU #2 recovers the input signal from the primary bus and delivers it to the PIU connecting to the protection card. The remaining PIUs are tri-stated in the digital output side so there is no bus contention. See Figure 6.

**Figure 5. Protection Switching, Transmit Path**

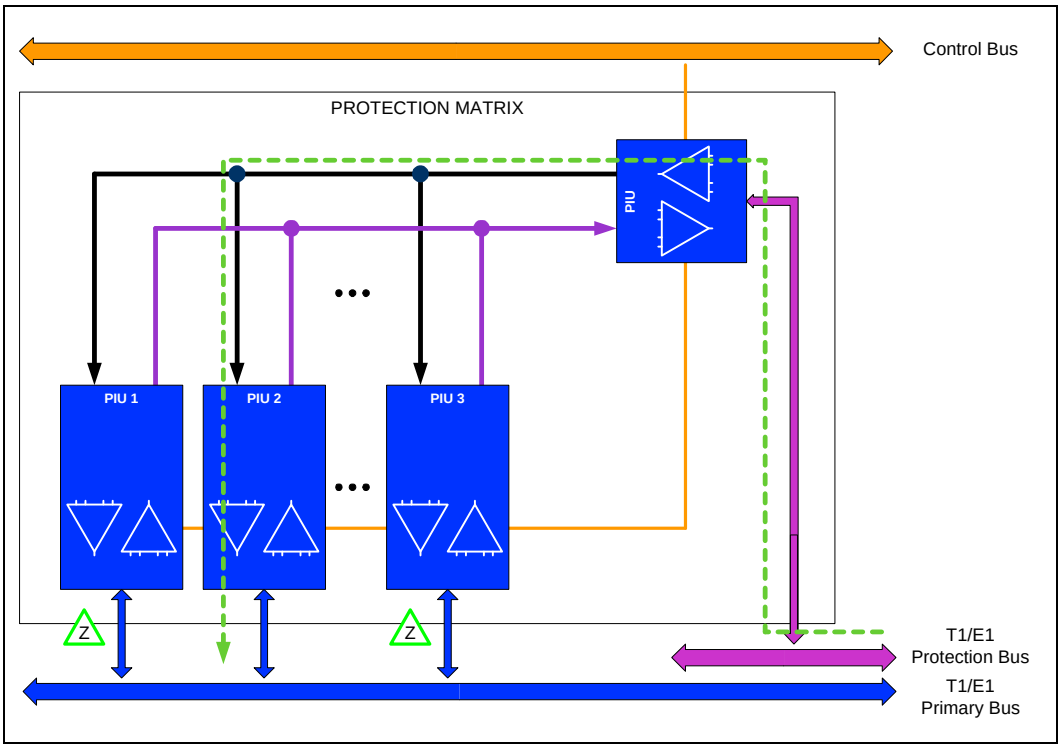
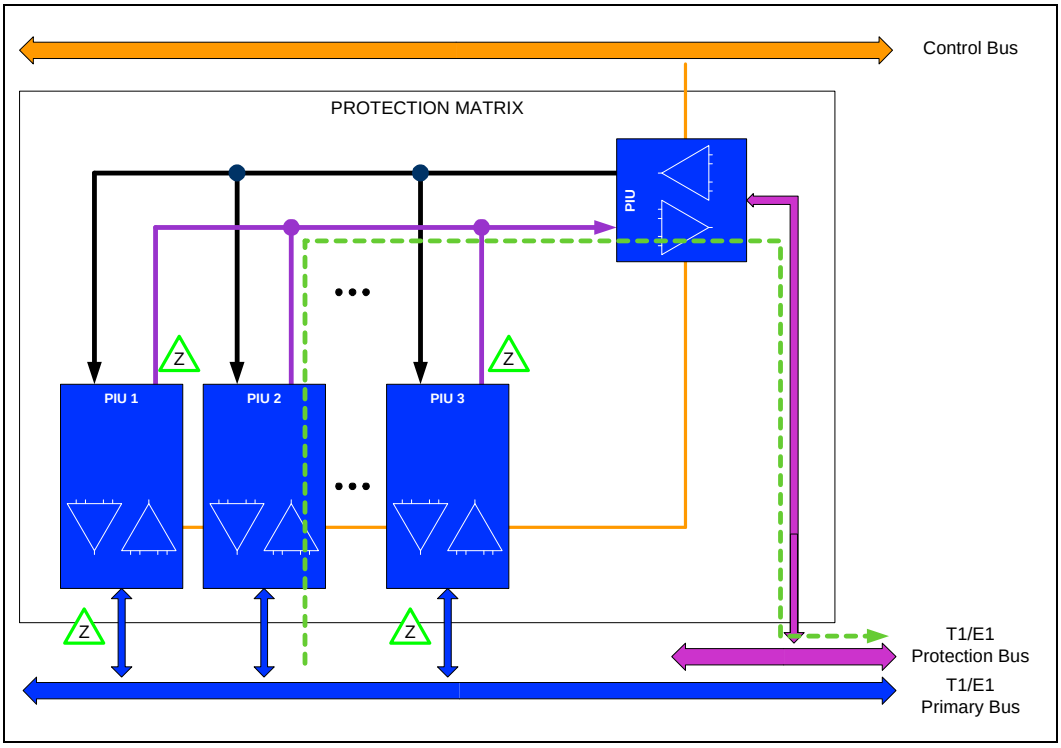
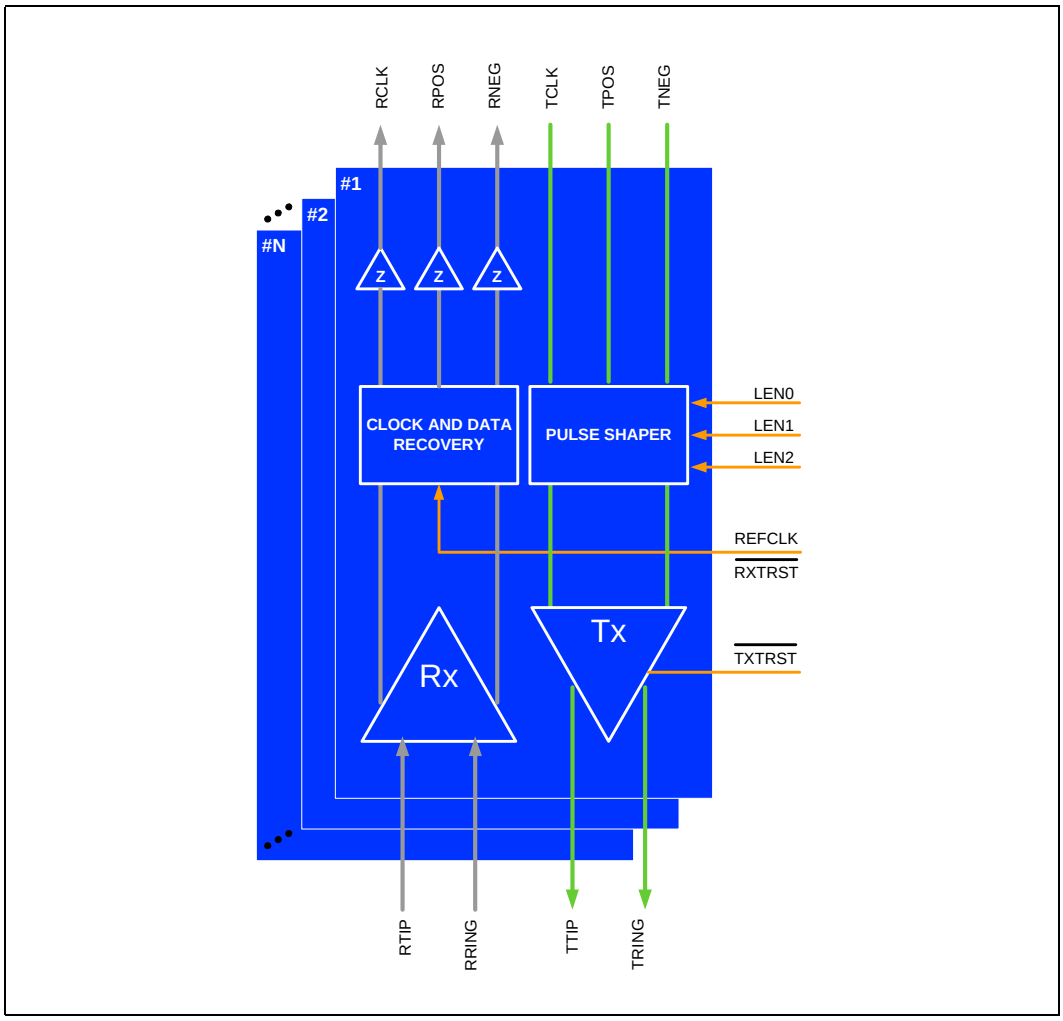



**Figure 6. Protection Switching, Receive Path**



## 3.2 The Intel® Protection Interface Unit (Intel® PIU)

**Figure 7. The PIU**




The Intel PIU is available as an 8 port, 15x15 mm, 160 pin PBGA package.

Intel PIUs are controlled by hardware or serial host mode. A 1x reference clock (1.544 MHz for T1 and 2.048 MHz for E1) is required for clock recovery. A single reference clock can feed all the PIUs in a protection matrix. Both the output analog drivers and the receive clock and data digital buffers can be tri-stated. PIUs also include three line build-out inputs (LEN0-2) for T1 DSX applications.

# 4.0 Implementation Details

The following sub-sections address specific implementation details from a technical perspective. We start by describing the electrical interface from the line cards to the protection matrix and from the matrix to the protection card. Design topics regarding the protection matrix implementation are also covered in this section. The following discussion is targeted to short-haul applications using the Intel LXT38x family of T1/E1/J1 LIUs in conjunction with the Intel PIU.

## 4.1 Line Card/Protection Matrix Interface

Application note 249464, "LXT380/1/4/6/8 Redundancy Applications, T1/E1/J1 Intel® Hitless Protection Switching (Intel® HPS) Without Relays" discusses the implementation details for 1:1 redundancy. Since the Intel PIU transmit and receive circuitry is identical to the LXT38x family of transceivers, the same interface as proposed in this application note can be used for connecting the line cards to the protection matrix in N+1 redundancy applications. Figure 8 and Figure 9 show the interface proposed in the above referenced application note. Only one channel is represented for simplicity. The reader is referred to the above referenced application note for further implementation details such as component values and performance test results.

**Figure 8. Line Card to Protection Matrix Interface, Receive Direction**

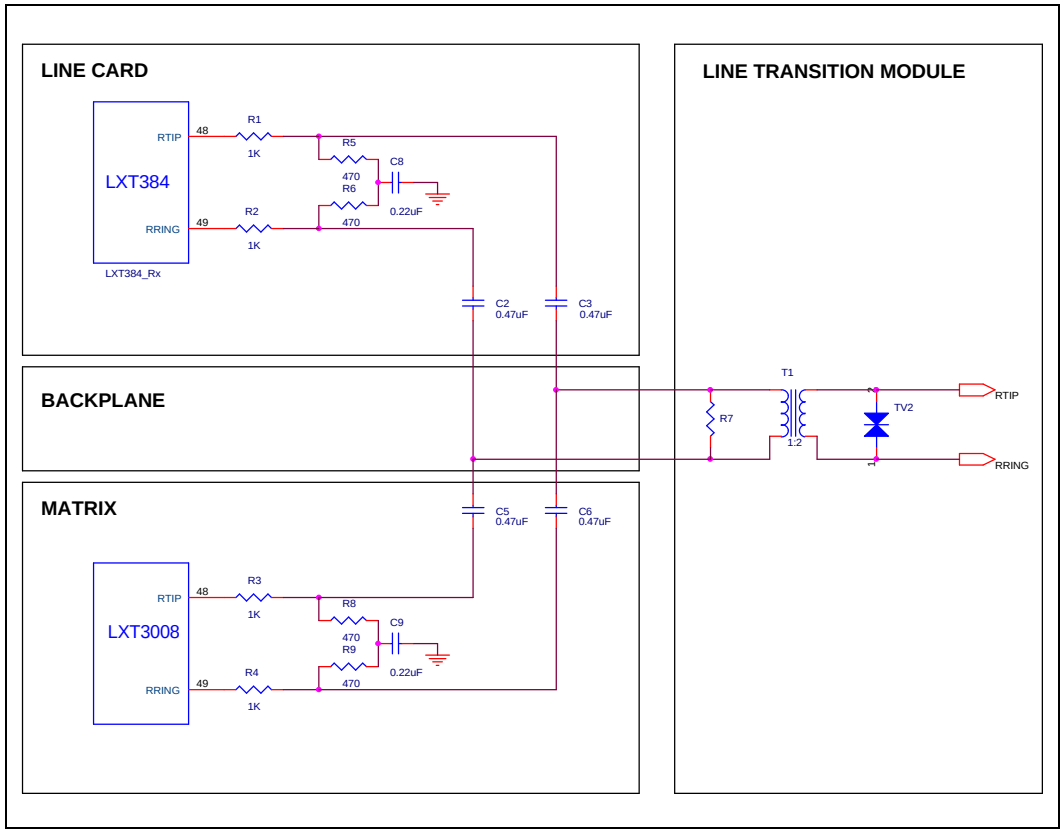
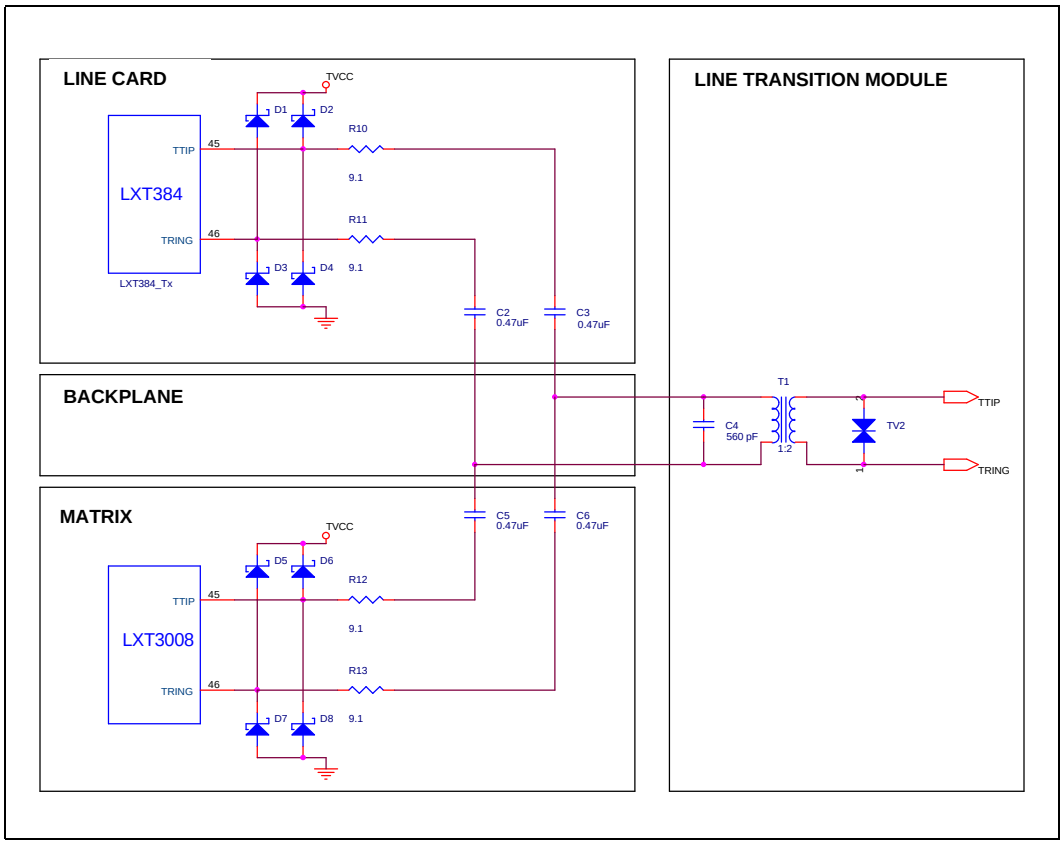


**Figure 9. Line card to Protection Matrix Interface, Transmit Direction**

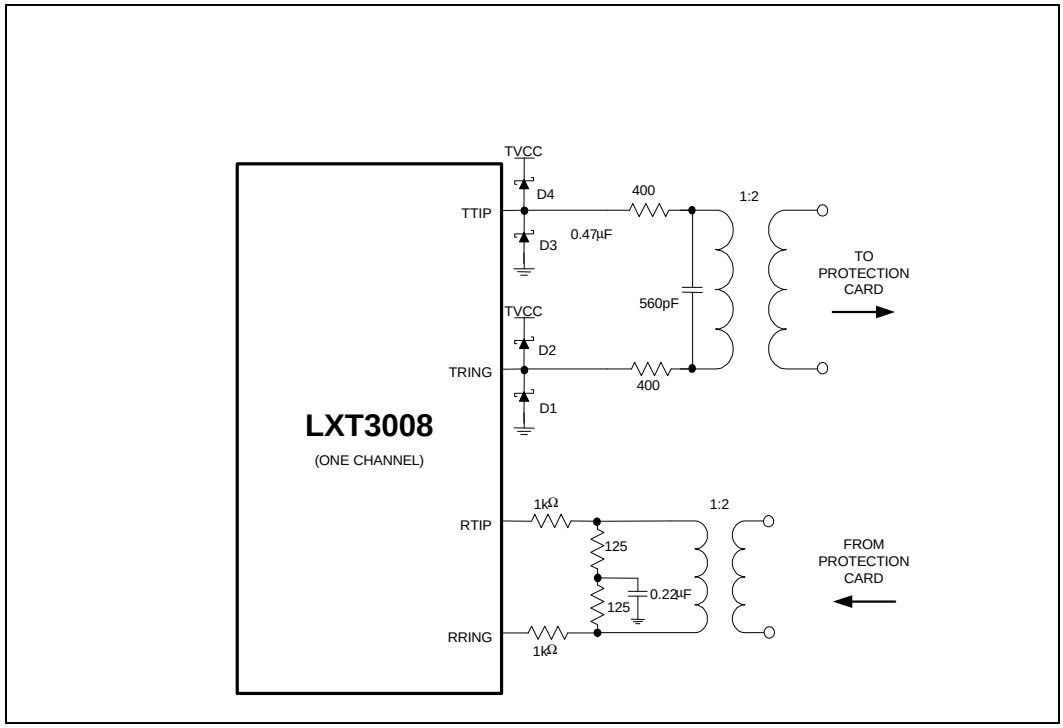



Because the protection matrix adds to the total data throughput delay, the N+1 configuration cannot guarantee hitless switching. However, the switching time is still much faster than that of using mechanical relays, significantly reducing data loss.

## 4.2 Protection Matrix/Protection Card Interface

The connection between the protection matrix and the protection card in Figure 3 is an internal connection. These signals do not go to any T1/E1/J1 lines outside this system. Therefore, the stringent pulse template and return loss specifications do not apply to this internal connection.When protection switching is activated, the line driver in the protection card and the line driver in the Intel PIU interfacing to the protection card will launch pulses that travel very short distances through the backplane. However, driving these pulses requires power. Fortunately, you can reduce power significantly by increasing the terminating impedances at the PIU line interface. The interface proposed in Figure 10 was tested in our labs for reliable transmission and it resulted in significant power savings. Please refer to the PIU data sheet for additional details on power consumption performance. The circuit in Figure 10 was designed to interface to the same capacitive coupled interface used in the line cards. Therefore, the protection card design can be exactly the same as the line card design.

**Figure 10. Low Power Interface To The Protection Card**




## 4.3 Matrix Control

The supervisory card is responsible for controlling protection switching within the matrix. As illustrated in Figure 5 and Figure 6, the Intel® PIU corresponding to a faulty line card must be activated while all the other PIUs are tri-stated on both the digital and the analog (line) side. Two input pins to the PIU control whether the analog and the digital interfaces are tri-stated or not. See Table 1.

**Table 1. LXT3008 Tri-State Control**

| PIU State | $\overline{\text{TXTRST}}$ | $\overline{\text{RXTRST}}$/REFCLK |
|---|---|---|
| **Active** | High | 1.544 or 2.048 MHz Clock |
| **Inactive** | Low | Low |

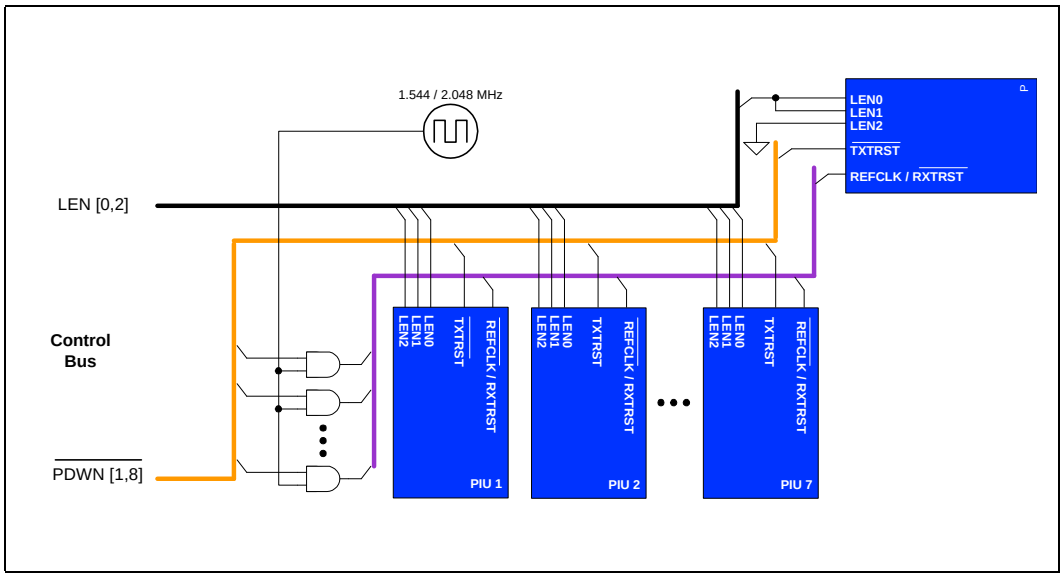
The PIU interfacing to the protection card (upper right corner in Figure 5 and Figure 6) should be activated whenever there is a faulty line card. Figure 11 represents a possible control circuitry implementation for a 7+1 protection matrix.

Eight $\overline{\text{PDWN}}$ (Power-Down) inputs determine whether the corresponding PIUs are active or not. A 1.544 MHz or 2.048 MHz reference clock is routed to a series of AND gates. The AND gates ensure that the $\overline{\text{RXTRST}}$/REFCLK inputs are set Low when the corresponding $\overline{\text{PDWN}}$ pin is Low. When the $\overline{\text{PDWN}}$ pin is High, the reference clock is applied to the PIU. Since of the seven PIUs in the bottom of Figure 11 only one will be active at any time, the $\overline{\text{PDWN}}$[1,7] control signals can also be generated from a three bit word and a decoder. This minimizes the number of control signals from the backplane.

In addition to the power-down signal, the control bus should also provide line build-out inputs for the PIU transmitters (LEN[0,2]). Since only one PIU will be active at any time, only three lines are required. Note: With this hardware mode only implementation, all the ports within one PIU will share the same LEN setting. This is not an issue for E1 only applications where there is no line build-out. However, if per port line build-out is required, you should use a PIU with a serial HOST mode control.

The Intel PIU interfacing to the protection board is only required to drive the short distance between the protection matrix and the protection board. Therefore, only LEN0 and LEN1 are connected to the line build-out inputs. Set LEN[0,1] to 11 for T1 applications. In E1 only applications, you should set all the LEN inputs Low. No line build-out control is required in this case.

**Figure 11. Protection Matrix Control**




## 4.4 Matrix Power Supply

Since the reliability of the protection matrix is fundamental in a N+1 architecture, you should pay special attention to its power supply design. Here are a few guidelines:

- **Power Supply Protection**

  The power supply should be adequately protected against lightning surges and EFTs (Electrical Fast Transients). Sidactors or TVS devices (Transient Voltage Suppressors) should be placed right at the power supply input, close to the disturbance source. Telecom systems are required to survive standardized surge testing performed according to international standards such a IEC 61000-4-5.

- **Fuse Protection**

  You should also consider including a protection fuse at the power supply input. If there is a severe malfunction in the matrix such as a latch-up, the fuse will power-down the matrix preventing it from interfering with other circuits. Note that a powered down matrix board will not interfere with the flow of traffic provided the tri-state pins are asserted.

- **Noise Filtering**

  You should follow common power supply noise reduction techniques in the matrix design. Power inputs should be filtered through a combination of ferrite beads and decoupling capacitors.

You will find additional information that applies to a PIU design including layout guidelines and recommended part numbers in the LXT384 Design Assistant at http://developer.intel.com.

# 5.0 Summary

As demonstrated in the previous sections, it is possible to implement T1/E1/J1, N+1 redundancy protection without relays. PIU based architectures, offer significant advantages over a relay implementation as summarized in Table 2.

**Table 2. Relays vs. PIU**

| Features Set | Relay | PIU |
|---|---|---|
| **Power Consumption** | High | Low |
| **Size** | Big | Small |
| **Isolation** | Good | Fair |
| **Switching Speed** | Milliseconds | Microseconds |
| **Switching Noise** | High | Low |

Figure 12 illustrates the space savings achieved through a PIU implementation. This figure assumes a 7+1 protection matrix with 112 relays. Each line card supports 8 T1/E1/J1 ports. A typical 6U Eurocard format board is shown.

**Figure 12. Space Comparison**