Designing an ITU G.742 Compliant PDH Multiplexer with the LXT332 Dual Transceiver

Application Note

January 2001

Order Number: 249164-001

As of January 15, 2001, this document replaces the Level One document known as *AN056*.

Application Note

Contents

Figures

1.0 General Description

This Application Note summarizes jitter performance requirements at the E1 line interface for digital multiplexing equipment as specified in ITU G.742. Appropriate conformance testing procedures using the SXT6234 PDH multiplexer device are explained. Typical performance results using the LXT332 E1 dual line interface are presented, showing that the combination of this transceiver with the SXT6234 provides a highly integrated solution when designing PDH multiplexing equipment with G.742 compliance requirements.

1.1 Features

The ITU-T recommendation G.742 specifies “second order digital multiplex equipment operating at 8448 Kbit/s and using positive justification”. In other words, G.742 specifies the multiplexing of four E1 2.048 Mbps data streams into a single E2 8.448 Mbps signal using a positive justification mechanism. This kind of system can be easily implemented using the configuration shown below.

The LXT332 dual E1 line interface provides a high level of integration and a digital crystal-less jitter attenuator. The SXT6234 provides a single chip solution for multiplexing the four E1 signals into one E2 8.448 Mbps aggregate signal. In addition, by using the configuration illustrated below, an E1 to E3 multiplexer can also be easily implemented.

For the E1 tributary output ports, recommendation G.742 specifies that “the peak to peak jitter at a tributary output in the absence of input jitter should not exceed 0.25 UI when measured in the frequency range up to 100 KHz”. The lower frequency limit should be as low as possible taking into account the limitations of measuring equipment.

Figure 1. E1 to E2 Multiplexer

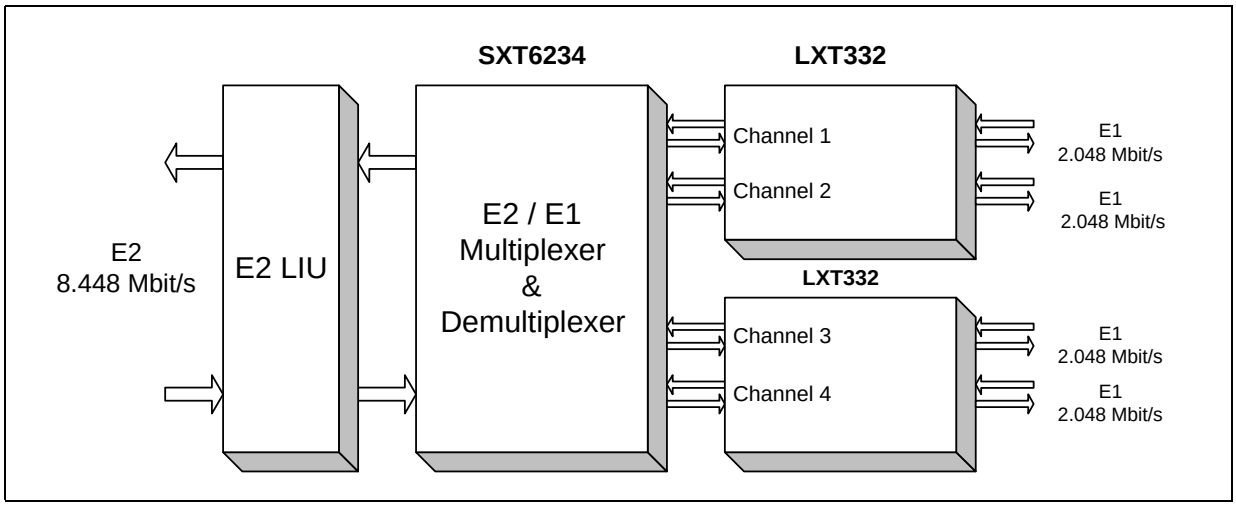
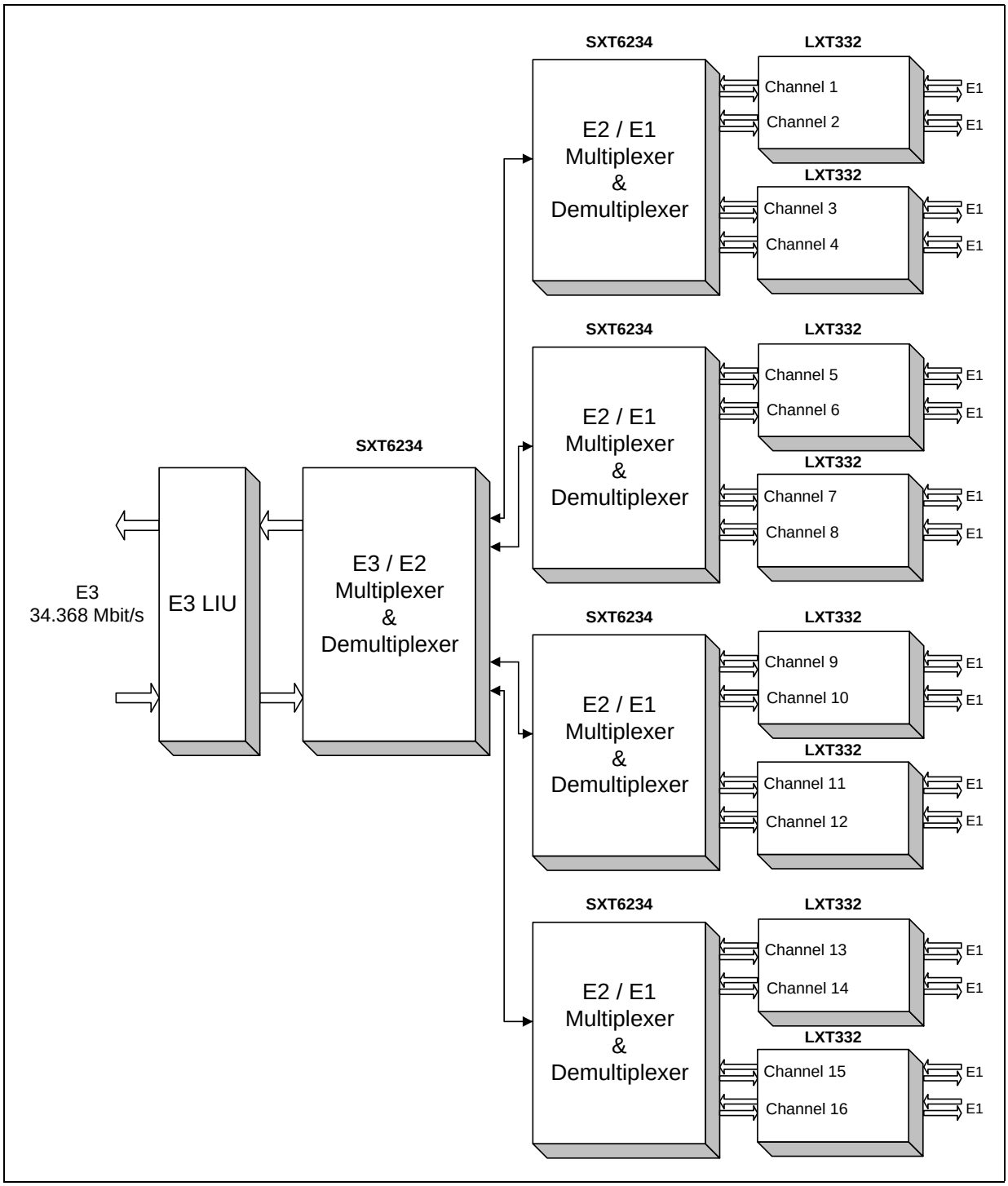


Figure 2. E1 to E3 Multiplexer



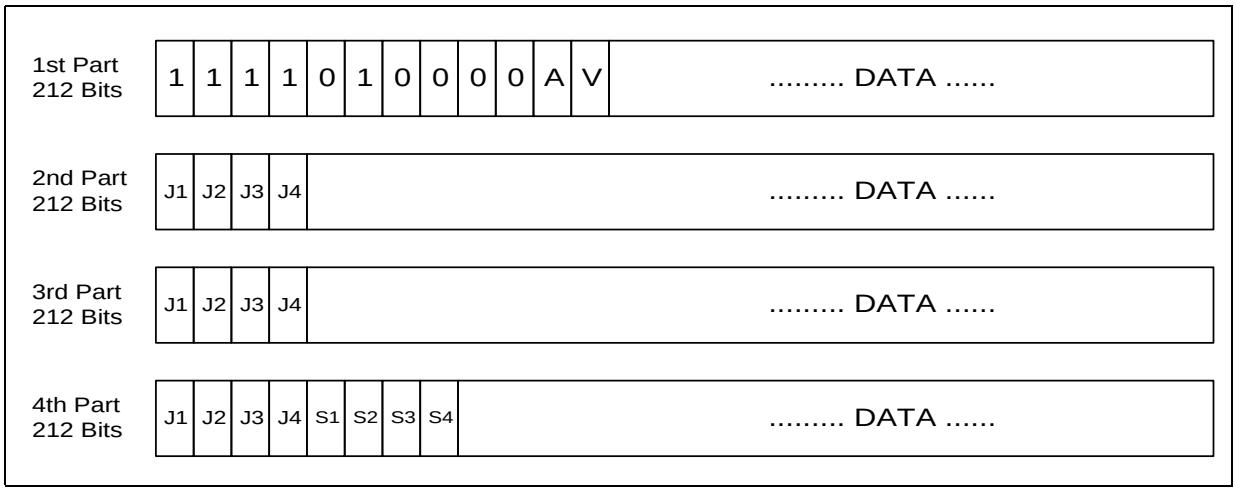
In the absence of jitter at the aggregate (E2) port, the two main sources of jitter that should be attenuated by the LXT332 jitter attenuator are the Multiplexing Jitter and the Stuffing Jitter. Both jitter sources result from extracting an E1 tributary out of the E2 frame. Figure 3 represents an E2 frame as described in G.742.

Multiplexing Jitter is due to clock gaps in the E1 transmission clock. These gaps occur as a result of discarding fixed control bits out of the E2 frame. This process translates into fixed 3-bit wide gaps from discarding the frame alignment word plus control bits (A,V) and 1-bit wide gaps from discarding the justification control bits (J1 to J4). These gaps occur at a fixed 8 KHz rate and have a fixed amplitude. The jitter component they originate is easily handled by the LXT332 jitter attenuator.

Stuffing Jitter is a consequence of the positive justification mechanism used to build the E2 frame. This mechanism is necessary to adapt the tributary E1 clock rate to the aggregate E2 clock rate. Normally, the S*n* bits (Stuff bits) in the E2 frame carry information pertaining to one of the tributaries. When a justification is needed to compensate for the asynchronous clock rates, the S*n* bits do not carry information. At the demultiplexer end, the J*n* bits (Justification control bits) indicate to the demultiplexer whether the S*n* bits carry information. If the S*n* bit does not carry information, the E1 transmission clock will be gapped at the S*n* position. This process is known as destuffing. The jitter originated by this mechanism is stuffing jitter.

The LXT332 has been refined for operation in gapped clock jitter environments and meets G.742 jitter requirements. Older LXT332 two-micron devices do not meet this specification. Please call your area Intel representative for more information about the availability of newer parts.

Figure 3. E2 Frame Structure



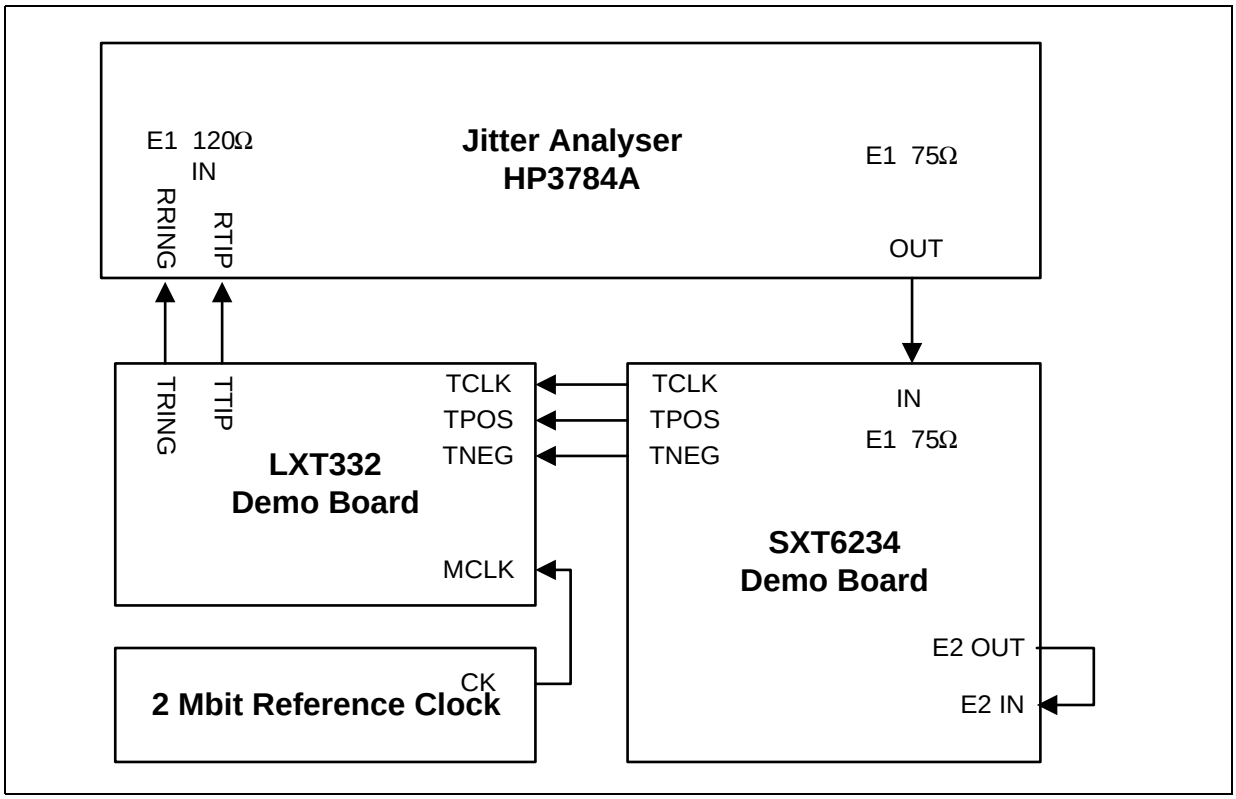
2.0 Conformance Testing

Figure 4 illustrates the recommended configuration for G.742 conformance testing. The SXT6234 Evaluation Board is used in conjunction with the LXT332 Evaluation Board in order to perform the jitter measurements. The SDB6234 board is set to E1/E2 multiplexing (E1LLBA=ON). The E2 output is looped back to the E2 input, so that the incoming E1 data stream is multiplexed into an E2 signal and is demultiplexed back into E1 again. The SXT6234 board uses the LXT305A as the E1 line interface. The TCLK, TPOS and TNEG inputs to the LXT305A reproduce the effects of stuffing and destuffing that occurred within this multiplexing/demultiplexing process in the form of TCLK gaps. These three transmit signals are extracted from the SDB6234 board and delivered to the LXT332. The LXT332 demo board must be set with the jitter attenuator placed in the transmit direction and the equalizer control inputs set to 120 Ω E1 (LEN[2,1,0] = 001).

The conformance test will ensure that the output jitter of the LXT332 on the E1 transmit line is smaller than 0.25 UI in the frequency range up to 100 KHz. Configure the HP3784A jitter generator/analyzer to transmit a 75 Ω E1, HDB3 encoded, 2^{15} -1 pseudo-random pattern. The jitter analyzer on the HP3784A should be set to 120 Ω E1 and the jitter measurement filter to 100 KHz low pass (LP). For improved accuracy, the jitter measurements should be taken using the smaller measurement scale of 1 UI max. Provide an external free-running 2.048 MHz clock to be used as MCLK for the LXT332.

The stuffing jitter presented at TCLK is dependent on the E1 clock rate being fed to the SXT6234 demo board. Therefore, the LXT332 jitter attenuation performance should be tested with different E1 transmit clock rates coming from the HP3784 generator. Recommendation G.703 specifies that the E1 bit rate should be within ±50 ppm. The bit rate can be adjusted using the transmit clock offset feature on the HP3784A.

Figure 4. Test Setup for G.742 Conformance



3.0 LXT332 Typical Performance

Figure 5 presents the typical LXT332 jitter performance measured in the frequency band up to 100 KHz using the procedure described above. Data was taken using transmission clock offsets over the ±90 ppm range. This extended range gives some margin to account for the MCLK allowable variation relative to the nominal 2.048 MHz frequency (±50 ppm).

Figure 5. Typical LXT332 Performance