LXT30x Integrated Short-Haul Transceiver Crystal Layout Guidelines

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN046*.

Application Note

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1.0 General Description

Intel transceivers are designed for robust operation. Good PCB design practices also contribute to overall application reliability. This application note reminds design engineers of PCB layout considerations that will make LXT30x (LXT300Z, LXT304A, and LXT305A) transceiver applications even more effective.

The PCB designs should lay out the crystal input to any of these transceivers to minimize coupling of other digital and analog signals into XTALOUT and XTALIN. See the figure below. These inputs (pins 9 and 10 for all products included in this note) are high impedance nodes which can pick up interference from adjacent PCB traces and other components on the board. Adhering to these considerations will help ensure proper operation.

Before beginning a PCB design for any of the LXT300-series family transceivers, consider the following points:

- Use a crystal that meets the recommended crystal specifications (see the appropriate Data Sheet)
- Minimize the trace lengths between the transceiver and the 6.176 or 8.192 MHz crystal (typically less than 0.25 in or 6 mm)
- Shield these connections and the area around the crystal with ground planes
- Keep other high speed system clocks away from crystal leads and traces
- Locate all magnetic components well away from the crystal, its leads and traces

Keep all high energy signals away from crystal leads and traces connected to pins 9 and 10.

Figure 1. Crystal Layout for LXT30x Transceivers