LXT30x Transceiver/Framer Interface Application Guidelines for Use with Mitel MT8976 and MT8979 Framers

Application Note

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1.0 General Description

This application note provides guidelines for interfacing the Intel LXT30x series (LXT300Z, 301Z, 304A, 305A, and 307) transceivers with Mitel framers in both T1 and E1 applications. Only minimal circuitry is required to implement the interface. For T1 (1.544 Mbps) applications, the transmit data pins may be connected directly between the two chips as shown below. A single 4-gate NAND package provides the signal inversion required on the receive side.

Receive-side signal inversion is also required for E1/CEPT (2.048 Mbps) applications. A similar setup using NAND gates in an E1 application is shown in Figure 2. Additional circuitry is also required to synchronize the transmit data stream in E1 applications. This synchronization is easily implemented with a pair of D-flip-flops, clocked by the common 2.048 MHz transmit clock.

Figure 1. LXT30x Transceiver/Framer Interface

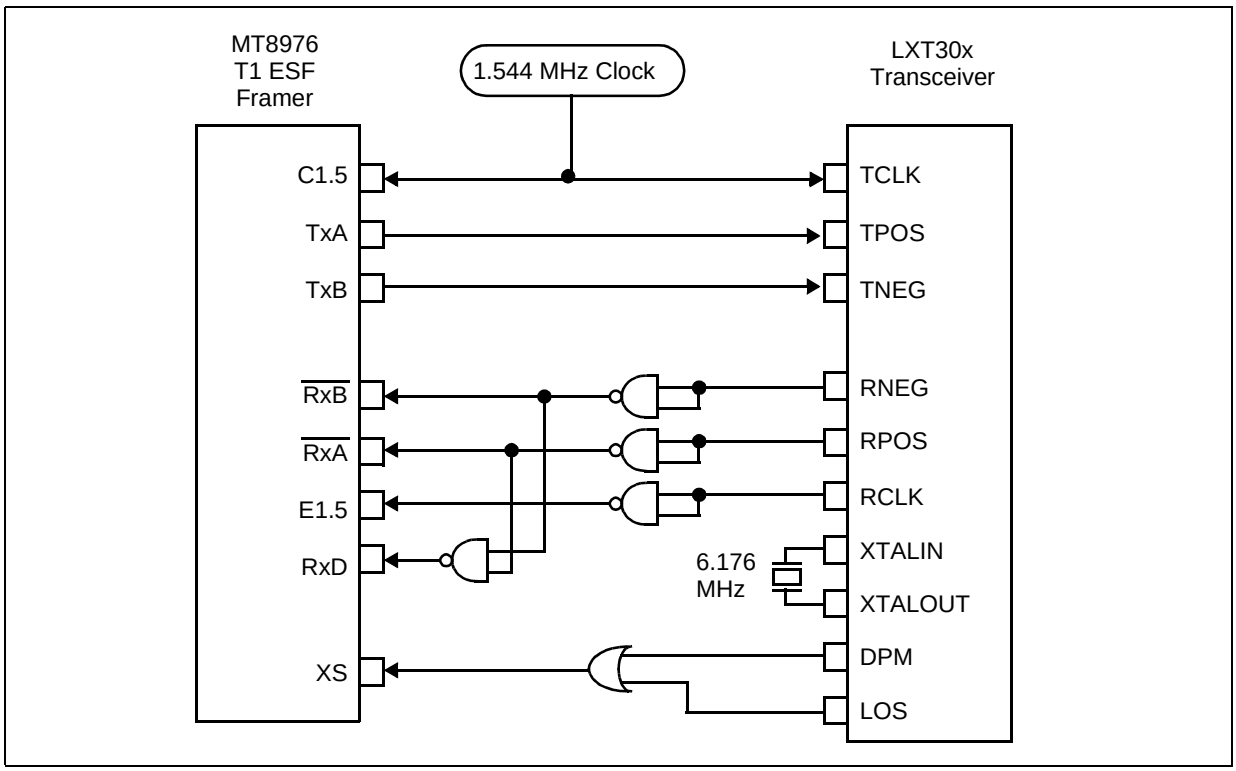

Figure 2. LXT300 Interface to MT8979 E1 CRC Framer