LXT380/1/4/6/8 Redundancy Applications

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN119*.

Application Note

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1.0 General Description

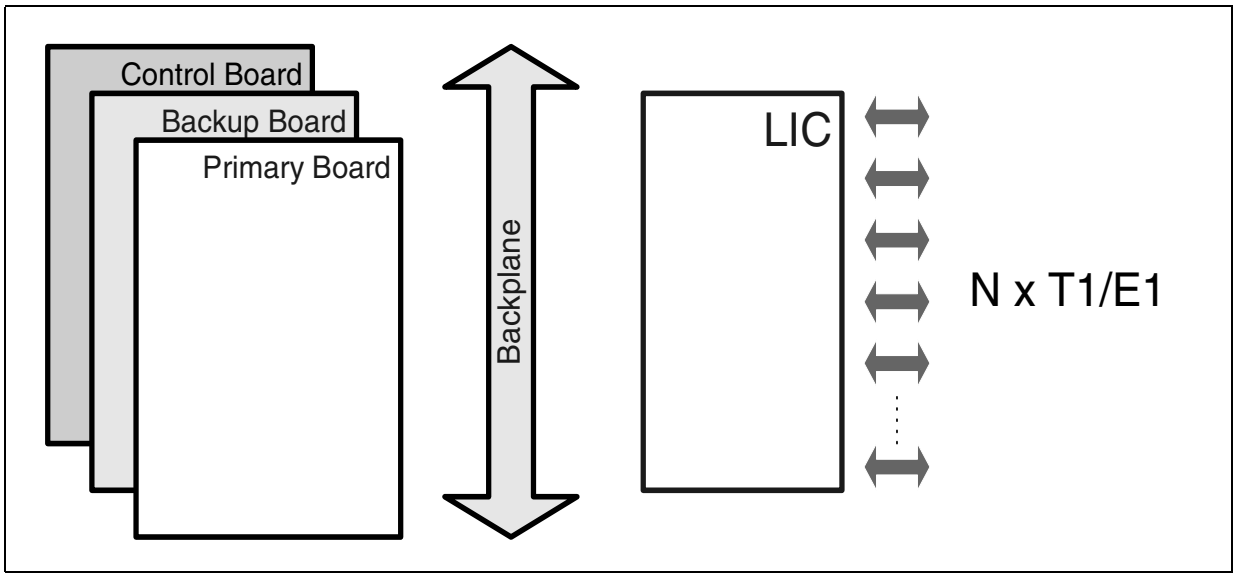
A primary concern in high-speed data networks is reliability. Today's telecommunication customers demand extremely high service quality with minimum or no periods of service failure. At the same time, international regulatory bodies are setting stringent standards for service quality. In this environment, telecommunication equipment manufacturers must take measures to ensure reliability of the critical network elements they develop. Redundancy is one way to ensure reliability in the event of board failure.

1.1 Features

In a typical T1/E1 system with redundancy protection, two independent boards, primary and backup, share a common backplane. In the event of failure in the primary board, all the T1/E1 circuits are switched to the backup board in a minimum amount of time.

Intel's LXT380/1/4/6/8 series of 3.3V T1/E1 HPS transceivers include an output driver tristatability feature for T1/E1 redundancy applications which do not require external relays. This feature greatly reduces the cost of implementing redundancy protection. In this application note, we provide some guidelines for implementing redundancy systems for both T1 and E1 operation using the LXT380/1/4/6/8.

Figure 1. Redundancy Protection



1.2 System Architecture

Figure 1 represents the typical architecture found in most T1/E1 systems with redundancy protection. This approach is common in rack based systems where several boards share a common backplane. The primary and backup boards are similar in function and access the same basic data signals. A separate Line Interface Card (LIC) includes the connectors and metallics that can be shared among the primary and backup boards. The common LIC approach reduces the cost in the

primary and backup boards by reducing the number of components duplicated in these cards. It also offers a simple mechanical solution for supporting several connector options and different line impedances (T1 100Ω and E1 120/75Ω). An independent control board supervises the system operation and determines which board (primary or backup) is being used. Naturally, depending on the equipment functionality, other boards may also exist.

In normal operation, the primary board is actively transmitting and receiving T1 or E1 signals. In this state, the backup board will be in "standby" mode with a minimum number of circuits activated. In the event of failure in the primary board, the control board will place it in "standby" mode and activate the backup board.

In a redundancy protection implementation it is crucial to ensure that the backup board does not load or alter the T1/E1 signal in the primary board. The fundamental electrical performance requirements such as pulse shaping receive sensitivity and return loss must still be met. In addition, switching between primary and backup board must be as fast as possible in order to minimize the number of bit errors.

As it will be shown in the following paragraphs, the LXT38x series of T1/E1 transceivers include several features that ease the design of redundancy protection implementations. These features guarantee excellent T1/E1 analog performance and minimize the switching time and associated number of bit errors.

1.2.1 LXT38x T1/E1 Transceiver Family

Intel's family of 3.3V T1/E1 transceivers includes the following members:

- LXT380: Octal E1 only LIU with clock recovery and hardware/software mode
- LXT381: Octal E1 only analog front-end with data recovery mode only. It operates only in hardware mode
- LXT384: Octal T1/E1 LIU with clock recovery and digital jitter attenuating (hardware/ software mode)
- LXT386: Quad T1/E1 LIU with clock recovery and digital jitter attenuating (hardware/ software mode)
- LXT388: Dual T1/E1 LIU with clock recovery and digital jitter attenuating (hardware/ software mode)

The appropriate LIU for a given application will depend on the system requirements (T1 or E1, need for jitter attenuation, etc.)

The following features included in these devices ease the development of redundant protection systems:

- Output tristating by freezing the TCLK signal
- Fast output tristating by using the OE pin
- Software controllable output driver tristate by using the OER register (LXT384/6/8 only)
- High receiver input impedance of 70 KΩ typ.
- Constant delay jitter attenuator (LXT384/6/8 only)

The driver tristate feature allows the designer to connect the redundant driver output in parallel with the primary driver output when one of them is tristated. Similarly, because the receiver impedance is very high, two receivers can be connected in parallel.

The constant delay jitter attenuator guarantees that, if a few conditions are met, the throughput delay in the primary and backup boards will be closely matched. This means that the number of bit errors resulting from switching boards will be minimized.

In the following paragraphs we will suggest solutions for the line interface circuit design using the LXT38x family. In the first section, we will cover the LXT380/1 in the context of E1 only applications. The following section suggests a T1/E1 solution using the LXT384/6/8. Finally, hitless switching is discussed in detail in the third section.

The following design recommendations were built and tested in the Intel engineering laboratory using the evaluation boards for the LIUs mentioned above.

1.2.2 LXT380/1 Redundancy Protection

In E1 only applications without jitter attenuator, the LXT380 and LXT381 are recommended. Since these devices use the same line interface circuitry, they will be both covered in this section.

1.2.2.1 Receive Line Interface

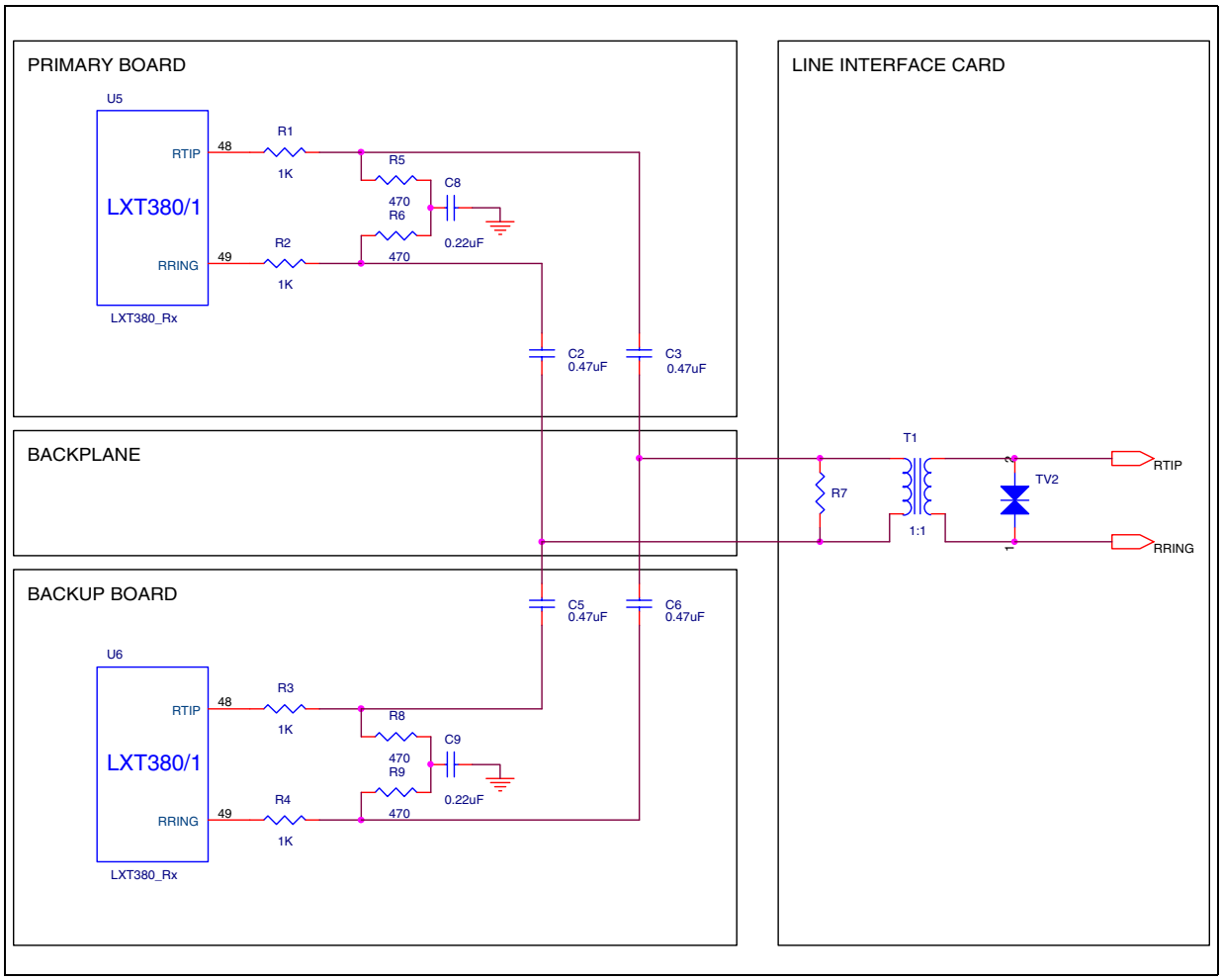
Figure 2 shows the recommended receive configuration for redundancy protection. For simplicity, only one channel is represented.

The LIC card contains the receive 1:1 transformer and the termination resistor R7. TV2 is a transient voltage suppressor. This device is recommended when there are stringent surge immunity requirements. In the primary and backup boards the series 1K resistors at the RTIP/RRING inputs further improve the surge and ESD immunity by decreasing the current coupled into the device. Primary and backup boards are connected together in the backplane and are capacitively coupled. Because of the high receiver input impedance, the backup board will not interfere with the primary board operation. Table 1 lists the components that were used in our tests for both 75Ω coaxial and 120Ω TWP cable (Twisted Pair Cable).

Table 1. Component List

Component	Coax Cable	TWP Cable
R7	90.9Ω ± 1%	162Ω ± 1%
TV2	LC03-6, Semtech (or equivalent)	
T1	S553-6500-55, Bel Fuse (or equivalent)	

Figure 2. LXT380/1 Receive Interface Circuit



1.2.2.2 Transmit Line Interface

Figure 3 represents the recommended transmit interface. The LIC contains the transmit transformer and 560 pF capacitor shared between the primary and backup boards. It also includes a first level of surge protection in the form of TV2. This protection is complemented by the Schottky diodes D1-D8 in each board. Note that the 11Ω resistors in the transmit interface do not need to be changed for coaxial/TWP cable operation. The output amplitude adjusts itself given the difference in the cable load impedance.

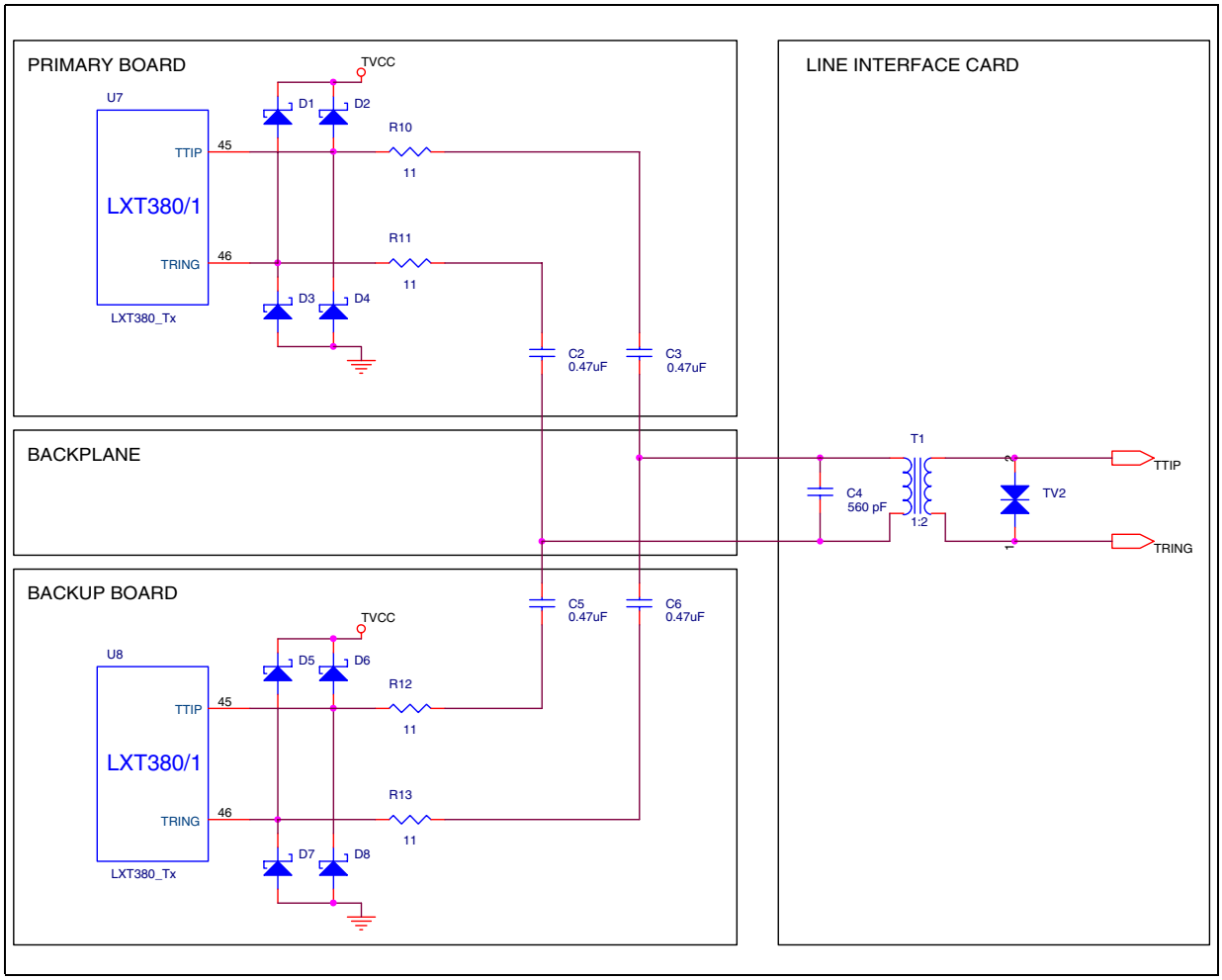
Primary and backup boards are connected in the backplane and are capacitively coupled. When tristated, the output driver impedance in the backup board is very high and will not affect the pulse shaping in the primary board.

Table 1 lists the components that were used in our tests for both 75Ω coaxial and 120Ω TWP cable.

Table 2. Component List

Component	Coax Cable	TWP Cable
D1-D8	MBR0540T1, Motorola (or equivalent)	
TV2	LC03-6, Semtech (or equivalent)	
T1	S553-6500-55, Bel Fuse (or equivalent)	

Figure 3. LXT380/1 Transmit Interface Circuit



1.2.2.3 Design Considerations

- *Minimize trace/cable lengths*. Longer cable lengths may reduce the output amplitude. In the experiments that were conducted, the cable connecting the primary, backup and LIC boards did not exceed 25cm. If longer cables are to be used, the transmit series resistors R10 - R13 may need to be reduced in order to compensate for the amplitude loss.

- *Minimize parasitic capacitance.* High parasitic capacitance will affect both the pulse shaping and return loss performance. The protection components chosen for this application note have a very low capacitance at the nominal operating voltage. Note that long cable lengths also add to the total parasitic capacitance. In some cases, the transmit capacitor C4 may have to be adjusted to optimize pulse shaping and transmit return loss performance.
- *Surge Immunity.* The protection elements recommended in Figure 2 and Figure 3 are sufficient for compliance with IEC 1000-4-5 (EN-6100-4-5) with up to 24A peak current on a 1.2/50 µs surge. If additional protection is required, a different line TVS may be necessary.
- *Place the TVS close to the connector.* Surge protection elements should be placed as close as possible to the disturbance source, i.e., the connector.
- *Include TVS protection in the power supply.* The protection diodes D1-D8 will couple current to the power supply in the event of a lightning surge. In order to protect other circuits on the board, a 3.3V TVS should be included in the power supply. A TVS suitable for this application is the SMLVT 3V3 from SGS-Thomson.
- *Avoid crossing transmit and receive signals:* this layout practice minimizes cross-talk.
- *Avoid routing digital signals near analog signals*: This is especially important near the receiver inputs as the cross-talk may induce bit errors.
- *EMI Filtering*: Some designs may require EMI filtering depending on the applicable emissions standards, total number of ports and shielding strategy. In these applications, common mode chokes may be added near the connectors.

1.2.2.4 Test Results

The circuits in Figure 2 and Figure 3 were tested using the LXD380/1 demo boards. The following performance parameters were tested for both coaxial and twisted pair cable:

- Receiver sensitivity per ITU-T G.703
- Pulse template per ITU-T G.703
- Receive Return Loss per ITU-T G.703
- Transmit Return Loss per ETSI ETS 300 166

Receiver Sensitivity

The devices were able to recover data correctly with cable attenuation up to 12 dB at 1.024 MHz. This figure greatly exceeds the 6dB minimum limit in ITU-T G.703.

Pulse Template

Figure 4 and Figure 12 represent the output pulses obtained for twisted pair cable and coaxial cable. During the tests, the backup boards were powered and the output drivers set to tristate mode.

Figure 4. Twisted Pair Cable Output

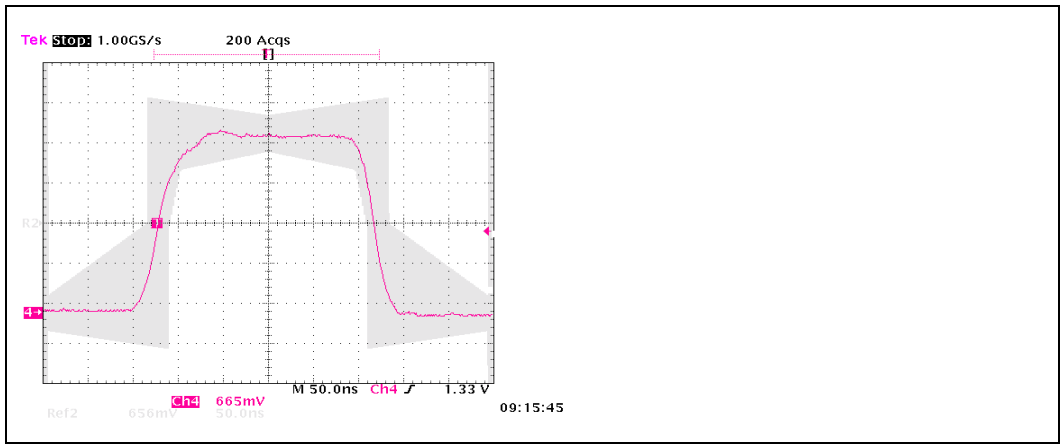
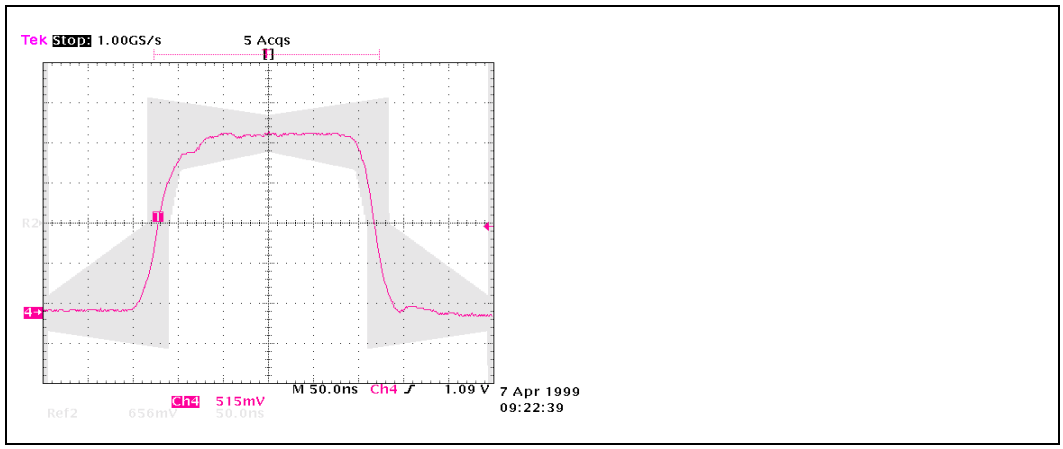


Figure 5. Coaxial Cable Output



Receive Return Loss

Figure 6 and Figure 7 represent the measured receiver return loss for both twisted pair cable and coaxial cable.

The results are compared against G.703 minimum requirements.

Figure 6. LXT380/1 Rx Return Loss, Twisted Pair Cable

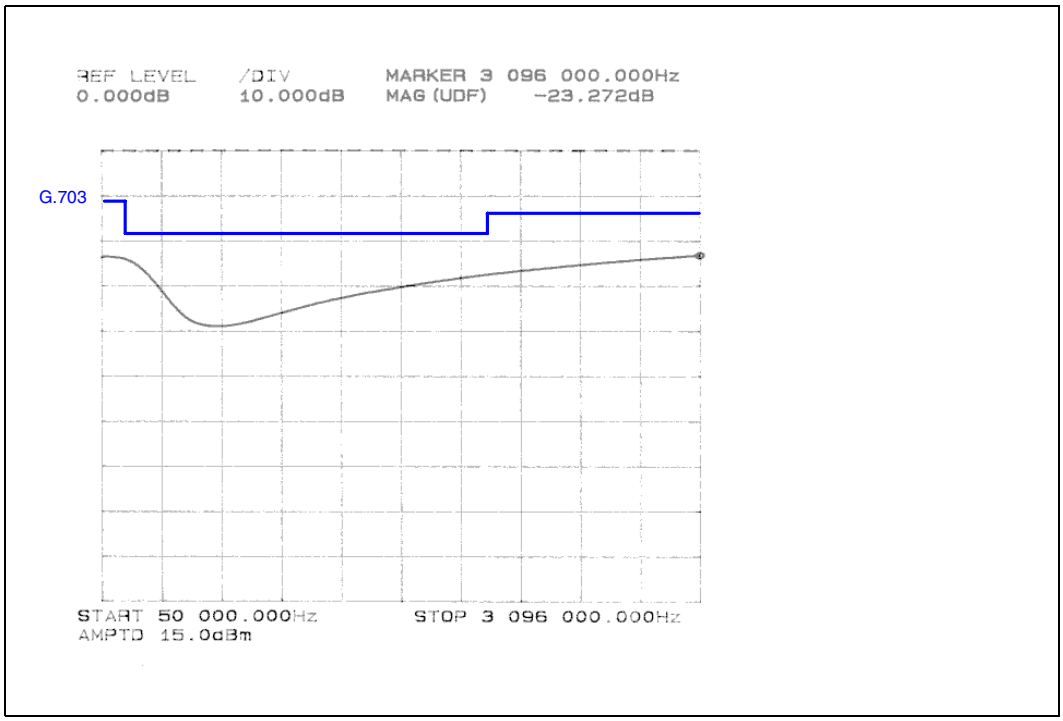
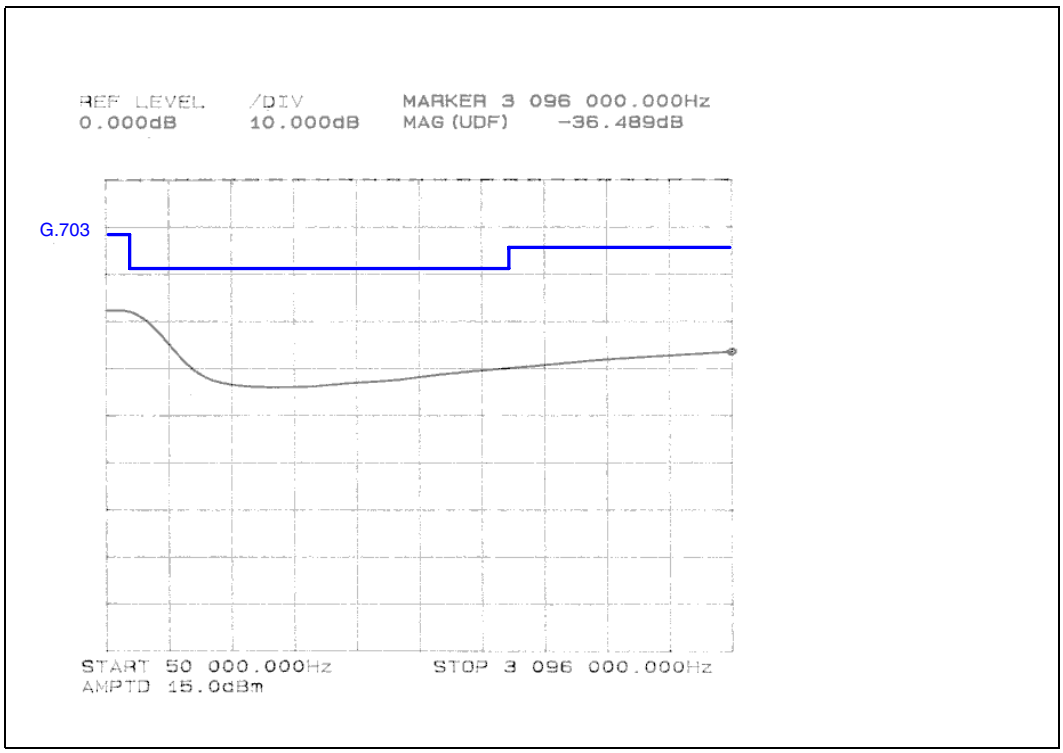


Figure 7. LXT380/1 Rx Return Loss, Coaxial Cable



Transmit Return Loss

Figure 8 and Figure 9 represent the measured transmit return loss for both twisted pair cable and coaxial cable.

The results are compared against ETSI ETS 300 166 requirements.

Figure 8. LXT380/1 Tx Return Loss, Twisted Pair Cable

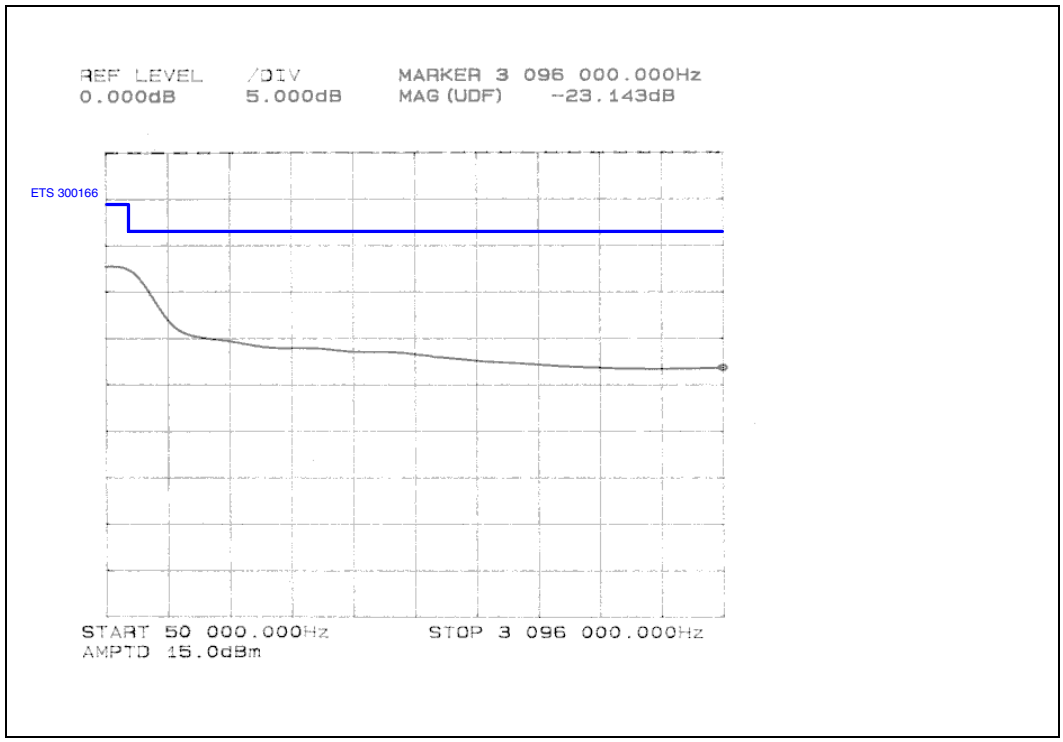
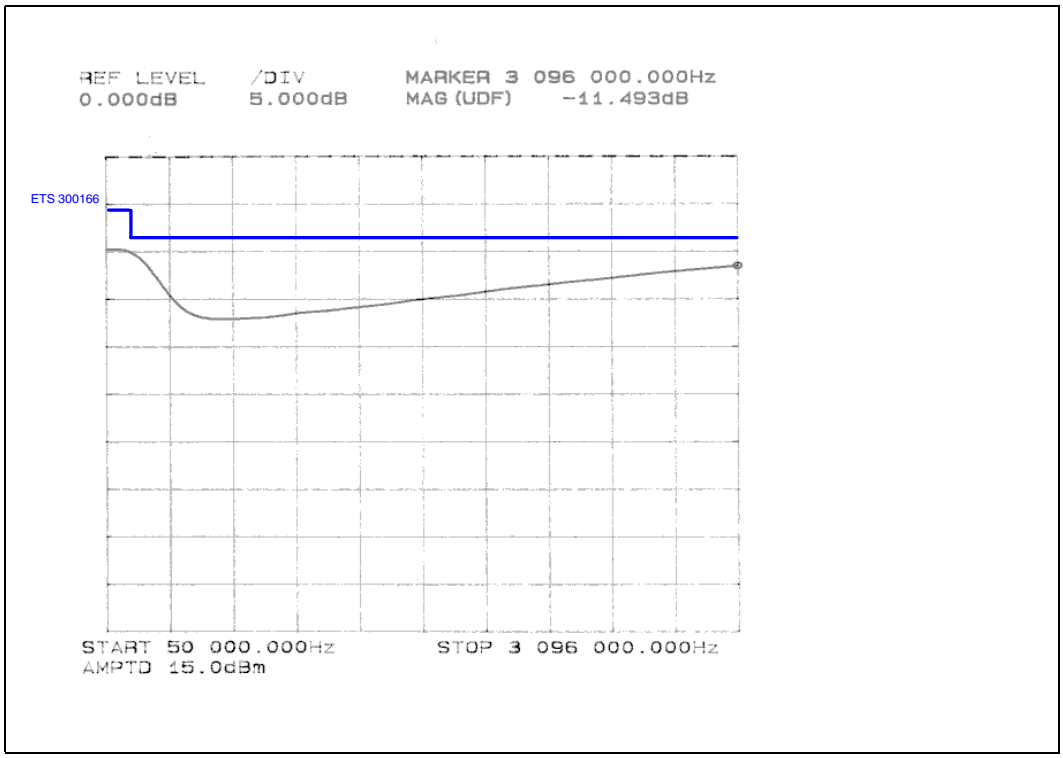


Figure 9. LXT380/1 Tx Return Loss, Coaxial Cable



1.2.3 LXT384/6/8 Redundancy Protection

In T1 only applications or T1/E1 applications requiring jitter attenuator, the LXT384/6/8 is recommended. The following paragraphs describe redundancy protection implementations using the LXT384/6/8.

1.2.3.1 Receive Line Interface

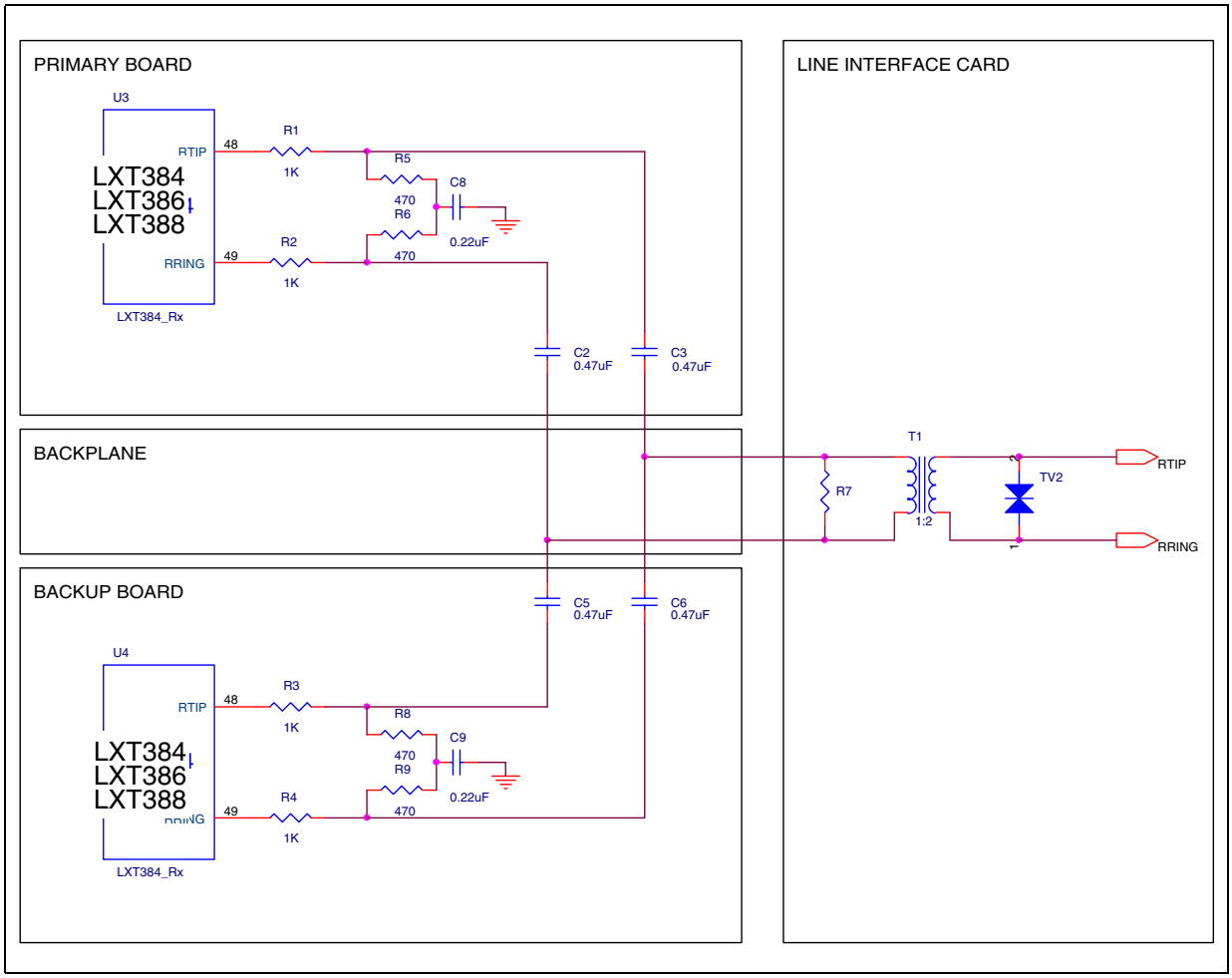
Figure 10 shows the recommended receive configuration for redundancy protection. For simplicity, only one channel is represented.

The LIC card contains the receive 2:1 transformer and the termination resistor R7. TV2 is a transient voltage suppressor. This device is recommended when there are stringent surge immunity requirements. In the primary and backup boards the series 1K resistors at the RTIP/RRING inputs further improve the surge and ESD immunity by decreasing the current coupled into the device. Primary and backup boards are connected together in the backplane and are capacitively coupled. Because of the high receiver input impedance, the backup board will not interfere with the primary board operation. Table 1 lists the components that were used in our tests for T1 100Ω and E1 75Ω coaxial / 120Ω TWP cable.

Table 3. Component List

Compon.	T1 TWP Cable	E1 Coax Cable	E1 TWP Cable
R7	26.1Ω ± 1%	19.6Ω ± 1%	32.4Ω ± 1%
TV2	LC03-6, Semtech (or equivalent)		
T1	S553-6500-55, Bel Fuse (or equivalent)		

Figure 10. LXT384/6/8 Receive Interface Circuit



1.2.3.2 Transmit Line Interface

Figure 11 represents the recommended transmit interface. For T1 operation, the transmitter power supply TVCC must be 5V in order to support series resistors. For E1 applications, TVCC can be either 3.3V or 5V.

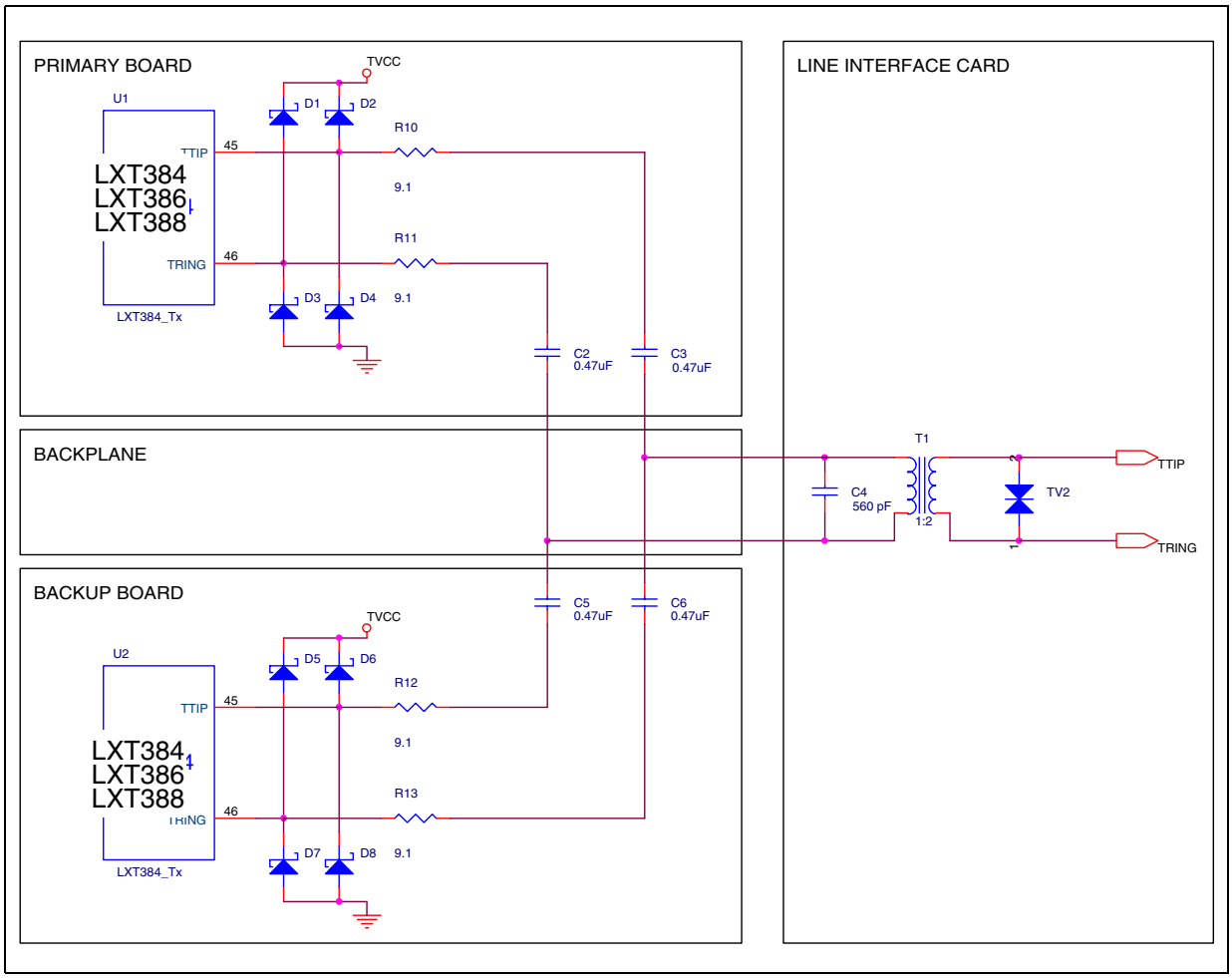
The LIC contains the transmit transformer and 560 pF capacitor shared between primary and backup board. It also includes a first level of surge protection in the form of TV2. This protection is complemented by the Schottky diodes D1-D8 in each board. For applications requiring the same design for T1 and E1, the resistors R10-R13 may be set to 9.1Ω (please refer to the LXT384 FAQ, question 2.11).

Primary and backup boards are connected in the backplane and are capacitively coupled. When tristated, the output driver impedance in the backup board is very high and will not affect the pulse shaping in the primary board. Table 1 lists the components that were used in our tests for both 75Ω coaxial and 120Ω TWP cable (Twisted Pair Cable).

Table 4. Component List

Component	T1 TWP Cable	E1 Coax Cable	E1 TWP Cable
R10-R13	9.1Ω ± 1%	11Ω ± 1% (see text)	
D1-D8	MBR0540T1, Motorola (or equivalent)		
TV2	LC03-6, Semtech (or equivalent)		
T1	S553-6500-55, Bel Fuse (or equivalent)		

Figure 11. LXT384/6/8 Transmit Interface Circuit



1.2.3.3 Design Considerations

Please refer to "Design Considerations" on page 9. The guidelines listed for the LXT380 should be observed when designing the LXT384/6/8. Note that the protection elements recommended for T1 are sufficient for compliance with Bellcore 1089 Intra-building lightning protection. If additional protection is required, a different line TVS may be necessary.

Test Results

The circuits in Figure 2 and Figure 3 were tested using LXD384 demo boards. The following performance parameters were tested:

- Receiver sensitivity
- Pulse template per ITU-T G.703 and ANSI T1.102
- Receive Return Loss per ITU-T G.703
- Transmit Return Loss per ETSI ETS 300 166

Receiver Sensitivity

The devices were able to recover data correctly with cable attenuation up to 12 dB at 772KHz. Note that this figure greatly exceeds the requirements in ANSI T1.102. This specification requires a minimum of 655ft of cable corresponding to approximately 3dB of attenuation at 772KHz.

Pulse Template

The circuits described above were tested for pulse template compliance in both E1 and T1 mode. During the tests, the backup boards were powered and the output drivers set to tristate mode

E1 Mode.

Figure 12 and Figure 13 represent the output pulses obtained for twisted pair cable and coaxial cable.

Figure 12. E1 Twisted Pair Cable Output

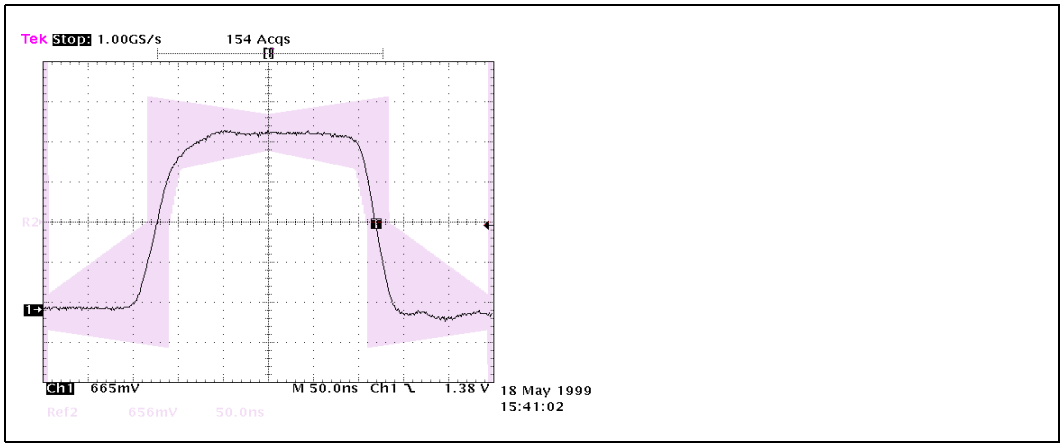
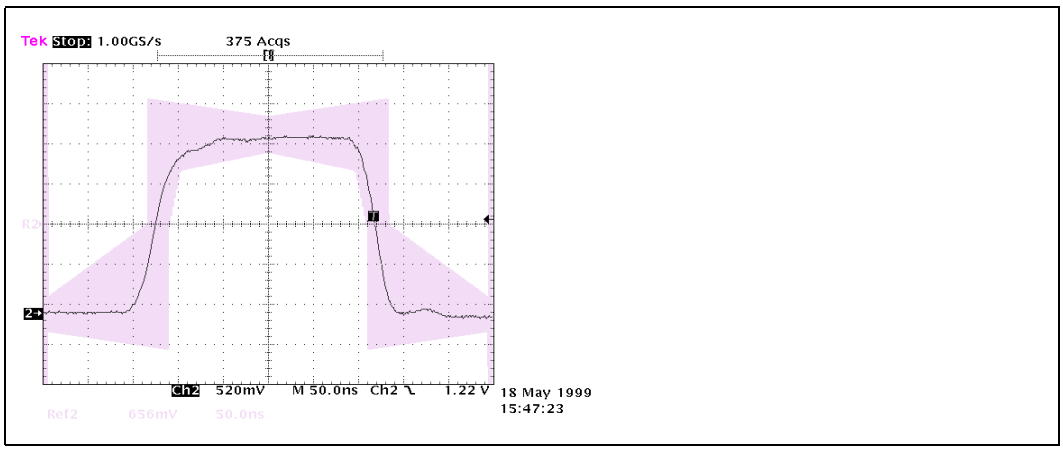


Figure 13. E1 Coaxial Cable Output



T1 Mode.

The configuration described in Figure 11 was tested successfully for all the possible cable length settings. Figure 14 and Figure 15 show the results for the two most extreme cases: no cable and maximum cable length.

Figure 14. T1 Output With 0ft of Cable

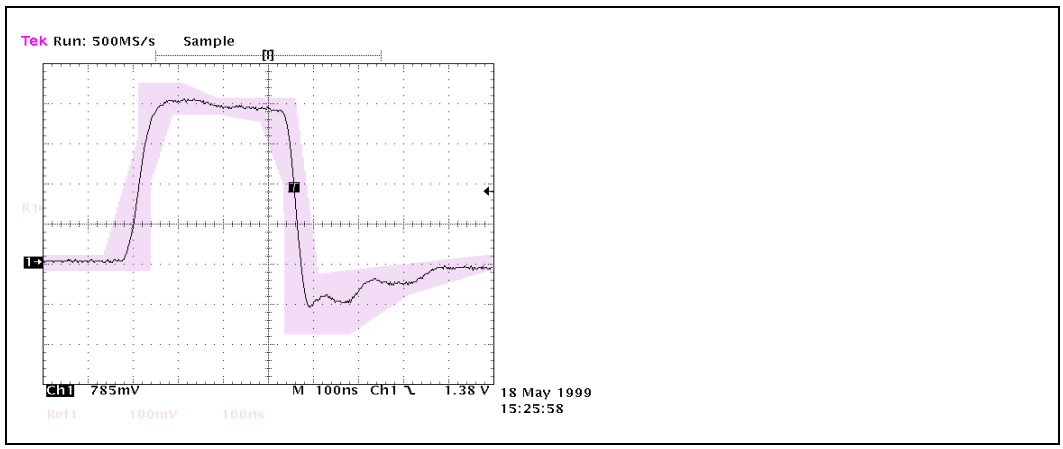
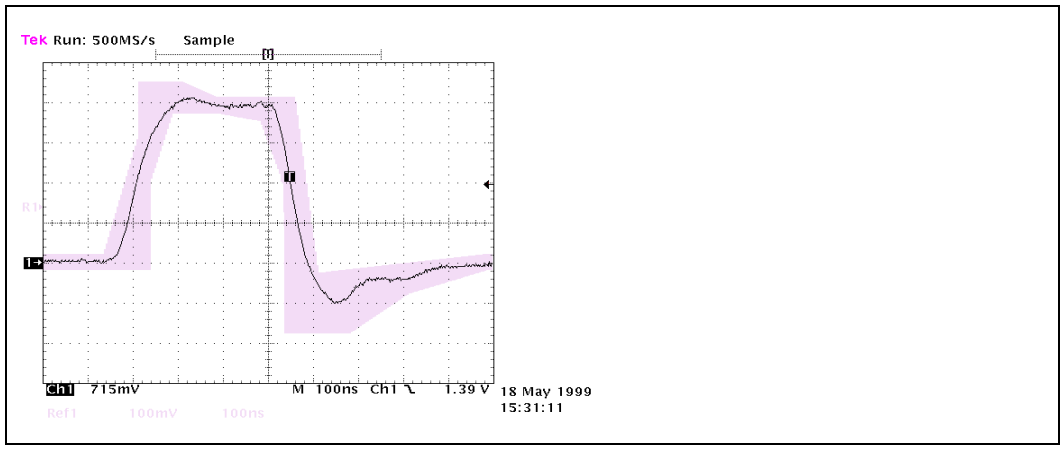


Figure 15. T1 Output With 655ft of Cable



Receive Return Loss

Figure 13 through Figure 15 represent the measured receive return loss for T1 and E1.

Although there are no receive return loss requirements for T1, the results are compared against G.703 minimum requirements.

Figure 16. LXT384 Rx Return Loss, E1 Twisted Pair Cable

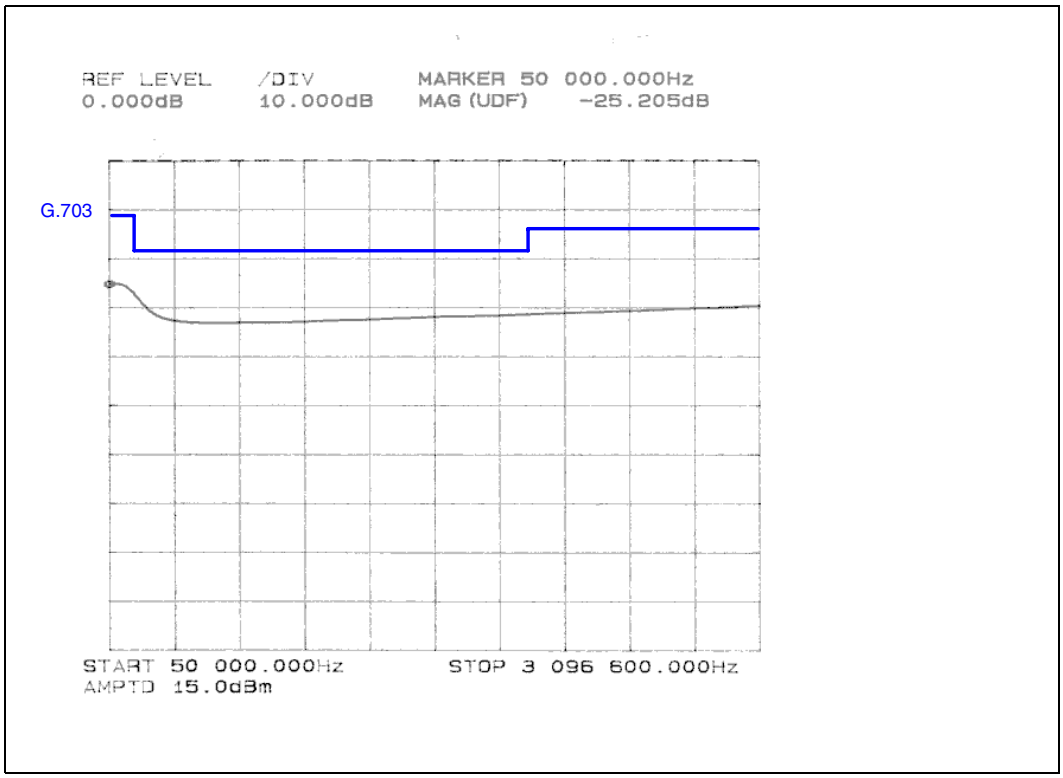


Figure 17. LXT384 Rx Return Loss, E1 Coaxial Cable

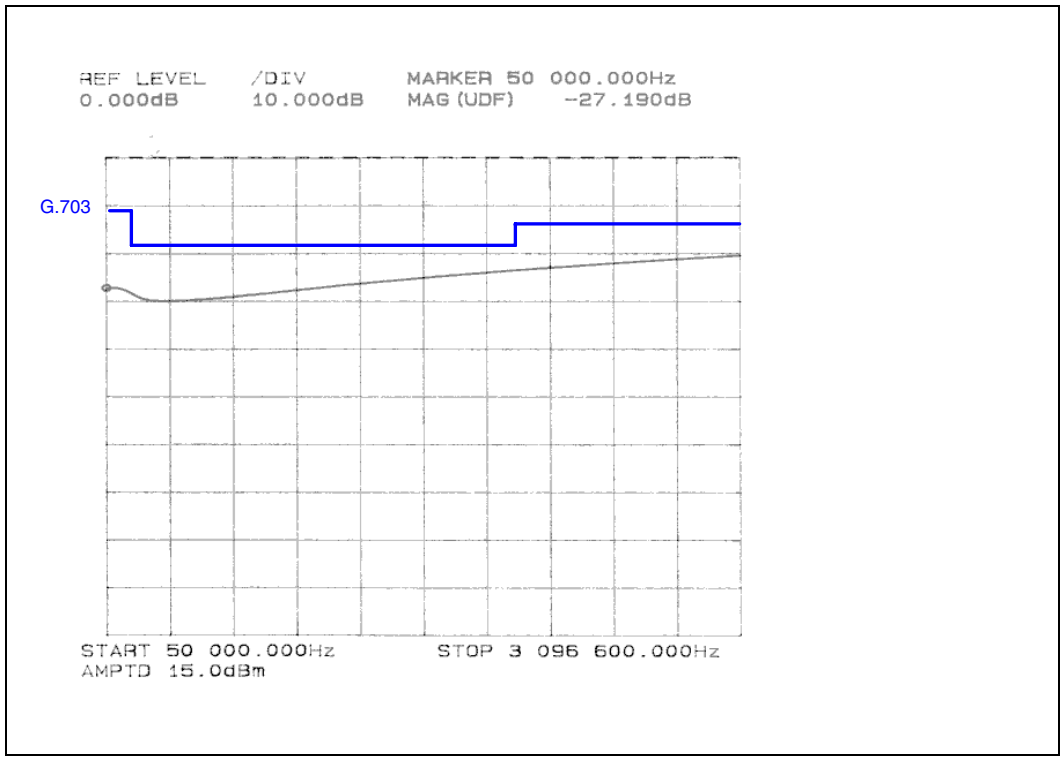
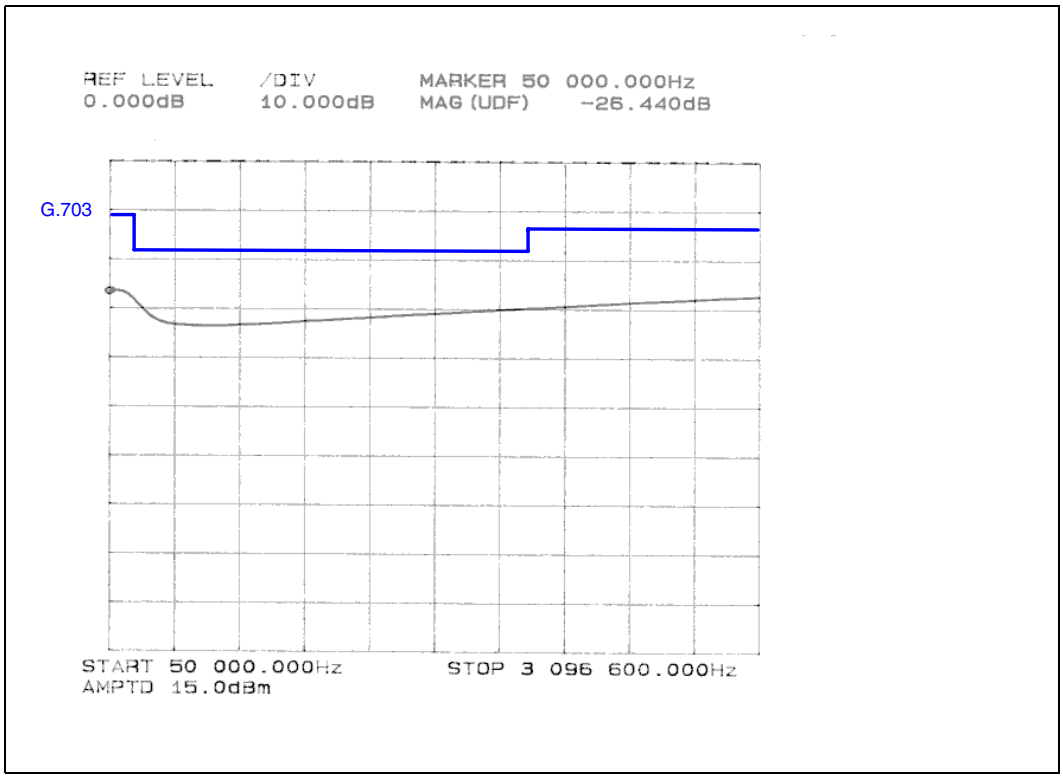


Figure 18. LXT384 Rx Return Loss, T1 Twisted Pair Cable



Transmit Return Loss

Figure 15 through Figure 17 represent the measured transmit return loss for both T1 and E1. Although there are no transmit return loss requirements for T1, the results are compared against ETSI ETS 300 166 requirements.

Figure 19. LXT384 Tx Return Loss, E1 Coaxial Cable

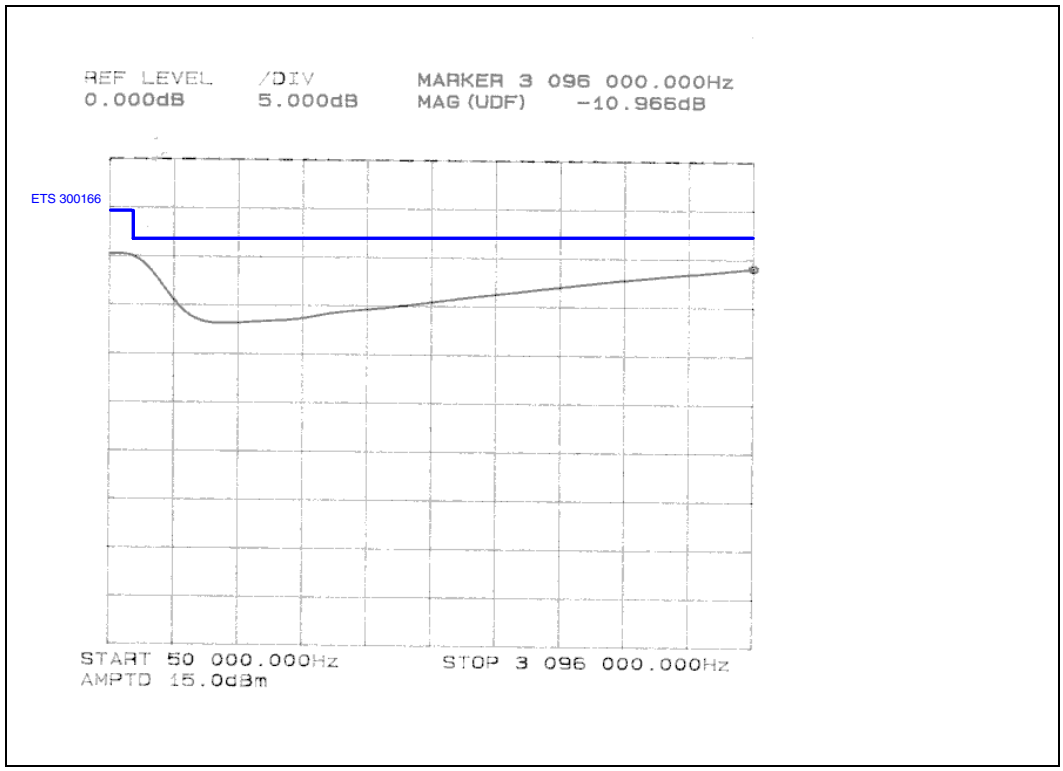


Figure 20. LXT384 Tx Return Loss, E1 Twisted Pair Cable

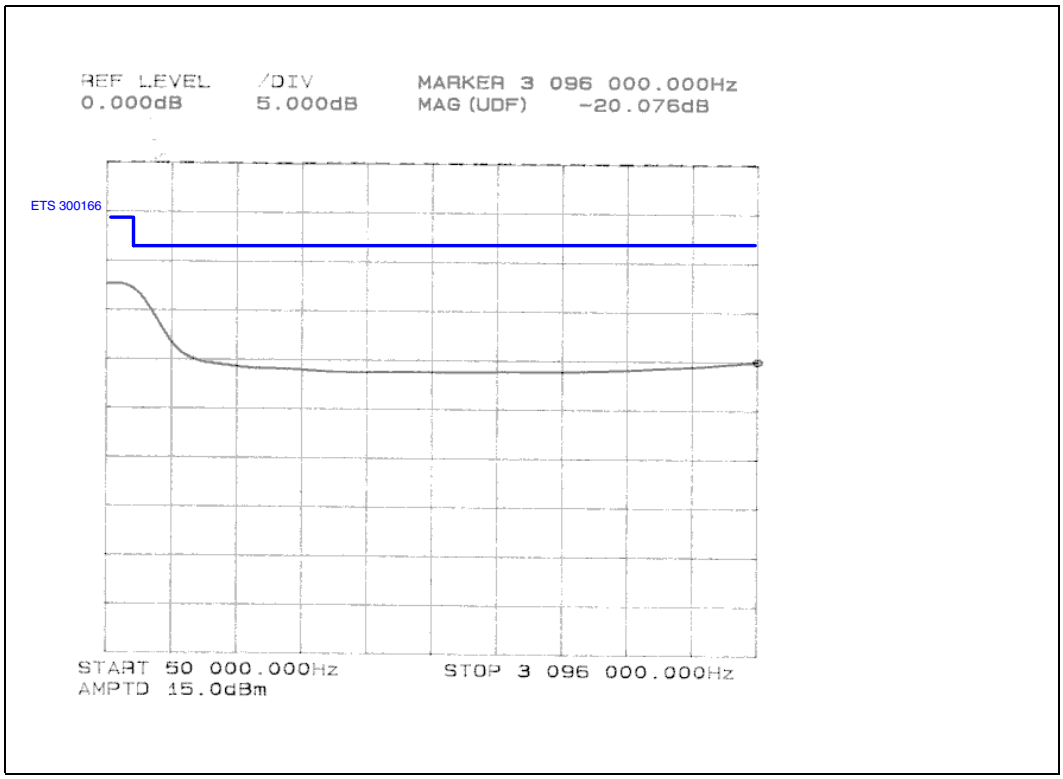
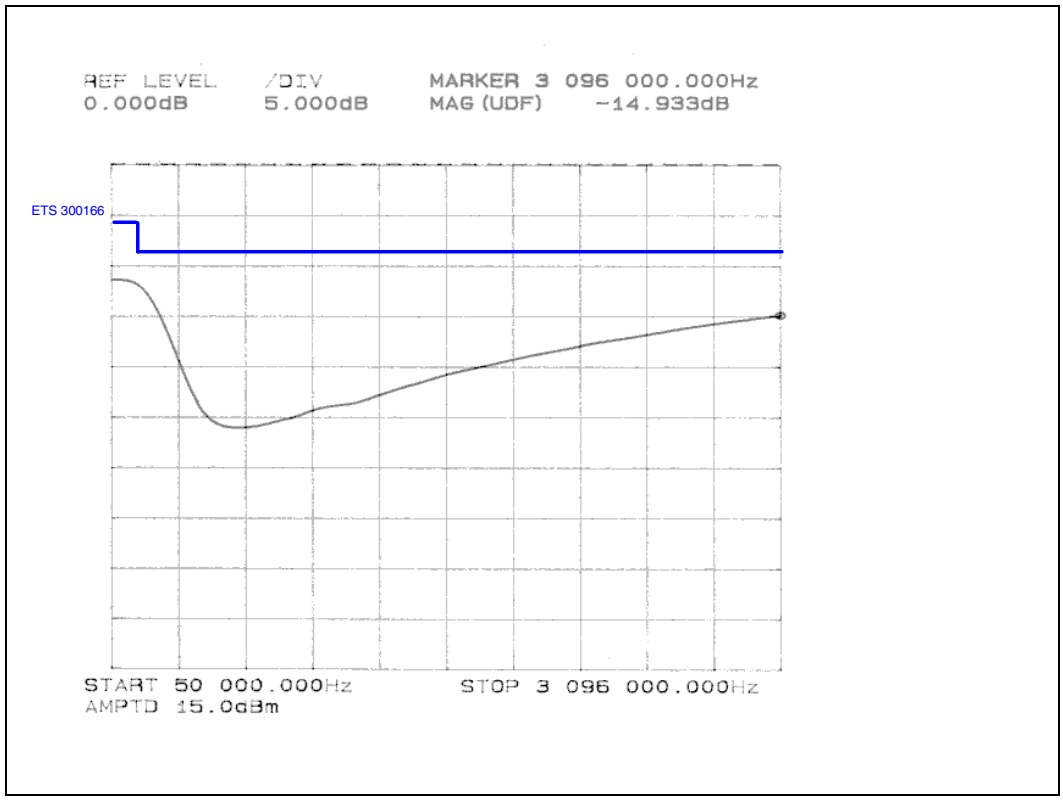


Figure 21. LXT384 Tx Return Loss, T1 Twisted Pair Cable



1.2.4 Hitless Protection Switching (HPS)

In most current redundancy protection implementations, switching between primary and backup boards is performed using mechanical relays. Because the switching time in relays is typically in the millisecond range, T1/E1 hitless switching is virtually impossible. The switching event will likely cause frame synchronization loss in the equipment downstream severely affecting the quality of service. The above is also true for tristating mechanisms triggered by software or triggered by inactivity in a given transmission clock.

The LXT38x series of transceivers includes a fast tristatability feature that allows switching between boards in less than 1 microsecond. Furthermore, by including a constant delay jitter attenuator in the LXT384/6/8, hitless switching applications requiring jitter attenuation can also be implemented.

The following paragraphs show that HPS can be achieved using the interface circuits described in the previous sections.

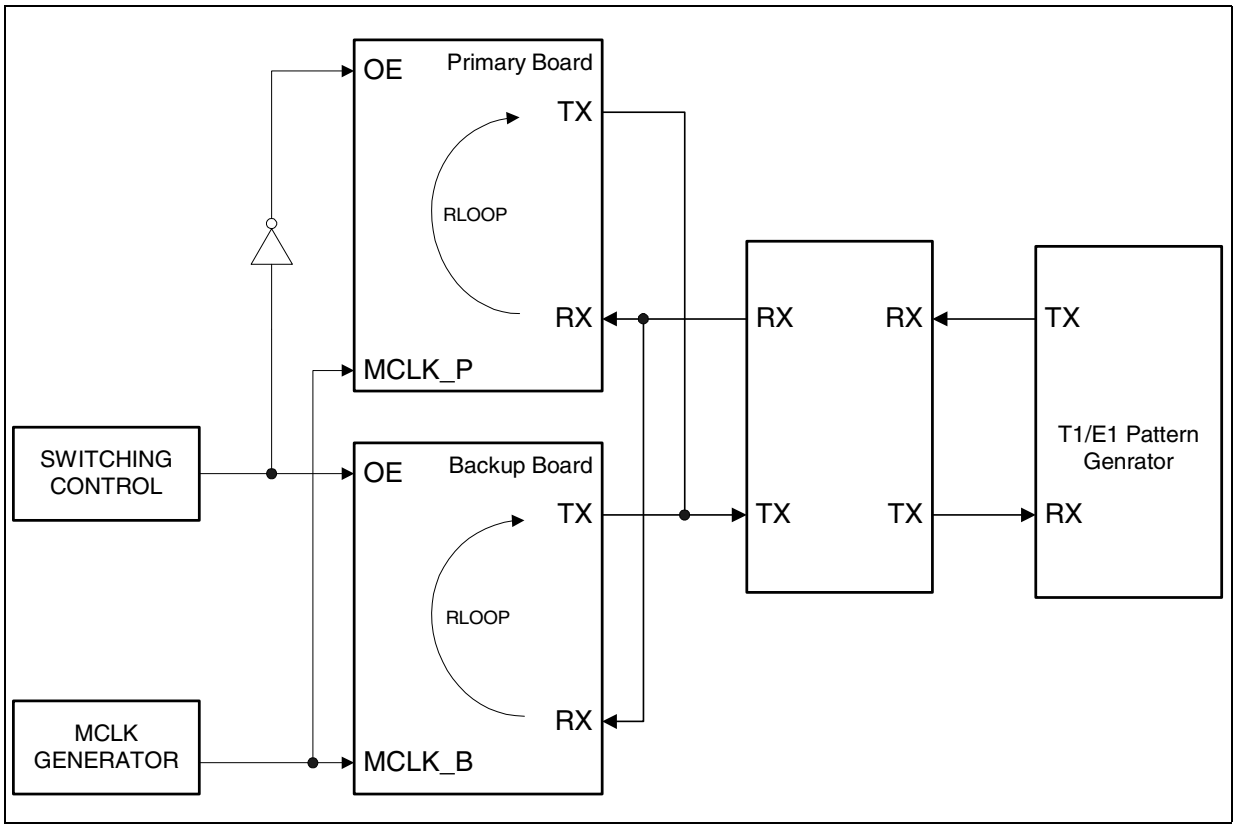
1.2.4.1 Test Setup

Figure 22 represents the setup used for hitless switching testing. A standard T1/E1 pattern generator/analyzer transmits a framed pseudo-random pattern (2^15-1 in E1, 2^20-1 in T1). Both the primary and the backup boards receive this pattern. The boards were set to retransmit the signals (Remote Loopback). A clock generator was used to provide MCLK references to the LXT384 LIUs.

One of the boards is kept active while the other board's driver is tristated (OE=Low). The "switching control" block, in this case a simple clock generator, determines which board is active at any given point in time. In order to obtain statistics on the number of bit errors caused by a switching event, the switching control block was set to generate a 50 Hz clock. This effectively generates 100 switching events per second.

The pattern analyzer was used to keep track of the number of bit errors and to verify frame synchronization status.

Figure 22. Hitless Switching Testing



1.2.4.2 Test Conditions

- Input frequency range: +/- 50 ppm.
- MCLK frequency range: +/- 100 ppm.
- Room temperature.
- Nominal power supply voltage.
- Jitter attenuator enabled in the LXT384.
  Since the device was set to a remote loopback it is not relevant whether the jitter attenuator is placed in the transmit or receive path.
- Jitter added to the input signal:
  The input E1 and T1 input signals were modulated with sinusoidal jitter. The tests were performed at the following jitter frequency/amplitude points:

Table 5. Jitter Test Points

Jitter Frequency	Jitter Amplitude
1 Hz	10 UI
10 Hz	10 UI
100 Hz	10 UI
1 KHz	2 UI
10 KHz	0.5 UI
100 KHz	0.3 UI

1.2.4.3 Test Results

The following results were obtained using the setup in Figure 22 for both T1 and E1 operation:

- Maximum number of errors per switching event: 1 error.
- Probability of an error during a switching event: 50%.
- No frame synchronization loss.

Note that the standard frame synchronization algorithms require errors in two or more consecutive frame alignment words in order to declare loss of frame synchronization. Since the number of errors is limited to one, frame loss will not be declared.

1.2.4.4 Design Considerations

- LXT384/6/8 *MCLK source*. The delay through the jitter attenuator depends on the frequency offset between MCLK and the input signal. In order to guarantee that the delays will be closely matched, there should be a common source for all the MCLK inputs in both the primary and backup boards (Figure 22). This is not a requirement for applications that do not need jitter attenuation.
- *Board delay*. The tests described above were performed using only the line interface units. In a specific system implementation, other components on the board may introduce delays. These delays and how they vary from board to board should be taken into account as they may affect the maximum number of bit errors.

1.3 Conclusions

The results presented in this application note demonstrate that the LXT38x series of LIUs greatly reduce the effort in the design of T1/E1 redundancy protection systems. The tristatable drivers enable designs without costly mechanical relays. Furthermore, as it was shown in the previous section, hitless switching can be achieved by using the fast tristating feature and the constant delay jitter attenuator. By taking advantage of these features, cost-effective protection switching systems can be designed while maintaining excellent electrical performance.