LXT6234 E-Rate Multiplexer

Application Note

January 2001

For 16 E1/E3 Multipexer/Demultiplexer

Order Number: 249313-001

As of January 15, 2001, this document replaces the Level One document *AN9501*.

Application Note

Contents

Figures

Tables

1.0 General Description

The LXT6234 E-Rate Multiplexer offers a simple and economic approach to building E1/E2, E2/E3 and E1/E3 multiplexers and demultiplexers. This application note provides the system designer with a 16E1/E3 multiplexer/demultiplexer design example.

A brief overview of fundamental E1/E3 protocol is included to establish a common reference with readers. For additional information, refer to the ITU-T General Aspect of Digital Transmission Systems, Recommendations G.700-G.772. Related documentation includes the LXT6234 Data Sheet and the LDB6234 E1/E3 Demo Board User Guide.

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1.1 Standards

The International Telecommunication Union - Telecommunication Standardization Sector (ITU-T) standardized the E1, E2, and E3 specifications. The ITU-T was formerly known as the Consultive Committee for International Telephone and Telegraph (CCITT).

1.2 E Standard European Hierarchy

To accommodate higher transmission speeds, carriers developed the hierarchy levels shown in Table 1.

Table 1. E Standard Hierarchy

Level Number	System	Number of Voice Circuits	Bit rate Mbps
1	E1	30	2.048
2	E2	120	8.448
3	E3	480	34.368
4	E4	1920	139.264

1.3 E1 Standard

The E1 standard was designed to support transmission of 30 digitized voice channels. Analog-Digital conversion of each channel is based on the Nyquist sampling theory. This theory says that to digitize an analog signal so that it contains sufficient information to allow an accurate analog reconstruction, the signal must be sampled at a frequency that is at least twice the channel bandwidth. Sampling 8,000 per second is the industry-accepted rate. This rate allows the accurate reproduction of a voice-grade 4-kHz bandwidth channel.

The 8 kHz sampling produces a series of narrow pulses with a 125 microseconds (µsec) period. The magnitude or height of each analog sample is digitally encoded as an 8 bit binary value. Furthermore, the sampling pulse has a duration of less than 4 µsec during the 125 µsec period. Consequently, it is possible to interleave sampled pulses from other signals within the 125 µsec

period. The E1 standard interleaves 32 channels; 30 channels transmit digitized analog signals, and the remaining two channels send signaling and synchronization information. As shown in Table 2, each channel is assigned a specific time-slot.

Table 2. E1 Frame

Time slot	Type of information
0	Synchronization
1-15	Speech
16	Signaling
17-32	Speech
1. Frame length = 256 bits 2. Frame duration = 125 µsec 3. The 32 time slots constitute a frame. Each slot is 8 bits. Consequently one frame is: 4. 8 bits x 32 time slots = 256 bits/frame 5. Since 8000 frames are transmitted each second, the bit rate is: 256 bits /frame x 8000 frames/second = 2.048 Mbps.	

1.4 E2 Standard

The second level is the E2 standard. The E2 standard multiplexes four E1 channels into a single 8.448 Mbps channel (4 X 2.048 Mbps = 8.448 Mbps). Two recommendations, defined in ITU-T G.742 and G.745, exist for this multiplexing. The G.742 for the LXT6234 is shown in Table 3. The G.742 uses positive justification and is intended for digital paths between countries.

Table 3. E2 Frame Bit Assignments

Bit Number	Bit Number by Set	Type of Information
1-10	1-10	Frame alignment
11	11	Alarm indication signal to the remote multiplex equipment
12	12	Bit reserved for national use
13-212	13-212	Bits from tributaries
213-216	1-4	Justification control bits Cj1
217-424	5-212	Bits from tributaries
425-428	1-4	Justification control bits Cj2
429-636	5-212	Bits from tributaries
637-640	1-4	Justification control bits Cj3
641-644	5-8	Bits from tributaries available for justification
645-848	9-212	Bits from tributaries available for negative justification

Table 4. E2 Frame

Standard	G 742
Bit rate	8.448 Kbits/s
Frame length	848 bits

Table 4. E2 Frame

Standard	G 742
Frame duration	100.39 µsec
Bits per tributaries	205 bits
Maximum justification rate per tributaries	10 Kbit/s

1.5 E3 Standard

The third level is the E3 standard. The nominal bit-rate of 34.368 Mbps is the result of the multiplexing of four 8.448 Mbps E2 channels.

Table 5. E3 Frame Bit Assignments

Bit Number	Bit Number by Set	Type of Information
1-10	1-10	Frame alignment
11	11	Alarm indication to remote digital multiplex equipment
12	12	Bit reserved for national use
13-384	13-384	Bits from tributaries
385-388	1-4	Justification service bits Cj1
389-768	5-384	Bits from tributaries
769-772	1-4	Justification service bits Cj2
773-1152	5 -384	Bits from tributaries
1153-1156	1-4	Justification service bits Cj3
1157-1160	5-8	Bits from tributaries available for justification
1161-1536	9-384	Bits from tributaries

Table 6. E2 Frame Bit Usage

# of bits	10	1	1	200	4	208	4	208	4	4	204
Usage	Frame	AIS	NAT	E1	Jus	E1	Jus	E1	Jus	Aux	E1

Table 7. E3 Frame Bit Usage

# of bits	10	1	1	372	4	380	4	380	4	4	376
Usage	Frame	AIS	NAT	E2	Jus	E2	Jus	E2	Jus	Aux	E2

1.6 Multiplexing Method

The multiplexing method uses cyclic bit interleaving in the tributary numbering order. This conforms with the positive justification recommendation of ITU-T G.742 and G.751.

Table 8. E3 Frame

Standard	G.751
Bit rate	34 368 kbit/s
Frame length	1536 bits
Frame duration	44.7 µsec
Bits per tributaries	378 bits
Maximum justification rate per tributary	22.375 kbit/s

1.7 Justification

Justification is the process of changing the data rate of a digital signal from its inherent rate to a different rate without loss of information. Positive justification is a method by which the data rate used to convey a signal has a higher bit-rate than the original signal. Positive justification is normally achieved by assigning some time-slots per frame to handle the additional information that may result from justification. If signal justification is unnecessary, these time-slots may contain regular channel information or they might remain empty. The justification service digits indicate if these time-slots contain information digits or justifying digits. The justification control signal in E standard is defined by the Cjn bits (see E2 and E3 frame tables). Three bits are used to show the type of justification; the fourth bit is the stuffing bit.

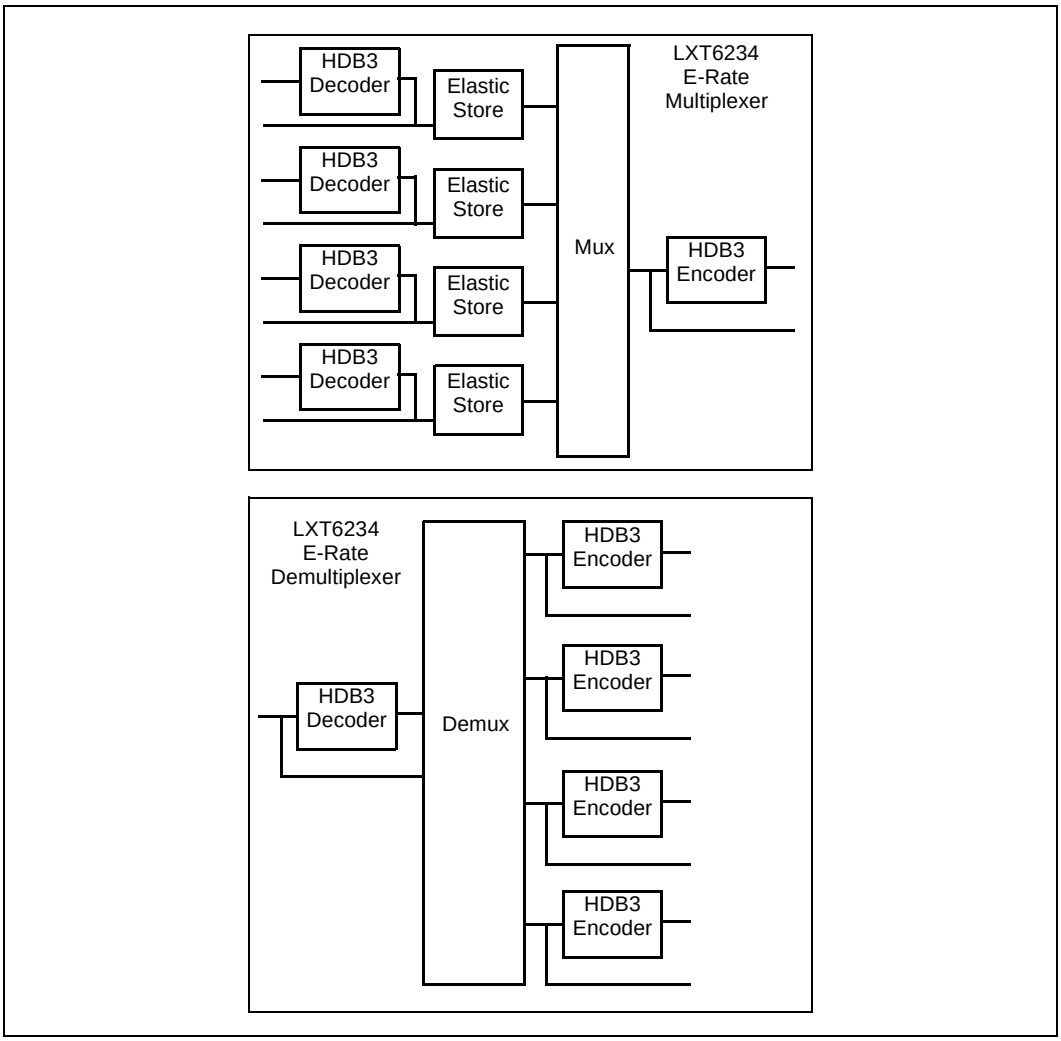
1.7.1 The E-Rate Multiplexer

The LXT6234 is a single-chip solution for multiplexing four tributaries into one high speed bit stream and the demultiplexing of the high speed bit stream back into four tributaries. All required circuitry has been integrated into the LXT6234; there is no need for an external framer.

The LXT6234, fabricated with 0.5-micron CMOS technology, is packaged in a 100-pin PQFP package. This device consists of the multiplexer block, the demultiplexer block, four HDB3 Encoder/Decoders for each tributary, and one HDB3 Encoder/Decoder for the high speed stream.

- The LXT6234 supports two multiplexing formats: One multiplexes four E1 channels into one E2 channel. The other format multiplexes four E2 channels into one E3 channel. Both are fully compliant with ITU-T recommendations, G.742 and G.751 respectively.
- All CODEC I/O pins are externally accessible, allowing either HDB3 or NRZ I/O to the multiplexer and demultiplexer. Alternatively, the LXT6234 can be used as a 5-channel HDB3 CODEC.
- Access is provided to the Alarm Indication Signal (AIS) and the National Bit.
- Four auxiliary low speed data or flag channels are available via the stuffing bits on each tributary channel.

Figure 1. LXT6234 E-Rate Multiplexer



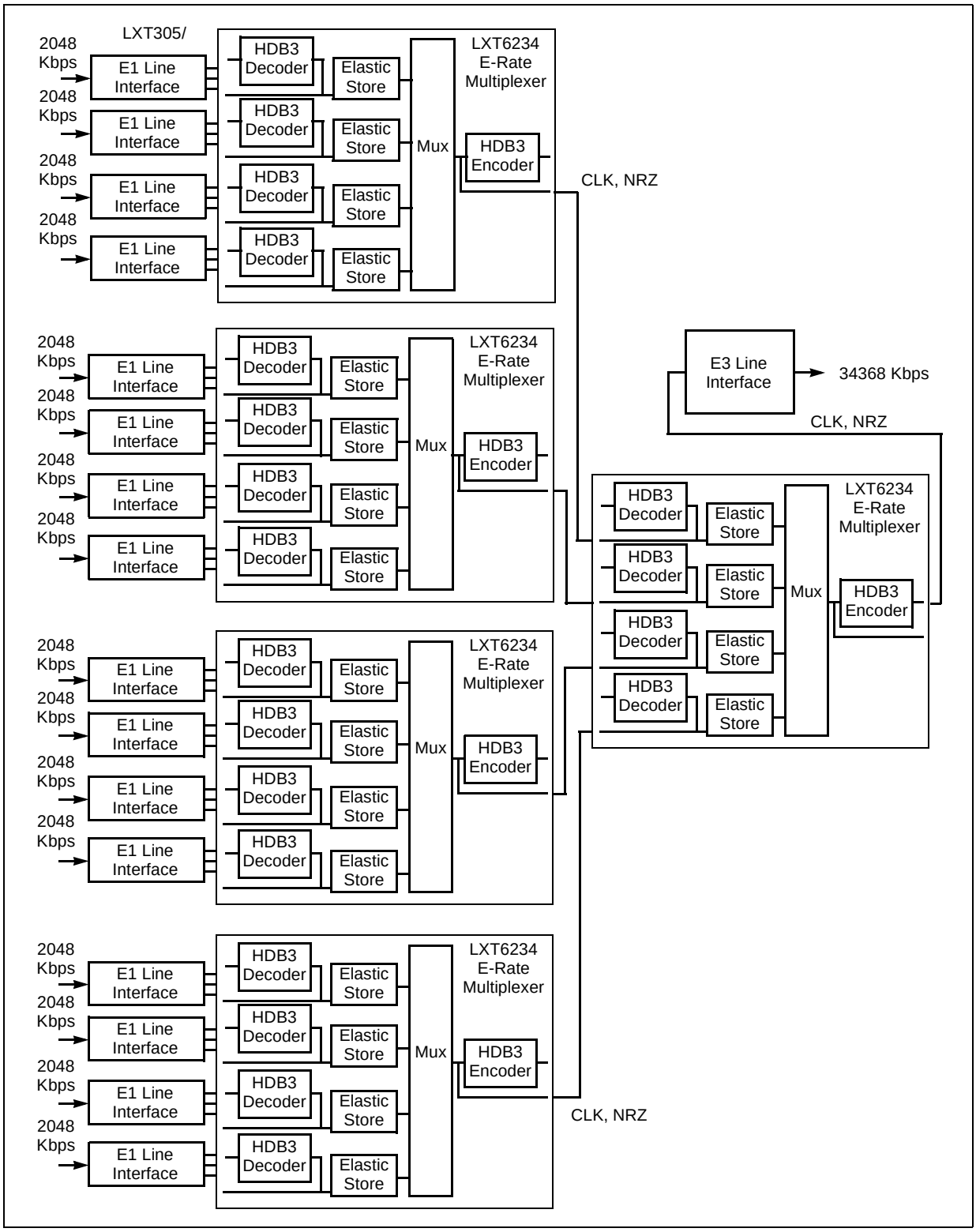
1.7.2 E1/E3 Multiplexer Block Diagram

The block diagram of the E1/E3 Multiplexer is shown in Figure 2.

1.7.2.1 E1 line Interface

- Receive clocks from the pulse data.
- Accepts either HDB3 encoded signals (clocks along with positive and negative RZ data), or NRZ data (clock and data). This depends on whether the Line Interface Unit (LIU) performs HDB3 coding.

Figure 2. E1/E3 Multiplexer



1.7.2.2 LXT6234, E1/E2 Stage

- If the tributary LIU does not perform HDB3 decoding, then the signals are routed to the LXT6234 onboard HDB3 decoder. The inputs are the clock and the decoder data input signals (both positive and negative). The onboard HDB3 decoder then outputs NRZ data and clock to the Elastic Store of the multiplexer portion of the LXT6234.
- If the LIU provides HDB3 decoding, then the NRZ data and clock are sent directly to the elastic store of the multiplexer portion of the LXT6234 via the external pin.
- Each four-tributary group is interleaved into a single, intermediary E2 data stream. An onboard crystal oscillator drives the data from the multiplexer at the E2 rate of 8.448 MHz. A bit stuffing algorithm implemented in the LXT6234 ensures tributary rate integrity at the output. The LXT6234 contains elastic store buffers to manage the bit-stuffing process.
- The NRZ data is sent to a tributary of the E-Rate Multiplexer, stage E2/E3.

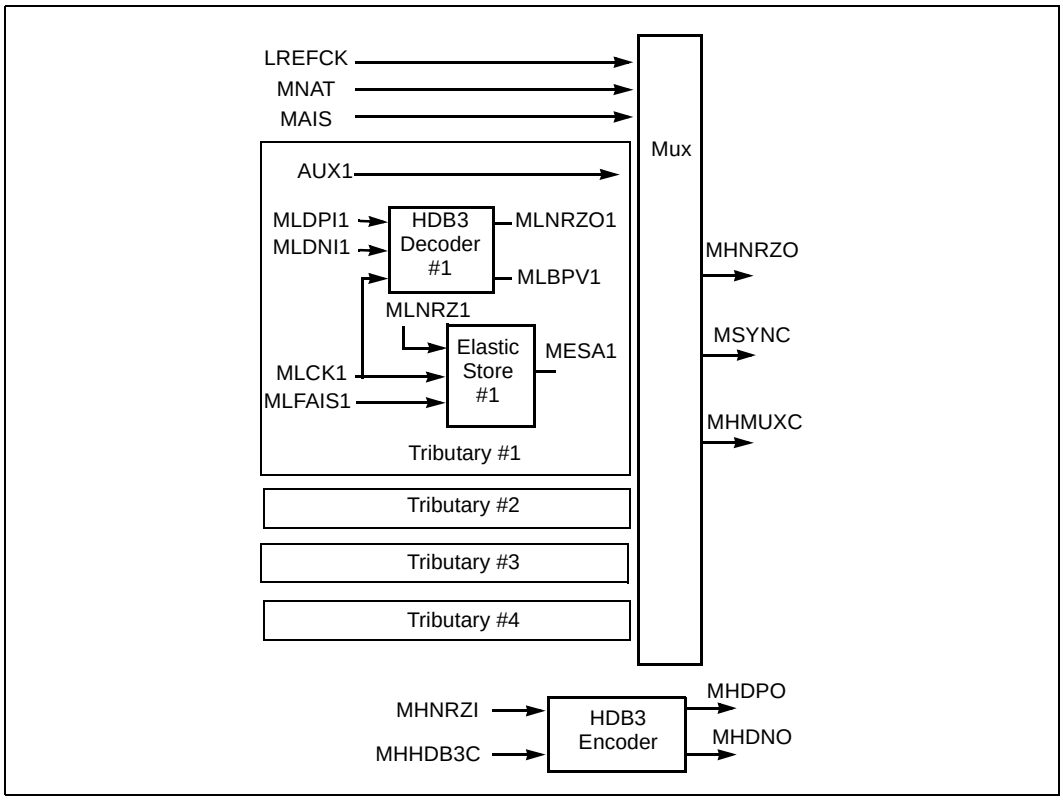
1.7.2.3 LXT6234, E3 Stage

- If the tributary LIU does not provide HDB3 encoding, then encoding is performed in the LXT6234; positive and negative data output is provided. An activity monitor provides tributary fail notification when necessary.
- If the LIU provides HDB3 encoding, the NRZ data and clock are passed to the multiplexer input.
- The multiplexer portion of the LXT6234 interleaves the four asynchronous E2 rate NRZ data streams into a single E3 data stream. Depending on the user configuration, either an onboard crystal oscillator or an external reference clock drives the data output frequency from the multiplexer at the rate of 34.368 Mbps. The bit stuffing algorithm implemented in the LXT6234 ensures tributary rate integrity at the output.

1.7.3 E Multiplexer Block Diagram

The block diagram in Figure 3 shows the I/O used on the LXT6234 to accomplish the multiplexing function. Only I/O for tributary #1 has been referenced. I/O for tributaries #2, #3, and #4 are omitted for clarity, but they are the same as tributary #1.

Figure 3. LXT6234 Multiplexing Function



1.7.4 E1/E3 Demultiplexer Block Diagram

The block diagram of the E1/E3 demultiplexer is shown in Figure 4.

1.7.4.1 E3 line Interface

- Receive clocks from the pulse data
- If the LIU does not provide HDB3 decoding, then the LIU passes HDB3 encoded signals to the LXT6234. These signals consist of the clock and (positive and negative) RZ data
- If the LIU does provide HDB3 decoding, then the LIU passes the NRZ data and clock to the LXT6234

1.7.4.2 LXT6234, E3/E2 Stage

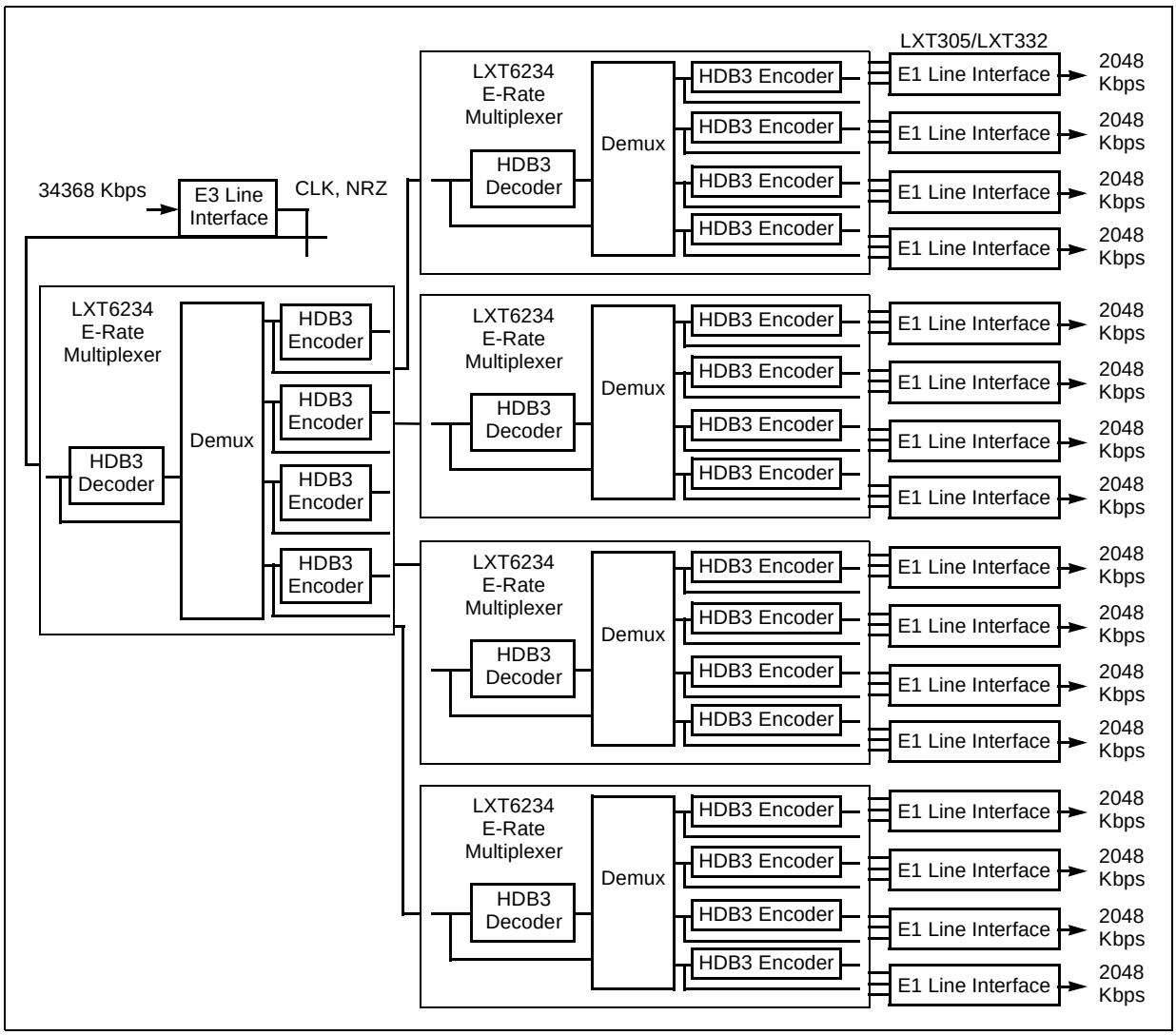
- If the LIU does not do HDB3 decoding then the signals are routed to the LXT6234 onboard HDB3 decoder. The inputs are the clock and the decoder data input signals (both positive and negative). The onboard HDB3 decoder then outputs NRZ data and clock to the elastic store of the multiplexer portion of the LXT6234.
- If the LIU provides HDB3 decoding, NRZ data and clock are received by the demultiplexer portion of the LXT6234.

- The four E2 rate data streams are recovered from the E3 NRZ data and are sent from the LXT6234 as four tributaries.

1.7.4.3 LXT6234, E2/E1 Stage

- The demultiplexer portion of the LXT6234 recovers four E1 data streams from the E2 intermediary stream.
- If the LIU does not provide HDB3 encoding, the streams are HDB3 encoded and sent out as positive and negative voltages to the E1 line interface. (LXT305 or LXT332)
- If the LIU provides HDB3 encoding the stream is sent out as NRZ data to the E1 line interface.

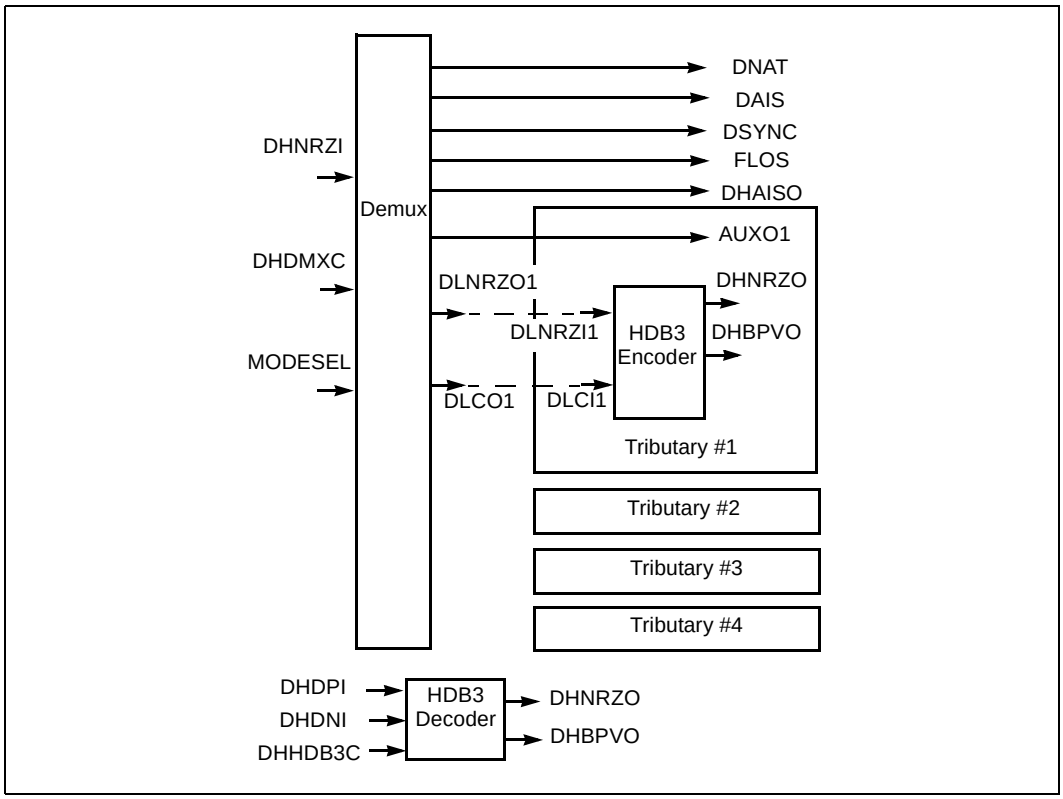
Figure 4. E1/E3 Demultiplexer



1.7.5 E Demultiplexer Block Diagram

Figure 5 shows the I/O used on the LXT6234 to perform the demultiplexing function. Only I/O for tributary #1 has been referenced. I/O for tributaries #2, #3, and #4 are omitted for clarity, but they are the same as tributary #1.

Figure 5. LXT6234 Demultiplexing Function



1.7.6 Alarms

The multiplexer and demultiplexer sides contain the following alarm provisions:

- Input Loss Alarms at all receive line interfaces
- Output Fail Alarms at all transmit line interfaces
- Frame Loss Alarm line

With ME for multiplexer and DE for demultiplexer:
i = 1 to 16 for E1
j = 1 to 4 for E2

Alarm equations are:

ME1FAISi=	MELOSi
DE1FAISi=	DE2AISDj + DE2FLOSj + DE3LOS + DE3FLOS + DE3AISD
ME2FAISj=	ME2LOSj
DE2FAISj=	DE3LOS + DE3FLOS + DE3AISD
ME3AIS=	DE3LOS + (DE3FLOS&~DE3LOS) + DEAISD

1.7.7 Auxiliary Channels

Within the E2 and E3 standards, there are four extra bits used for justification (bits 641-644 in the E2 frame, and bits 1157-1160 in the E3 frame). These bits may be used as four auxiliary channels that would provide an E2 rate of 10 KHz, or an E3 rate of 22 KHz.

Two examples how these may be used are:

- Voice Channel Maintenance
- Data Counter implemented with a parity circuit that would count data bits during one frame of the incoming stream

1.7.8 National and AIS Bits

The bits are accessible for compliance with the ITU-T recommendation. However, these two bits can also be used as auxiliary channel at the rate of 10 KHz for E2 or 22 KHz E3.

1.7.9 Microcontroller

E1/E3 multiplexer design can be improved by using a microcontroller to control the alarms and other settings. An 8 bit microcontroller, such as an Intel 87C51 is sufficient. The microcontroller could monitor alarms, provide an alarm history, update a control panel and even sound an audible alert if necessary. This microcontroller could monitor switches for loop-back instructions, test and update the National Bit, and check the configuration jumpers for E1/E2 or E2/E3 functions.

Table 9. Multiplexer Pin Description

Mux Input	
LFRECK	Reference clock for tributary data is used as reference for the AIS functions.
MNAT	National Bit Input.
MAIS	AIS bit input.
MHMUXC	High speed multiplexer clock input.
Tributary #1 Input	
AUX1	Auxiliary data input #1. The signal on this pin is clocked into the frame at the stuffing bit location (J1) when justification is such that tributary data is not placed at this location. A high on alarm signal MESA1 indicates this condition during the current frame.
MLDPI1	Positive data input. Clocked on the positive transition of the clock MCKL1.
MLDNI1	Negative data input. Clocked on the positive transition of the clock MCKL1.
MCKL1	Clock input for tributary channel 1.
MLFAIS1	Force AIS on tributary 1. Active high signal forces AIS (all 1) data and LREFCK clock.
Tributary #1 Output	
MLNRZO1	HDB3 decoder #1 NRZ output clocked on the rising edge of MCKL1.
MLNRZ1	Multiplexer tributary NRZ input clocked on the falling edge of the clock signal MLCK1.
MLBPV1	HDB3 decoder #1 bipolar violation alarm. This open collector output pulses when a bipolar violation occurs in the decoding process.

Table 9. Multiplexer Pin Description (Continued)

MESA1	Multiplexer justification status for tributary #1. A high indicates bit stuffing on the current frame. A low indicates an information bit. When externally filtered, this can be used to indicate elastic store failure or incorrect tributary frequency.
Mux Output	
MHRZO	Multiplexer NRZ output data is clocked out on the rising edge of MHMUXC.
MSYNC	Multiplexer frame synchronization pulse is one high speed clock cycle synchronous with the last bit of the frame.
HDB3 Decoder	
MHNRZI	HDB3 encoder #5 NRZ input clocked on the rising edge of MHHDB3C.
MHHDB3C	HDB3 encoder #5 clock input. When used in conjunction with the multiplexer, this pin should be tied to the multiplexer clock (MHMUXC).
MHDPO	HDB3 encoder #5 positive data output. Positive rail clocked out on the rising edge of MHHDB3C.
MHDNO	HDB3 encoder #5 negative data output. Negative rail clocked out on the rising edge of MHHDB3C.

Table 10. Demultiplexer Pin Description

Demultiplexer Input	
DHNRZI	NRZ input clocked on the rising edge of DHDMXC.
DHDMXC	Clock input.
MODESEL	Mode selection for multiplexer / demultiplexer operation. A low selects 4E1/E2 multiplexing. A high selects 4E2/E3 multiplexing.
HDB3 Decoder	
DHDPI	HDB3 decoder #5 positive rail input clocked on the rising edge of DHHDB3C.
DHDNI	HDB3 decoder #5 negative rail input clocked on the rising edge of DHHB3C.
DHHDB3C	Clock input for HDB3 decoder # 5. When used in conjunction with the demultiplexer this pin should be tied to the demultiplexer clock DHMUXC.
DHNRZO	HDB3 decoder #5 NRZ data clocked out on the rising edge of DHHDB3C.
DHBPVO	HDB3 decoder #5 bipolar violation alarm. This active high signal pulses when a bipolar violation occurs in the decoding process.
HDB3 Encoder	
DLNZO1	Tributary #1 NRZ output. This signal is clocked out on the rising edge of DHDMXC and transitions are coincident with the falling edge of DLCO1.
DLCO1	Demultiplexer side recovered clock of tributary #1. This clock has a duty cycle of 75% and is gapped at points in the frame where tributary data is not present. The maximum gap is 3 clocks at the frame word will match that of the far end multiplexer tributary input. This signal is clocked out on the rising edge of DHDMXC.
DLNRZI1	HDB3 encoder #1 NRZ input clocked on the rising edge of DLCI1.
DLCI1	Clock input for HDB3 encoder #1.
Multiplexer Output	
DNAT	National Bit output.
DAIS	AIS bit output.
DSYNC	Pulse of one high speed clock cycle synchronous with the last bit of the frame.

Table 10. Demultiplexer Pin Description (Continued)

FLOS	Loss of frame alarm. Active high frame loss alarm that occurs when the demux has not detected the frame word.
DHAIS	Input AIS detect. Active high alarm occur when an all 1's condition (AIS) is detected at the DHNRZI input. This alarm does not trip if the input is a frame signal (i.e., all tributaries are AIS on the multiplexer side).
Auxiliary #1 Output	
AUXO1	Auxiliary flag data #1 output that contains data value input on AUX1.
DLDPO1	HDB3 encoder #1 positive rail output clocked out on the rising edge of DLCI1.
DLDNO1	HDB3 encoder #1 negative output clocked out on the rising edge of DLCI1.