

SHARP

SPEC No.	C T 9 0 8 7 0 2
I S S U E:	Jul. 2 1998

To : _____

**P R E L I M I N A R Y
S P E C I F I C A T I O N S**

Product Type Timing IC for Two-power supply 270K/320K pixels color CCD

Model No. L R 3 8 6 1 3

※This specifications contains 49 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE: _____

BY: _____

PRESENTED

BY: _____

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 - Instrumentation and measuring equipment
 - Machine tools
 - Audiovisual equipment
 - Home appliances
 - Communication equipment other than for trunk lines
 - (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
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 - Mainframe computers
 - Traffic control systems
 - Gas leak detectors and automatic cutoff devices
 - Rescue and security equipment
 - Other safety devices and safety equipment, etc.
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1. General

The L R 3 8 6 1 3 is a CMOS gate array LSI. It generates timing pulses for driving a 2000k pixels CCD area sensor, and processing pulses.

1-1. Features

- * The package material is plastic.
- * A p-type silicon circuit board is used.
- * The package type is 48-pin FQFP
- * The process (structure) is CMOS.
- * The delay time per 1 gate is 0.4ns.
- * Not designed or rated as radiation hardened.

1-2. Functions

- * Designed for CCD area sensor LZ21N3V and LZ21N3 with 2,000,000 pixels on 1/2 Format size.
- * 3.3V and +4.5V power supply.
- * A freqency of driving horizontal CCD is 17.987MHz.
- * Both double speed drive monitoring mode and still mode are possible.
- * External function control with serial data input is possible.

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2. Pin Assignment

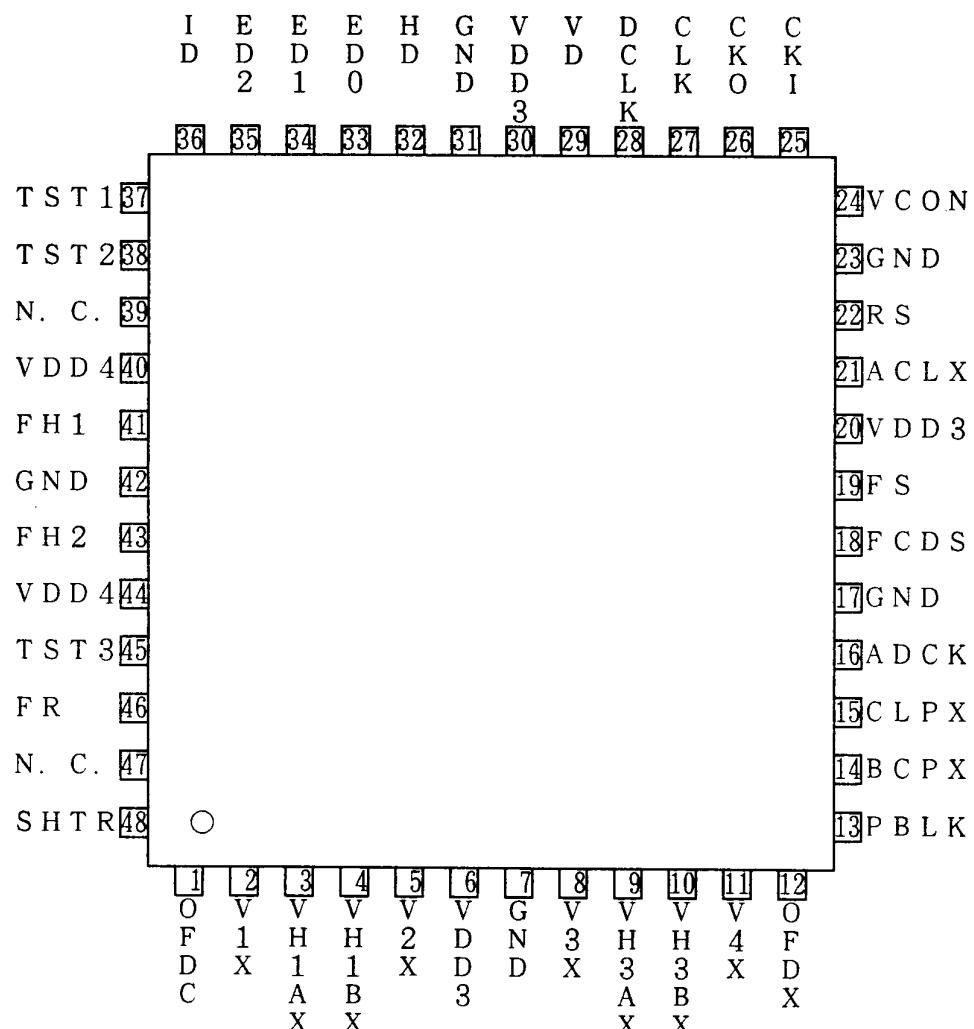
2-1. Pin Assignment

PIN NO.	I / O	SIGNAL	PIN NO.	I / O	SIGNAL
1	O 3	O F D C	2 5	O S C I 3	C K I
2	O 3	V 1 X	2 6	O C S O 3	C K O
3	O 3	V H 1 A X	2 7	O 6 M A 3	C L K
4	O 3	V H 1 B X	2 8	O 6 M A 3	D C L K
5	O 3	V 2 X	2 9	I C 3	V D
6	-	V D D 3	3 0	-	V D D 3
7	-	G N D	3 1	-	G N D
8	O 3	V 3 X	3 2	I C 3	H D
9	O 3	V H 3 A X	3 3	I C S U 3	E D 0
1 0	O 3	V H 3 B X	3 4	I C S U 3	E D 1
1 1	O 3	V 4 X	3 5	I C S U 3	E D 2
1 2	O 3	O F D X	3 6	O 3	I D
1 3	O 3	P B L K	3 7	I C D 4	T S T 1
1 4	O 3	B C P X	3 8	I C D 4	T S T 2
1 5	O 3	C L P X	3 9	-	N. C.
1 6	O 3	A D C K	4 0	-	V D D 4
1 7	-	G N D	4 1	O 6 M A 4 3	F H 1
1 8	O 6 M A 3	F C D S	4 2	-	G N D
1 9	O 6 M A 3	F S	4 3	O 6 M A 4 3	F H 2
2 0	-	V D D 3	4 4	-	V D D 4
2 1	I C U 3	A C L X	4 5	I C D 4	T S T 3
2 2	O 6 M A 3	R S	4 6	O 6 M A 4 3	F R
2 3	-	G N D	4 7	-	N. C.
2 4	O 3	S H T R	4 8	I C D 3	S H T R

- I C 3 : Input (CMOS level)
 I C U 3 : Input (CMOS level with pull-up resister)
 I C S U 3 : Input (CMOS level with schmitt-trigger)
 I C D 3 : Input (CMOS level with pull-down resister)
 I C U 4 : Input (CMOS level with pull-up resister)
 I C D 4 : Input (CMOS level with pull-down resister)
 O 3 : Output (Output High level is VDD3)
 O 6 M A 3 : Output (Output High level is VDD3)
 O 6 M A 4 3 : Output (Output High level is VDD4)
 O S C I 3 : Input pin for oscillation
 O S C O 3 : Output pin for oscillation
 V D D 3 : +3.3V Power Supply
 V D D 4 : +4.5V Power Supply

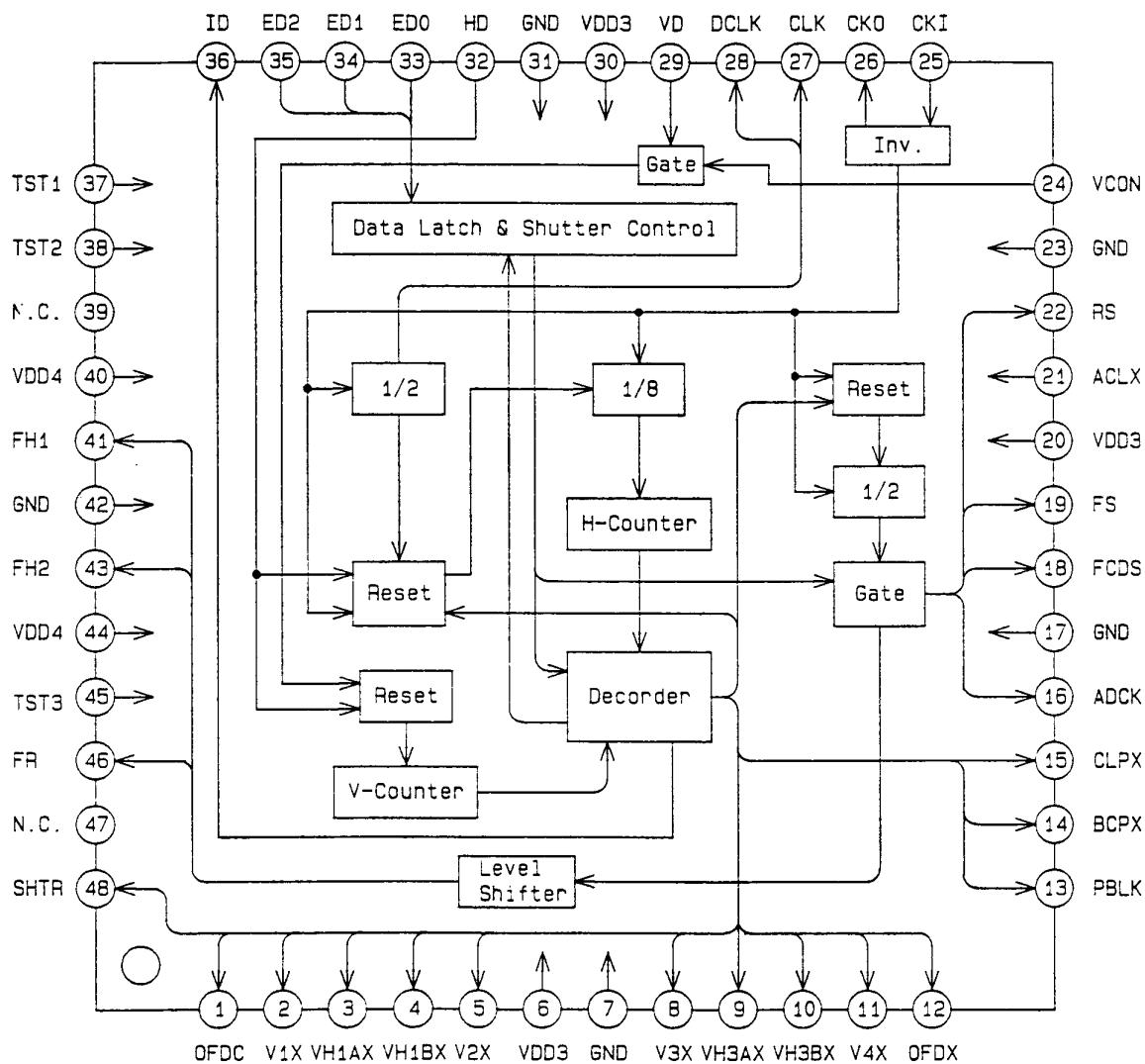
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2-2. Pin Configuration (Top View)



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3. Block Diagram



L R 3 8 6 1 3

4. Pin Description

4-1. Pin description

No.	Symbol	I/O	Pol.	Pin Name	Description
1	OFDC	03	↑	Control pulse for OFD Voltage	A pulse to control OFD Voltage.
2	V1X	03	↑	Ver. transfer pulse 1	A vertical transfer pulse for CCD. Connect to V Driver IC.
3	VH1AX	03	↑	Read out pulse 1A	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to V Driver IC.
4	VH1BX	03	↑	Read out pulse 1B	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to V Driver IC.
5	V2X	03	↑	Ver. transfer pulse 2	A vertical transfer pulse for CCD. Connect to V Driver IC.
6	VDD3	-	-	Power supply	Supply +3.3 V power.
7	GND	-	-	Ground	A grounding pin.
8	V3X	03	↑	Ver. transfer pulse 3	A vertical transfer pulse for CCD. Connect to V Driver IC.
9	VH3AX	03	↑	Read out pulse 3A	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to V Driver IC.
10	VH3BX	03	↑	Read out pulse 3B	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to V Driver IC.
11	V4X	03	↑	Ver. transfer pulse 4	A vertical transfer pulse for CCD. Connect to V Driver IC.
12	OFDX	03	↑	OFD pulse output	A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFD of CCD through the V Driver IC and DC offset circuit. Held at H level at normal mode.
13	PBLK	03	↑	Pre-blanking pulse	A pulse for pre-blanking. This pulse stays low during the absence of effective pixels within the ver. blanking or the period of sweepout signal. (see 4-6)
14	BCPX	03	↑	Optical black clamp pulse	A pulse to clamp the optical black signal. This pulse stays high during the absence of effective pixels within the ver. blanking or the period of sweepout signal. (see 4-6)
15	CLPX	03	↑	Clamp pulse	A pulse to clamp the dummy signal. This pulse stays high during the sweep-out period

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No.	Symbol	I/O	Pol.	Pin Name	Description
16	ADCK	06MA3	U	AD Clock	An AD converter clock. The phase is selectable by serial data control. (See 4-12)
17	GND	-	-	Ground	A grounding pin.
18	FCDS	06MA3	U	CDS pulse 1	A pulse to clamp the feed-through level of the signal from CCD. The phase is selectable by serial data control. (See 4-9)
19	FS	06MA3	U	CDS pulse 2	A pulse to sample-hold the signal from CCD. The phase is selectable by serial data control. (See 4-10)
20	VDD3	-	-	Power supply	Supply +3.3 V power.
21	ACLX	ICU3	-	All clear input	An input pin for resetting all internal circuit at power on. Connect VDD through the diode and GND through the capacitor.
22	RS	06MA3	U	S/H pulse	A pulse to sample-hold the signal. The phase is selectable by serial data control. (See 4-11)
23	GND	-	-	Ground	A grounding pin.
24	VCON	ICU3	-	VD control	An input pin to control internal vertical clock for long shutter speed. H level or open ; VD L level ; VD is masked by the pulse which is latched by the rising edge of VD. It's necessary to be set SMD=High and number of the fields data $n \geq 2$ in serial data control at VCON operation.
25	CKI	OSCI3	-	Clock input	An input pin for reference clock oscillation. The frequency is 35.874MHz.
26	CKO	OSC03	-	Clock output	An output pin for reference clock oscillation. The output is the inverse CKI(pin 25).
27	CLK	06MA3	U	Clock output	An output pin to generate HD and VD pulse. The frequency is 17.937MHz.
28	DCLK	06MA3	U	Clock output	An output pin for DSP circuit. The frequency is 17.937MHz. The phase is selectable by serial data control. (See 4-7)

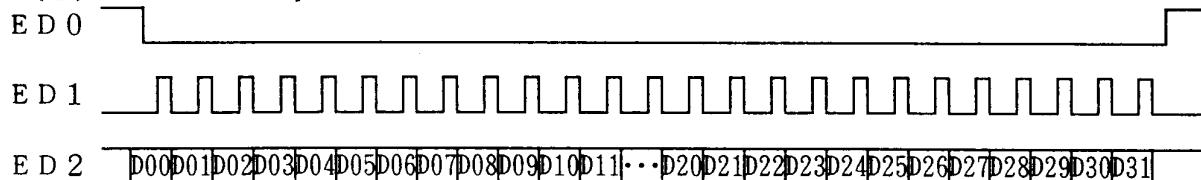
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No.	Symbol	I/O	Pol.	Pin Name	Description
29	VD	IC3	U	Ver. drive pulse input	An input pin for reference of vertical pulse. The length of low level is 9H. The period is following Still mode : 656H Monitor. mode : 262.5H
30	VDD	-	-	Power supply	Supply +3.3 V power.
31	GND	-	-	Ground	A grounding pin.
32	HD	IC3	U	Hor. drive pulse input	An input pin for reference of Horizontal pulse. As HD is latched by the rising edge of CLK, HD should be generated by the rising edge of CLK. The period is 2280 clocks.
33	ED0	ICU3	-	Strobe pulse input	An input pin for the strobe pulse to control the functions.
34	ED1	ICU3	-	Shift register clock input	An input pin for the clock of the shift register to control the functions.
35	ED2	ICU3	-	Shift register data input	An input pin for the data of the shift register to control the functions.
36	ID	03	U	Line index pulse	The pulse is used in color separator. The signal switches between high and low at every lines.
37	TST1	ICD4	-	Test terminal 1	A test pin. Set open or to low level in the normal mode.
38	TST2	ICD4	-	Test terminal 2	A test pin. Set open or to low level in the normal mode.
39	NC	-	-	Non connection	Non connection
40	VDD4	-	-	Power supply	Supply +4.5 V power.
41	FH1	06MA43	U	Hor. transfer pulse 1	A horizontal transfer pulse for CCD. Connect to φH1 of CCD.
42	GND	-	-	Ground	A grounding pin.
43	FH2	06MA43	U	Hor. transfer pulse 2	A horizontal transfer pulse for CCD. Connect to φH2 of CCD.
44	VDD4	-	-	Power supply	Supply +4.5 V power.
45	TST3	ICD4	-	Test terminal 3	A test pin. Set open or to low level in the normal mode.
46	FR	06MA43	U	Reset pulse	A reset pulse for CCD. The phase is selectable by serial data control. (See 4-8)
47	NC	-	-	Non connection	Non connection
48	SHTR	03	U	Trigger output	A trigger pulse for effective signal period.

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4-2. Serial data control

(1) Serial data input



The data is shifted by the rising edge of ED1, and latched by the rising edge of ED0. PWSA is effective at the rising edge of ED0, but others are effective at the Hori. lines in which VH1AX~VH3BX are active.

ED0 should be Low level during data inputs of ED1, ED2.

As all inner data are set to Low level by ACLX or PWSA, ED0~ED1 should be input for desirable operations.

As all inner data except PWSA are set to Low level by PWSA, ED0~ED1 should be input for desirable operations.

(2) Item of Serial data input

Data	Name	Function	Data=L	Data=H	at ACLX=L
D00	S D 0	Step of high speed shutter	See the table of Shutter speed control		
	S				All L
D06	S D 6				
D07	S D 7	Number of exposed fields	See the table of Shutter speed control		
D08	S D 8				All L
D09	S D 9				
D10	S M D	Electronic shutter mode control	See the table of Shutter mode		L
D11	I N M D	Integration mode cont.	Monitoring	Still	L
D12	P W S A	Power save control	Normal	Power save	L
D13	P L C H	Polarity cont. of FCDS, FS, RS pulses	Negative	Positive	L
D14	D U M M Y	Dummy	—	—	—
D15	B C P C N T	BCP control	Uncontinuously	Continuously	L
D16	M L 1	Phase cont. of DCLK	See the table of DCLK		L
D17	M L 2				L
D18	M L 1				L
D19	M R 2	Phase cont. of FR	See the table of FR		L
D20	M R 3				L
D21	M C 1				L
D22	M C 2	Phase cont. of FCDS	See the table of FCDS		L
D23	M C 3				L
D24	M S 1				L
D25	M S 2	Phase cont. of FS	See the table of FS		L
D26	M S 3				L
D27	M F 1				L
D28	M F 2	Phase cont. of RS	See the table of RS		L
D29	M F 3				L
D30	M A 1	Phase cont. of ADCK	See the table of ADCK		L
D31	M A 2				L

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(3) S D 0 ~ S D 9, SMD

(3-1) Shutter mode

D10;SMD		Shutter mode	Function
L	OFF	Electronic shutter off	
H	ON	It can be possible to use shutter speed select combine with High-speed shutter and Low-speed shutter in monitoring mode. It can be possible to use Low speed shutter speed in still mode.	

(3-2) The table of shutter speed

•High speed shutter

 $1 \leq n \leq 118$

•Low speed shutter

 $0 \leq n \leq 7$

D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	No.	Shutter speed (sec)	Notes
SD0	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	SD9	SMD			
X	X	X	X	X	X	X	X	X	X	L	-	1/ 30;Moni. 1/ 15;Still	shutter off
L	H	H	L	H	H	H	L	L	L	H	118	1/26,471	High speed shutter
H	L	H	L	H	H	H	L	L	L	H	117	1/23,560	
L	L	H	L	H	H	H	L	L	L	H	116	1/21,951	
H	H	L	L	H	H	H	L	L	L	H	115	1/20,362	
L	H	L	L	H	H	H	L	L	L	H	114	1/18,828	
H	L	L	L	H	H	H	L	L	L	H	113	1/17,375	
L	L	L	L	H	H	H	L	L	L	H	112	1/16,245	
H	H	H	H	L	H	H	L	L	L	H	111	1/15,152	
L	H	H	H	L	H	H	L	L	L	H	110	1/14,107	
H	L	H	H	L	H	H	L	L	L	H	109	1/13,120	
L	L	H	H	L	H	H	L	L	L	H	108	1/12,262	
H	H	L	H	L	H	H	L	L	L	H	107	1/11,392	
L	H	L	H	L	H	H	L	L	L	H	106	1/10,638	
H	L	L	H	L	H	H	L	L	L	H	105	1/ 9,934	
L	L	L	H	L	H	H	L	L	L	H	104	1/ 9,278	
H	H	H	L	L	H	H	L	L	L	H	103	1/ 8,637	
L	H	H	L	L	H	H	L	L	L	H	102	1/ 8,021	
H	L	H	L	L	H	H	L	L	L	H	101	1/ 7,488	
L	L	H	L	L	H	H	L	L	L	H	100	1/ 6,977	
H	H	L	L	L	H	H	L	L	L	H	99	1/ 6,531	
L	H	L	L	L	H	H	L	L	L	H	98	1/ 6,081	
H	L	L	L	L	H	H	L	L	L	H	97	1/ 5,562	
L	L	L	L	L	H	H	L	L	L	H	96	1/ 5,190	
H	H	H	H	H	L	H	L	L	L	H	95	1/ 4,803	
L	H	H	H	H	L	H	L	L	L	H	94	1/ 4,532	
H	L	H	H	H	L	H	L	L	L	H	93	1/ 4,265	
L	L	H	H	H	L	H	L	L	L	H	92	1/ 3,501	
H	H	L	H	H	L	H	L	L	L	H	91	1/ 3,704	
L	H	L	H	H	L	H	L	L	L	H	90	1/ 3,574	
H	L	L	H	H	L	H	L	L	L	H	89	1/ 3,435	

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D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	No.	Shutter speed (sec)	Notes
SD0	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	SD9	SMD			
L	L	L	H	H	L	H	L	L	L	H	88	1/ 3.217	
H	H	H	L	H	L	H	L	L	L	H	87	1/ 3.034	
L	H	H	L	H	L	H	L	L	L	H	86	1/ 2.879	
H	L	H	L	H	L	H	L	L	L	H	85	1/ 2.709	
L	L	H	L	H	L	H	L	L	L	H	84	1/ 2.521	
H	H	L	L	H	L	H	L	L	L	H	83	1/ 2.394	
L	H	L	L	H	L	H	L	L	L	H	82	1/ 2.242	
H	L	L	L	H	L	H	L	L	L	H	81	1/ 2.080	
L	L	L	L	H	L	H	L	L	L	H	80	1/ 1.947	
H	H	H	H	L	L	H	L	L	L	H	79	1/ 1.837	
L	H	H	H	L	L	H	L	L	L	H	78	1/ 1.716	
H	L	H	H	L	L	H	L	L	L	H	77	1/ 1.607	
L	L	H	H	L	L	H	L	L	L	H	76	1/ 1.490	
H	H	L	H	L	L	H	L	L	L	H	75	1/ 1.409	
L	H	L	H	L	L	H	L	L	L	H	74	1/ 1.335	
H	L	L	H	L	L	H	L	L	L	H	73	1/ 1.253	
L	L	L	H	L	L	H	L	L	L	H	72	1/ 1.171	
H	H	H	L	L	L	H	L	L	L	H	71	1/ 1.082	
L	H	H	L	L	L	H	L	L	L	H	70	1/ 1.020	
H	L	H	L	L	L	H	L	L	L	H	69	1/ 951	
L	L	H	L	L	L	H	L	L	L	H	68	1/ 903	
H	H	L	L	L	L	H	L	L	L	H	67	1/ 849	
L	H	L	L	L	L	H	L	L	L	H	66	1/ 810	
H	L	L	L	L	L	H	L	L	L	H	65	1/ 767	
L	L	L	L	L	L	H	L	L	L	H	64	1/ 735	
H	H	H	H	H	H	L	L	L	L	H	63	1/ 699	
L	H	H	H	H	H	L	L	L	L	H	62	1/ 672	
H	L	H	H	H	H	L	L	L	L	H	61	1/ 642	
L	L	H	H	H	H	L	L	L	L	H	60	1/ 594	
H	H	L	H	H	H	L	L	L	L	H	59	1/ 526	
L	H	L	H	H	H	L	L	L	L	H	58	1/ 516	
H	L	L	H	H	H	L	L	L	L	H	57	1/ 484	
L	L	L	H	H	H	L	L	L	L	H	56	1/ 456	
H	H	H	L	H	H	L	L	L	L	H	55	1/ 431	
L	H	H	L	H	H	L	L	L	L	H	54	1/ 409	
H	L	H	L	H	H	L	L	L	L	H	53	1/ 389	
L	L	H	L	H	H	L	L	L	L	H	52	1/ 371	
H	H	L	L	H	H	L	L	L	L	H	51	1/ 354	
L	H	L	L	H	H	L	L	L	L	H	60	1/ 339	
H	L	L	L	H	H	L	L	L	L	H	49	1/ 325	
L	L	L	L	H	H	L	L	L	L	H	48	1/ 312	
H	H	H	H	L	H	L	L	L	L	H	47	1/ 300	
L	H	H	H	L	H	L	L	L	L	H	46	1/ 279	
H	L	H	H	L	H	L	L	L	L	H	45	1/ 261	
L	L	H	H	L	H	L	L	L	L	H	44	1/ 244	

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D00 SD0	D01 SD1	D02 SD2	D03 SD3	D04 SD4	D05 SD5	D06 SD6	D07 SD7	D08 SD8	D09 SD9	D10 SMD	No.	Shutter speed (sec)	Notes
H	H	L	H	L	H	L	L	L	L	H	43	1/ 230	
L	H	L	H	L	H	L	L	L	L	H	42	1/ 217	
H	L	L	H	L	H	L	L	L	L	H	41	1/ 206	
L	L	L	H	L	H	L	L	L	L	H	40	1/ 196	
H	H	H	L	L	H	L	L	L	L	H	39	1/ 187	
L	H	H	L	L	H	L	L	L	L	H	38	1/ 178	
H	L	H	L	L	H	L	L	L	L	H	37	1/ 171	
L	L	H	L	L	H	L	L	L	L	H	36	1/ 163	
H	H	L	L	L	H	L	L	L	L	H	35	1/ 157	
L	H	L	L	L	H	L	L	L	L	H	34	1/ 151	
H	L	L	L	L	H	L	L	L	L	H	33	1/ 145	
L	L	L	L	L	H	L	L	L	L	H	32	1/ 135	
H	H	H	H	H	L	L	L	L	L	H	31	1/ 127	
L	H	H	H	H	L	L	L	L	L	H	30	1/ 119	
H	L	H	H	H	L	L	L	L	L	H	29	1/ 112	
L	L	H	H	H	L	L	L	L	L	H	28	1/ 106	
H	H	L	H	H	L	L	L	L	L	H	27	1/ 101	
L	H	L	H	H	L	L	L	L	L	H	26	1/ 96	
H	L	L	H	H	L	L	L	L	L	H	25	1/ 91	
L	L	L	H	H	L	L	L	L	L	H	24	1/ 87	
H	H	H	L	H	L	L	L	L	L	H	23	1/ 84	
L	H	H	L	H	L	L	L	L	L	H	22	1/ 80	
H	L	H	L	H	L	L	L	L	L	H	21	1/ 77	
L	L	H	L	H	L	L	L	L	L	H	20	1/ 74	
H	H	L	L	H	L	L	L	L	L	H	19	1/ 69	
L	H	L	L	H	L	L	L	L	L	H	18	1/ 65	
H	L	L	L	H	L	L	L	L	L	H	17	1/ 61	
L	L	L	L	H	L	L	L	L	L	H	16	1/ 57	
H	H	H	H	L	L	L	L	L	L	H	15	1/ 54	
L	H	H	H	L	L	L	L	L	L	H	14	1/ 51	
H	L	H	H	H	L	L	L	L	L	H	13	1/ 49	
L	L	H	H	L	L	L	L	L	L	H	12	1/ 46	
H	H	L	H	L	L	L	L	L	L	H	11	1/ 44	
L	H	L	H	L	L	L	L	L	L	H	10	1/ 42	
H	L	L	H	L	L	L	L	L	L	H	9	1/ 41	
L	L	L	H	L	L	L	L	L	L	H	8	1/ 39	
H	H	H	L	L	L	L	L	L	L	H	7	1/ 38	
L	H	H	L	L	L	L	L	L	L	H	6	1/ 36	
H	L	H	L	L	L	L	L	L	L	H	5	1/ 35	
L	L	H	L	L	L	L	L	L	L	H	4	1/ 34	
H	H	L	L	L	L	L	L	L	L	H	3	1/ 33	
L	H	L	L	L	L	L	L	L	L	H	2	1/ 32	
H	L	L	L	L	L	L	L	L	L	H	1	1/ 31	

High speed
shutter

L R 3 8 6 1 3

D00	D01	D02	D03	D04	D05	D06	D07	D08	D09	D10	No.	Shutter speed (sec)	Notes
SD0	SD1	SD2	SD3	SD4	SD5	SD6	SD7	SD8	SD9	SMD			
X	X	X	X	X	X	X	L	L	L	H	-	1 field	Low speed shutter
X	X	X	X	X	X	X	H	L	L	H	-	2 fields	
X	X	X	X	X	X	X	L	H	L	H	-	3 fields	
X	X	X	X	X	X	X	H	H	L	H	-	4 fields	
X	X	X	X	X	X	X	L	L	H	H	-	5 fields	
X	X	X	X	X	X	X	H	L	H	H	-	6 fields	
X	X	X	X	X	X	X	L	H	H	H	-	7 fields	
X	X	X	X	X	X	X	H	H	H	H	-	8 fields	

(4) I N M D [D11]

H level input ; CCD outputs the data for Still picture.

L level input ; CCD outputs the data for Monitoring picture.

(5) P W S A [D12]

H level input ; The power save function is operated.

CK0, CLK ; Operate

Other outputs ; L level outputs

L level input ; All outputs are operate.

(6) B C P C N T [D15]

Control BCPX(pin14)

L level ; Held to H level at ver. blanking period and sweep-out.

H level ; Held to H level at sweep-out period.

(7) M L 1, M L 2 [D16, D17]

ML 1 [D16]	L	H	L	H
ML 2 [D17]	L	L	H	H
Phase	0°	90°	180°	270°

(8) M R 1, M R 2, M R 3 [D18, D19, D20]

MR 1 [D18]	L	H	L	H	L	H	L	H
MR 2 [D19]	L	L	H	H	L	L	H	H
MR 3 [D20]	L	L	L	L	H	H	H	H
Phase	A	A+a	A+2a	A+3a	A+4a	A+5a	A+6a	A+7a

(9) M C 1, M C 2, M C 3 [D21, D22, D23]

MC 1 [D21]	L	H	L	H	L	H	L	H
MC 2 [D22]	L	L	H	H	L	L	H	H
MC 3 [D23]	L	L	L	L	H	H	H	H
Phase	A	A+a	A+2a	A+3a	A+4a	A+5a	A+6a	A+7a

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(10) MS 1, MS 2, MS 3 項目 [D24, D25, D26]

MS 1 [D24]	L	H	L	H	L	H	L	H
MS 2 [D25]	L	L	H	H	L	L	H	H
MS 3 [D26]	L	L	L	L	H	H	H	H
Phase	A	A+a	A+2a	A+3a	A+4a	A+5a	A+6a	A+7a

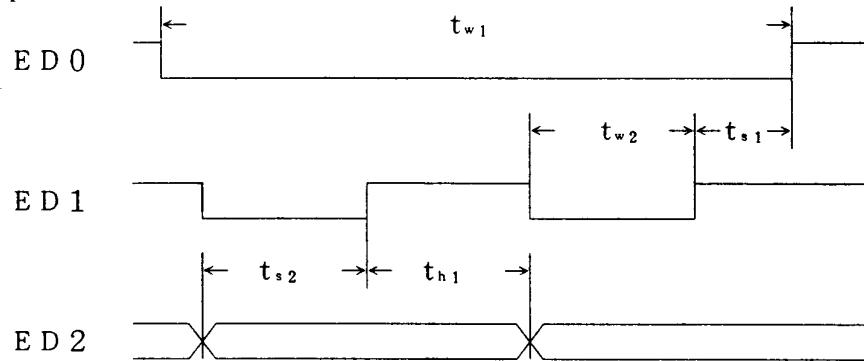
(11) MF 1, MF 2, MF 3 [D27, D28, D29]

MF 1 [D27]	L	H	L	H	L	H	L	H
MF 2 [D28]	L	L	H	H	L	L	H	H
MF 3 [D29]	L	L	L	L	H	H	H	H
Phase	A	A+a	A+2a	A+3a	A+4a	A+5a	A+6a	A+7a

(12) MA 1, MA 2 [D30, D31]

MA 1 [D30]	L	H	L	H
MA 2 [D31]	L	L	H	H
Phase	0°	90°	180°	270°

(13) Input characteristics of serial data



Symbol	Definition	Min.	Max.
t_{w1}	Pulse width of ED0	*	-
t_{w2}	Pulse width of ED1	20ns	-
t_{s1}	The rising set-up of ED0 regard with the rising edge of ED1	20ns	-
t_{s2}	The rising set-up of ED2 regard with the rising edge of ED1	20ns	-
t_{h1}	The hold-time of ED2 regard with the rising edge of ED1	20ns	-

* t_{w1} : The period of the effective data inputs at ED1, ED2

L R 3 8 6 1 3

5. Electrical Characteristics

5-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD3}, V_{DD4}	-0.3 ~ 6.07	V
Input voltage	$V_{in} (n=3, 4)$	-0.3 ~ $V_{DDn} + 0.3$	V
Output voltage	$V_{on} (n=3, 4)$	-0.3 ~ $V_{DDn} + 0.3$	V
Operation temperature	T_{opr}	-20 ~ +70	°C
Storage temperature	T_{stg}	-55 ~ +150	°C

5-2. DC Characteristics ($V_{DD3, 3A}=3.0V \sim V_{DD4}, V_{DD4}=4.2V \sim 5.5V, T_{opr}=-20 \sim +70°C$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH3}		$0.8 \times V_{DD3}$			V	1, 2,
Input "Low" voltage	V_{IL3}				$0.2 \times V_{DD3}$	V	4
Input "High" voltage	V_{IH4}	Schmitt-buffer			$0.75 \times V_{DD3}$	V	3
Input "Low" voltage	V_{IL4}		$0.2 \times V_{DD3}$			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		$0.08 \times V_{DD3}$			V	
Input "High" voltage	V_{IH4}		$0.8 \times V_{DD4}$			V	5, 6
Input "Low" voltage	V_{IL4}				$0.2 \times V_{DD4}$	V	
Input "High" current	I_{IH3-1}	$V_I = V_{DD3} V$			1.0	μA	1
Input "Low" current	I_{IL3-1}	$V_I = 0 V$			1.0	μA	
Input "High" current	I_{IH3-2}	$V_I = V_{DD3} V$			2.0	μA	2, 3
Input "Low" current	I_{IL3-2}	$V_I = 0 V$	2.0		30	μA	
Input "High" current	I_{IH3-3}	$V_I = V_{DD3} V$	2.0		30	μA	4
Input "Low" current	I_{IL3-3}	$V_I = 0 V$			2.0	μA	
Input "High" current	I_{IH4-1}	$V_I = V_{DD4} V$	4.0		60	μA	5
Input "Low" current	I_{IL4-1}	$V_I = 0 V$			2.0	μA	
Input "High" current	I_{IH4-2}	$V_I = V_{DD4} V$	4.0		60	μA	6
Input "Low" current	I_{IL4-2}	$V_I = 0 V$			2.0	μA	
Output "High" voltage	V_{OH3-1}	$I_{OH} = -1mA$	$V_{DD3}-0.5$			V	7
Output "Low" voltage	V_{OL3-1}	$I_{OL} = 2mA$			0.4	V	
Output "High" voltage	V_{OH3-2}	$I_{OH} = -3mA$	$V_{DD3}-0.5$			V	8
Output "Low" voltage	V_{OL3-2}	$I_{OL} = 3mA$			0.4	V	
Output "High" voltage	V_{OH4}	$I_{OH} = -10mA$	$V_{DD4}-0.5$			V	9
Output "Low" voltage	V_{OL4}	$I_{OL} = 10mA$			0.4	V	

Note 1 : Applied to Inputs(IC3, OSCI33).

Note 2 : Applied to Inputs(ICU3).

Note 3 : Applied to Input(ICSU3).

Note 4 : Applied to Inputs(ICD3).

Note 5 : Applied to Inputs(ICU3).

Note 6 : Applied to Inputs(ICD4).

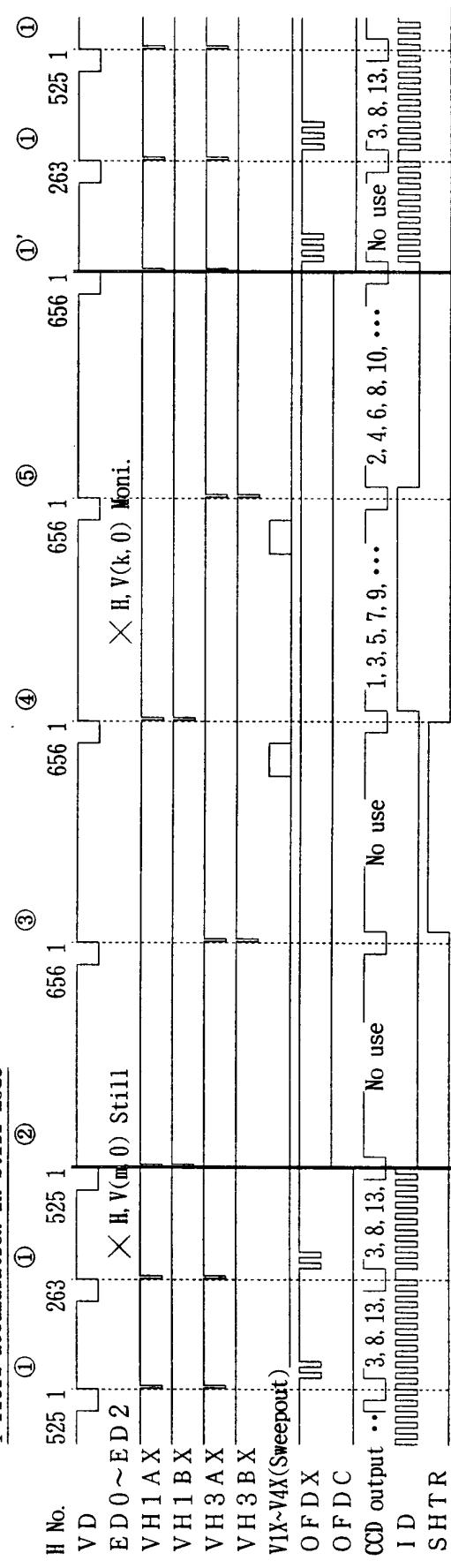
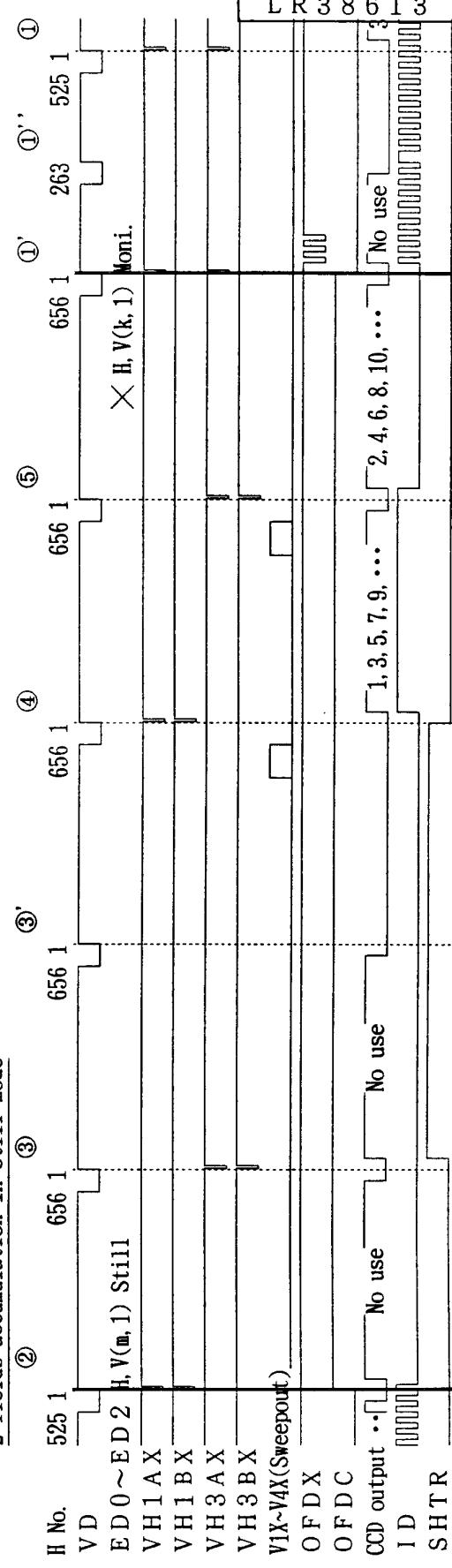
Note 7 : Applied to (O3).

Note 8 : Applied to (OSC03).

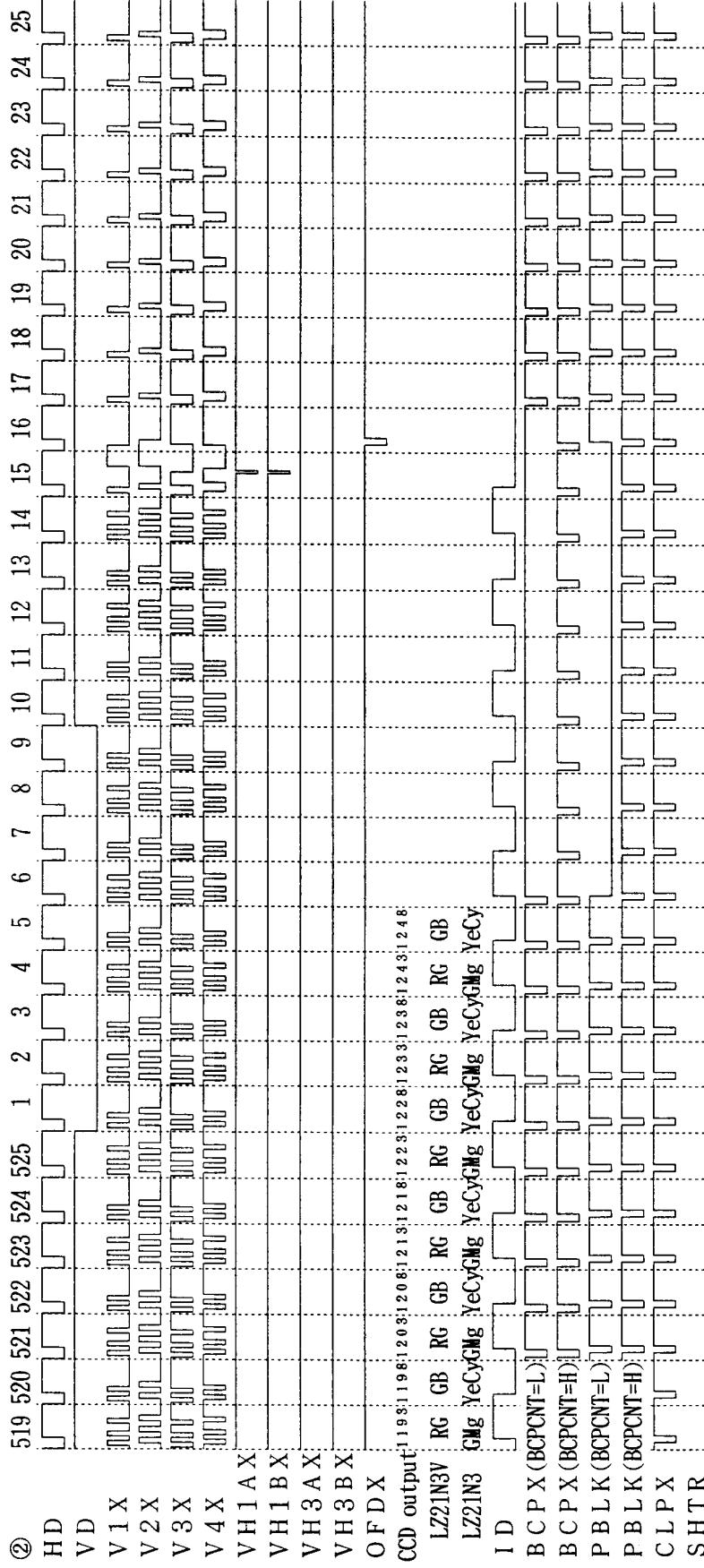
(Output(OSC03) measures on conditions that input(OSCI3) level is 0V or V_{DD3} .)

Note 9 : Applied to Output(06MA43).

6-1. Pulse timing for camera system

1 field accumulation in still mode2 fields accumulation in still mode

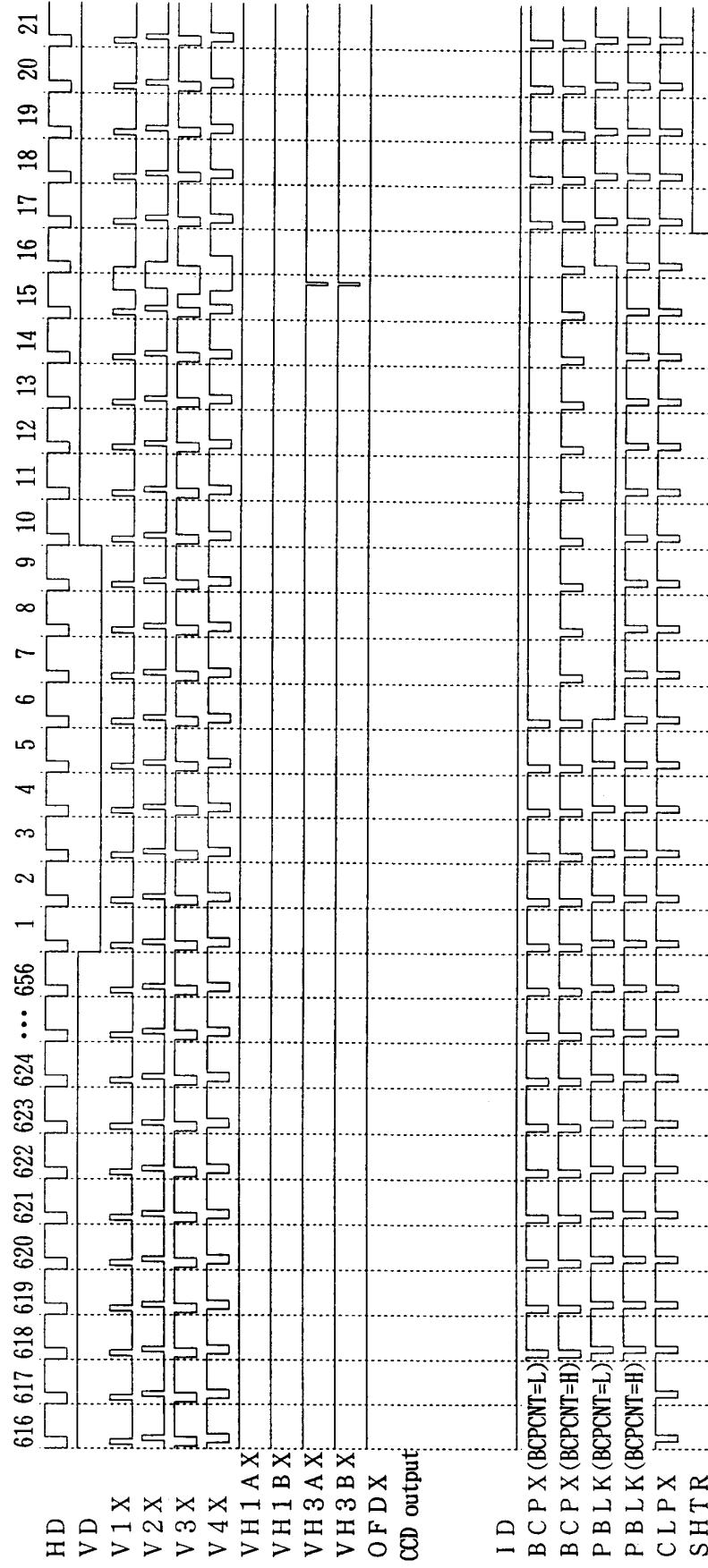
Vertical pulse timing-2
Switching from monitoring to still mode (②)



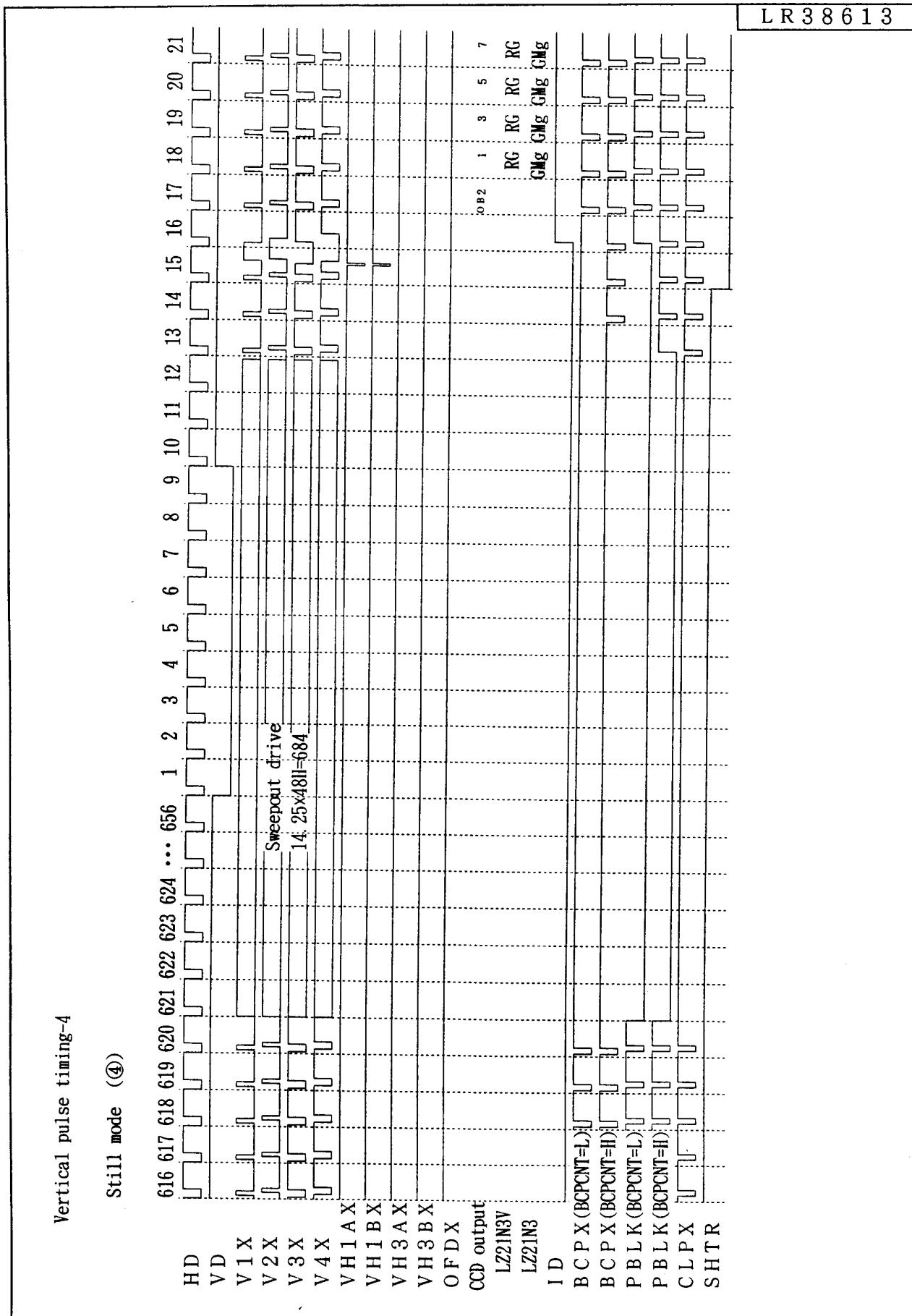
LR 38613

Vertical pulse timing-3

Still mode (③)

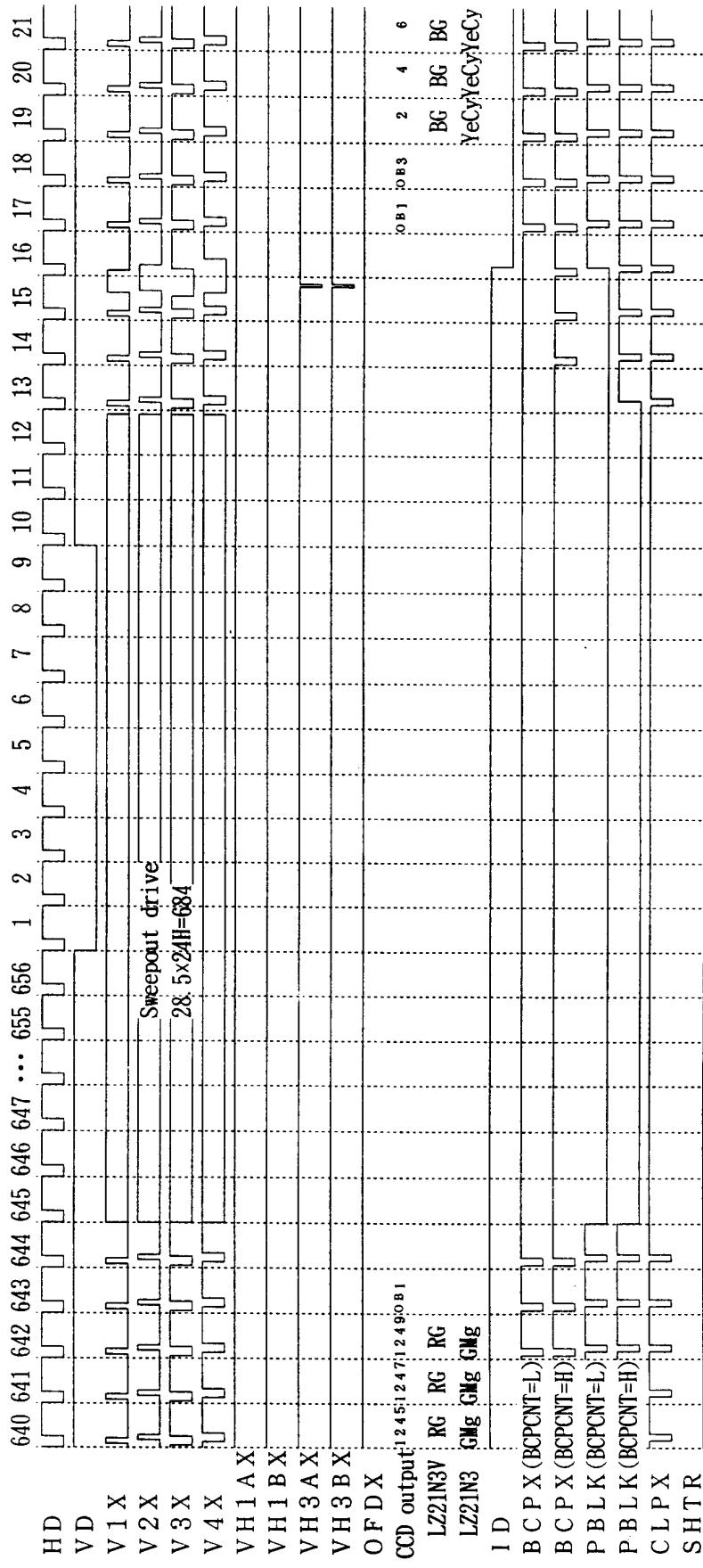


L R 3 8 6 1 3



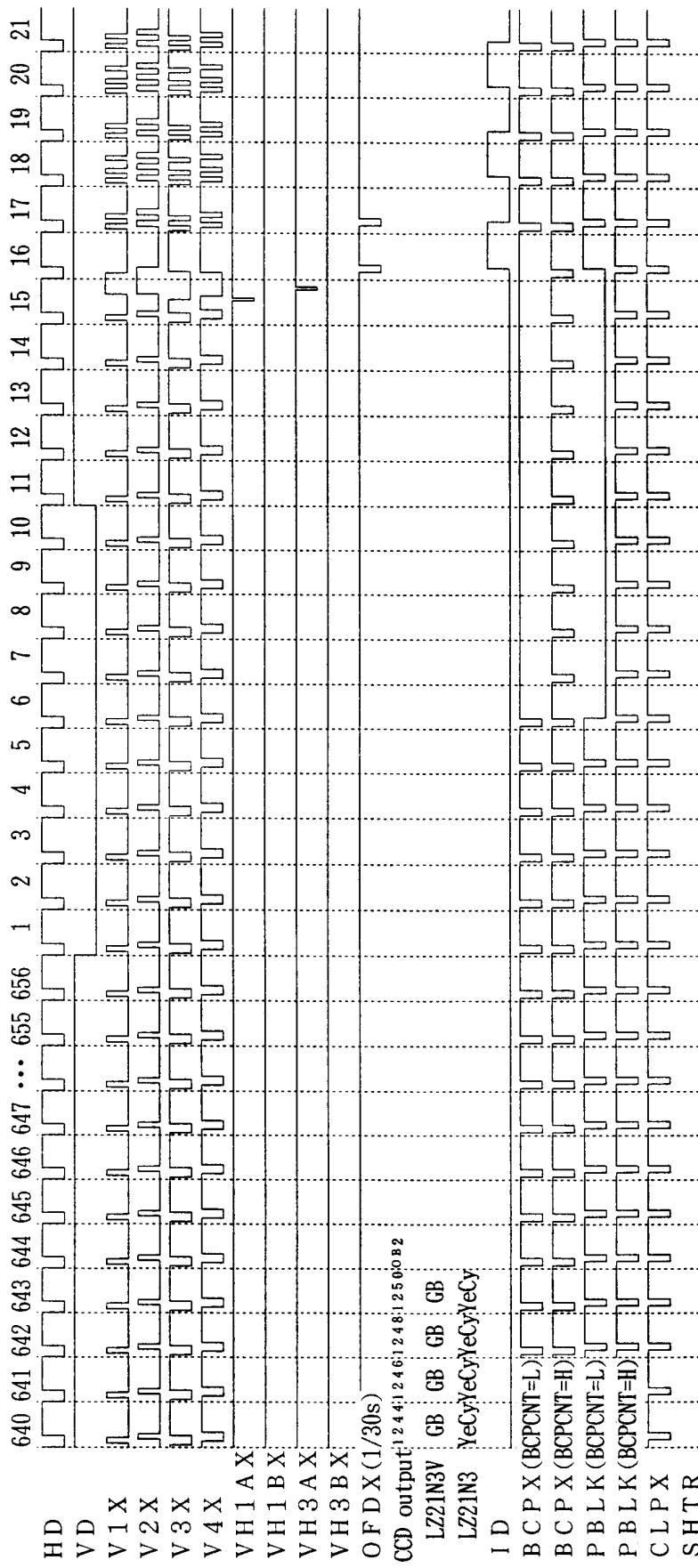
Vertical pulse timing-5

Still mode (⑤)



Vertical pulse timing-6

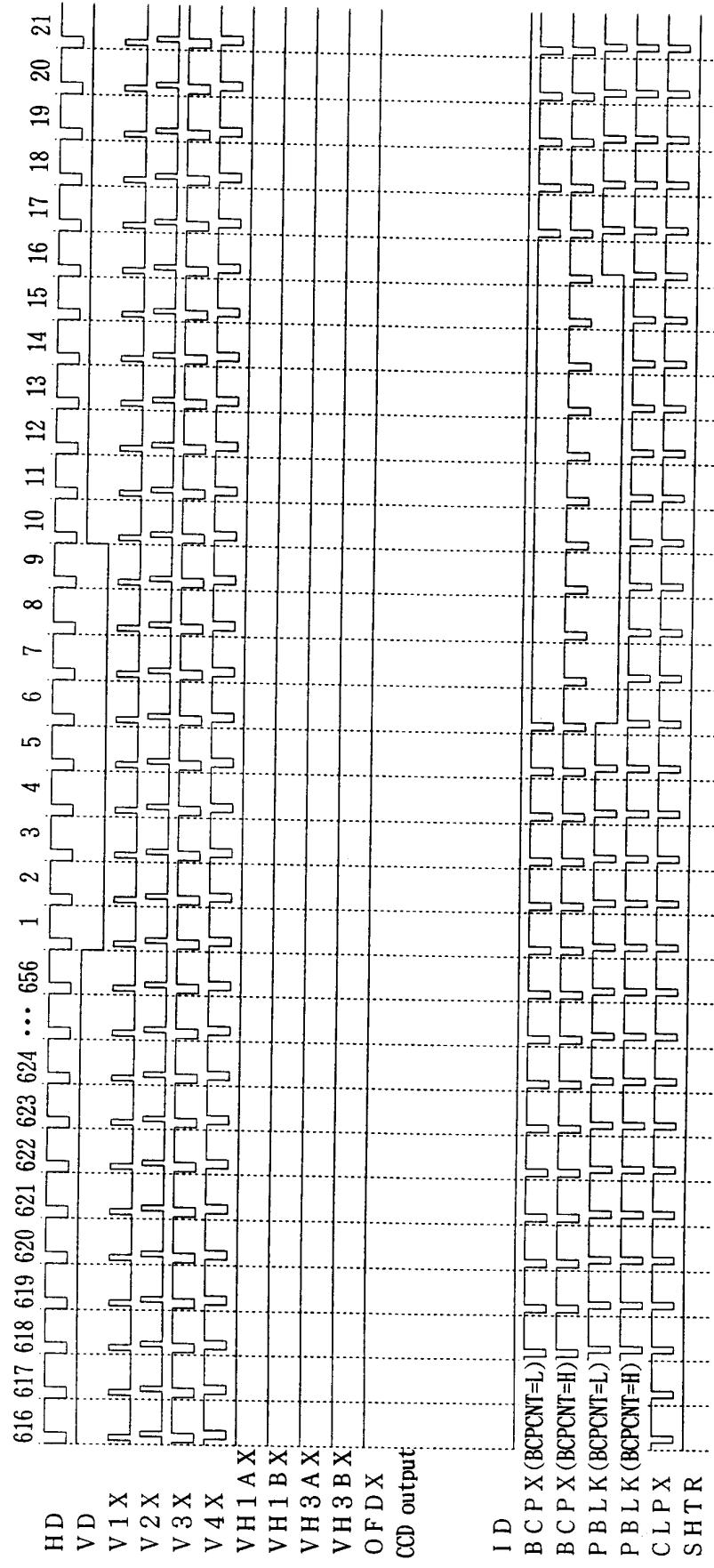
Switching from still to monitoring mode (①')



L R 3 8 6 1 3

Vertical pulse timing-7

Still mode (Low speed shutter) (③')



L R 3 8 6 1 3

Vertical pulse timing-8

2
HD
VD(1)
VD(2)

OFDX

I D(1)
I D(2)
B C P X
B C P X
P B L K
P B L K
C L P X
S H T R

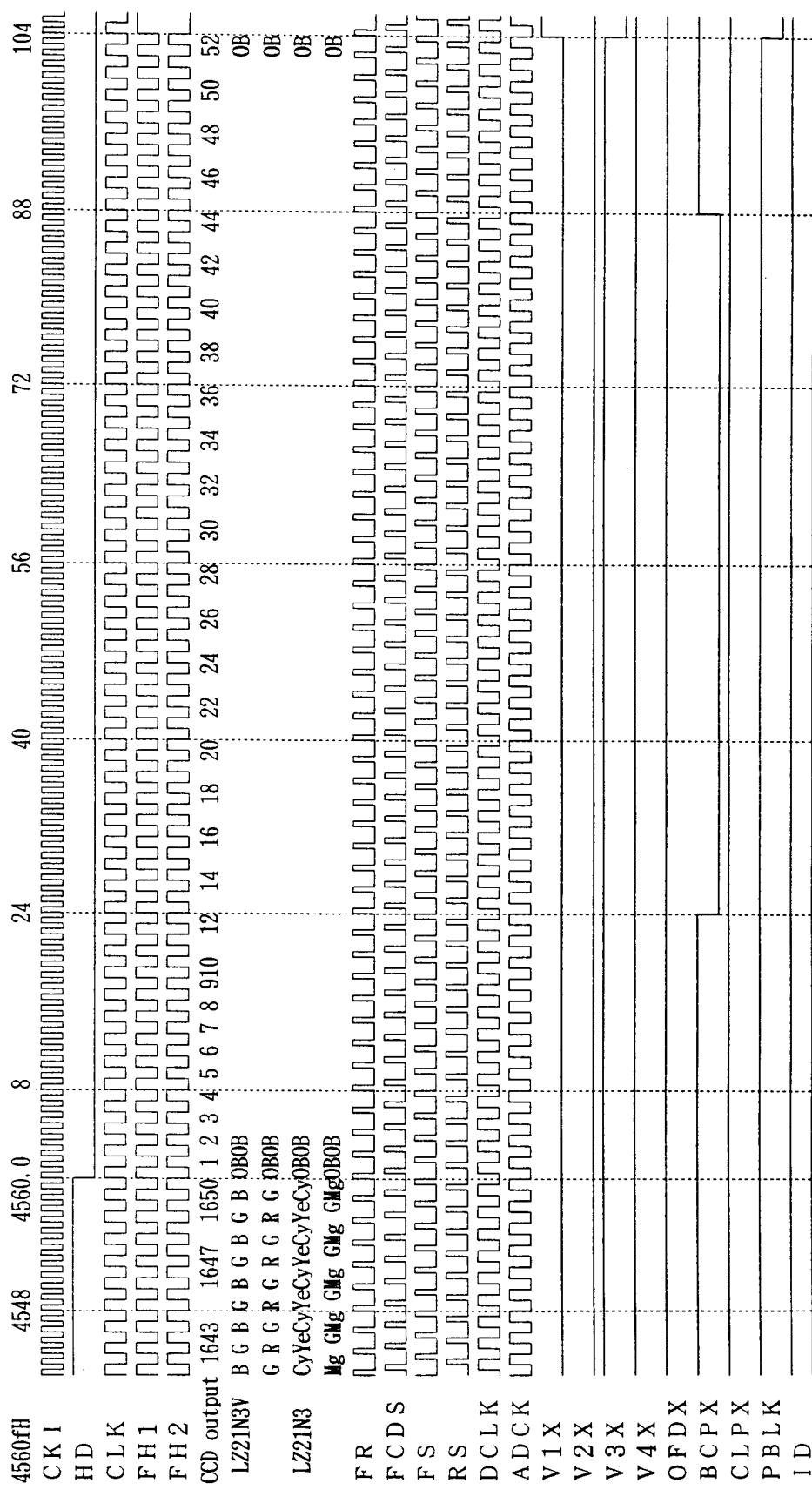
LR38613

CLPX
SHTR

6-3. Horizontal pulse timing

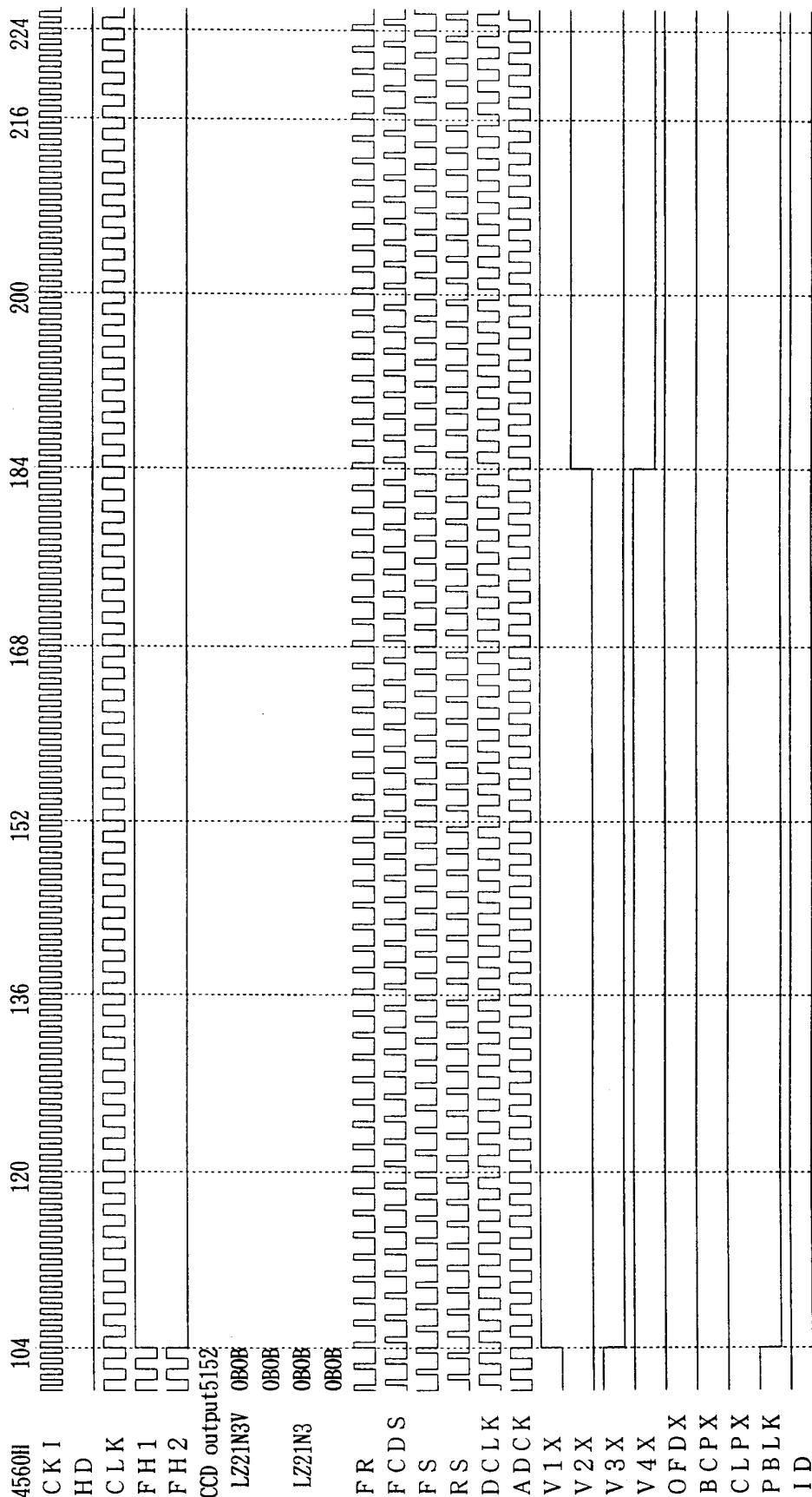
(1) Horizontal pulse timing (Monitoring mode) -1

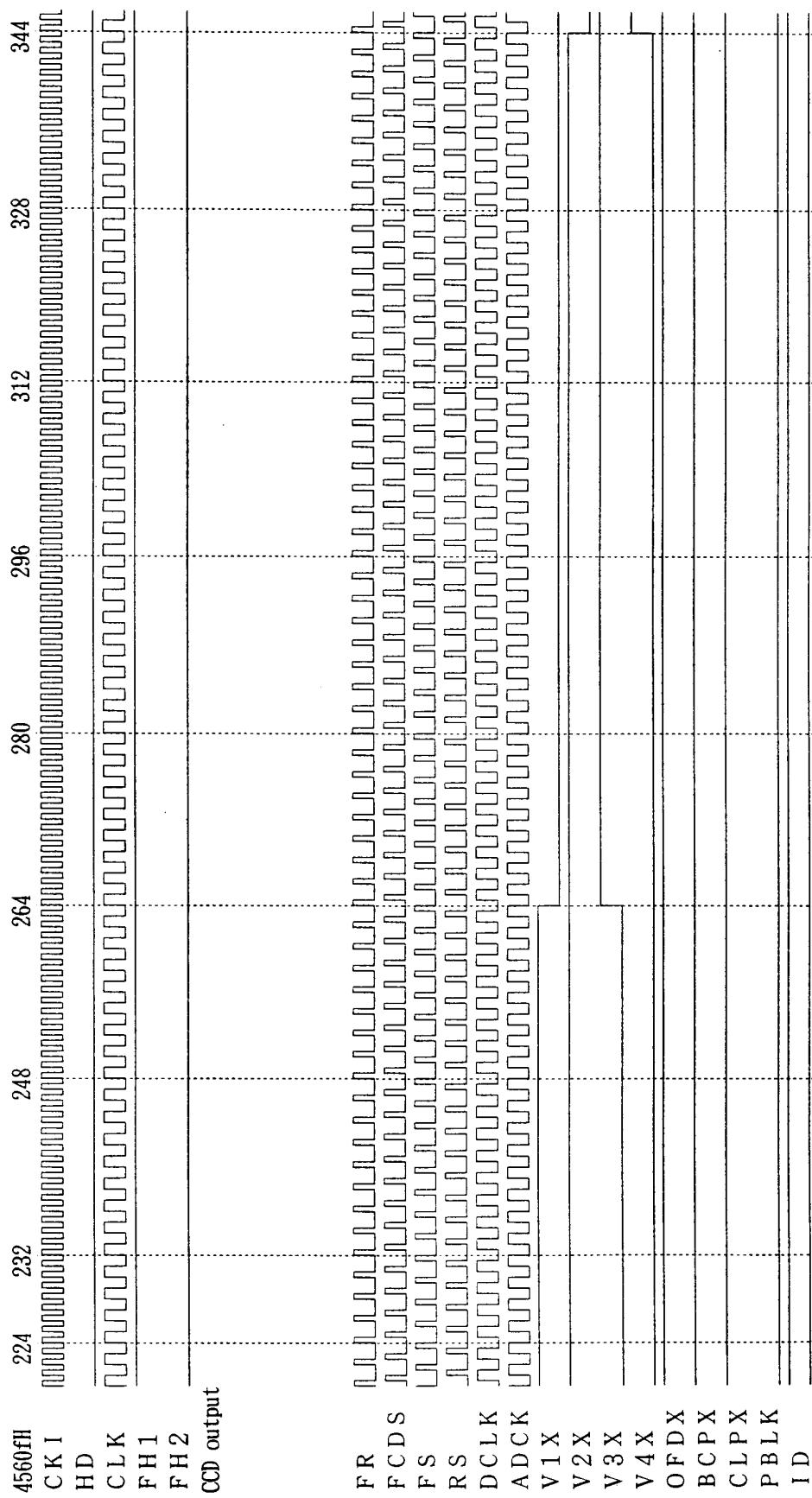
PLCH=H, WL1=H, WL2=L, WA1=L, WA2=H

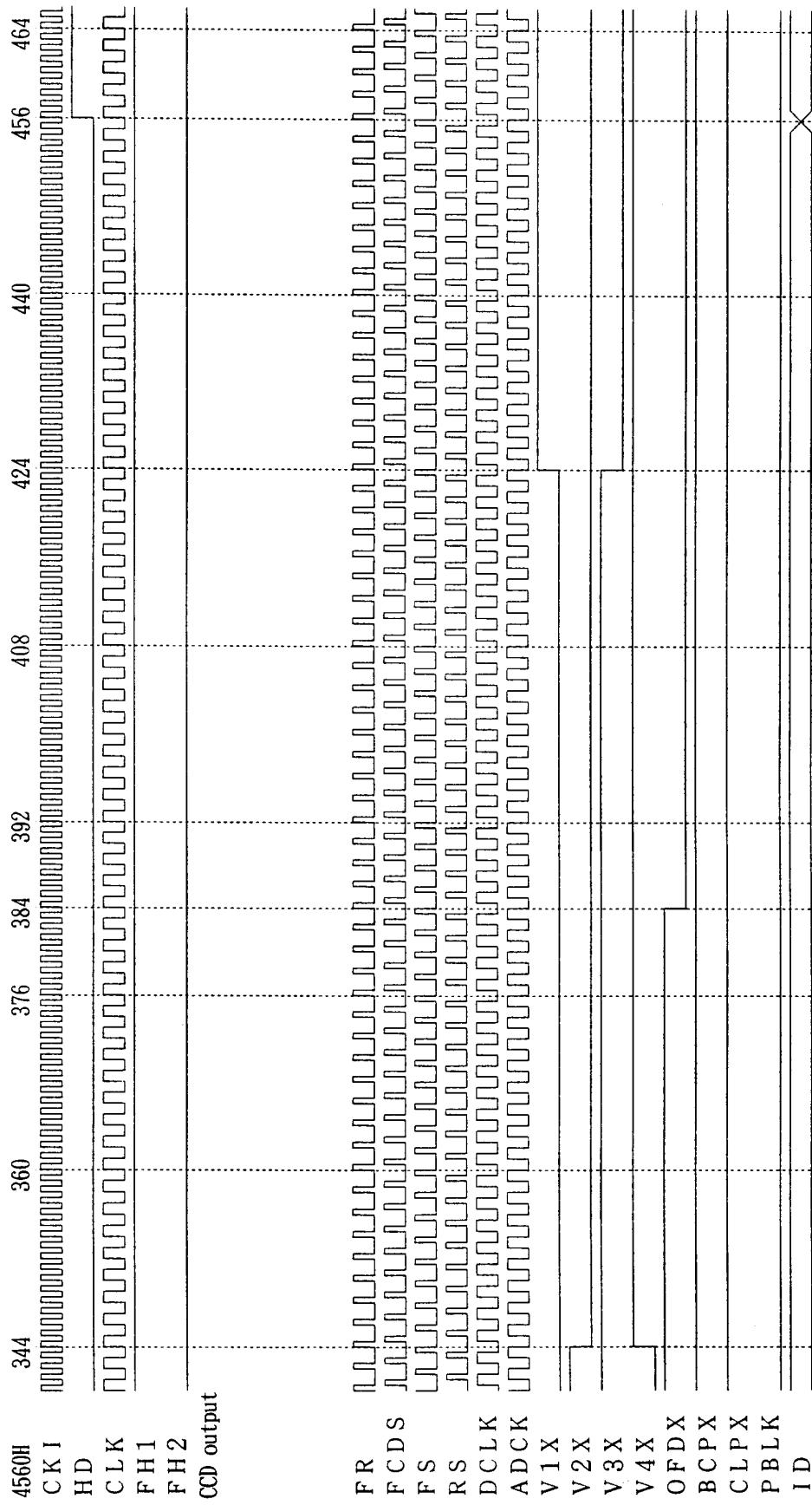


Horizontal pulse timing (Monitoring mode) -2

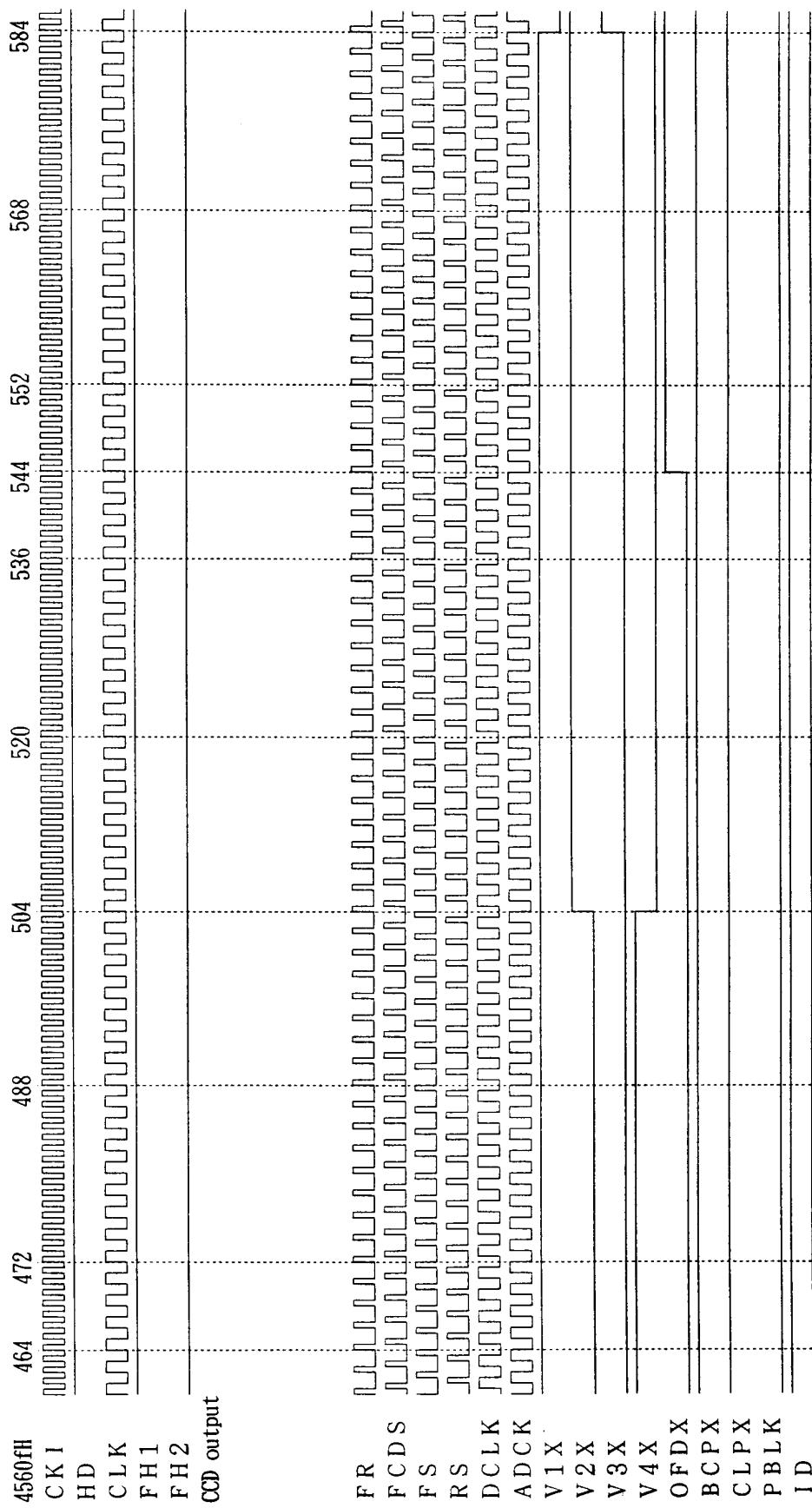
PLCH=H, ML1=L, ML2=L, MA1=L, MA2=H

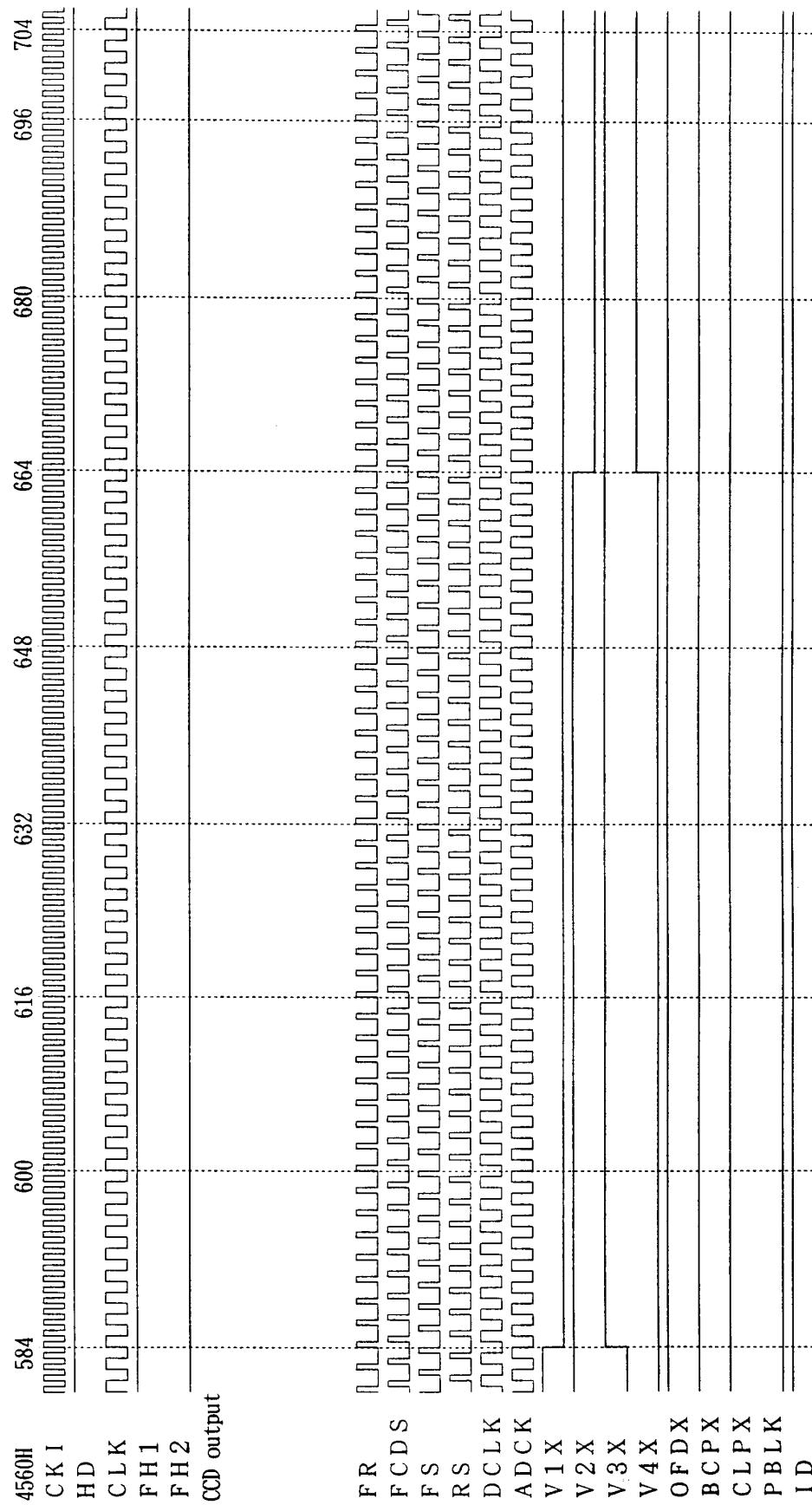


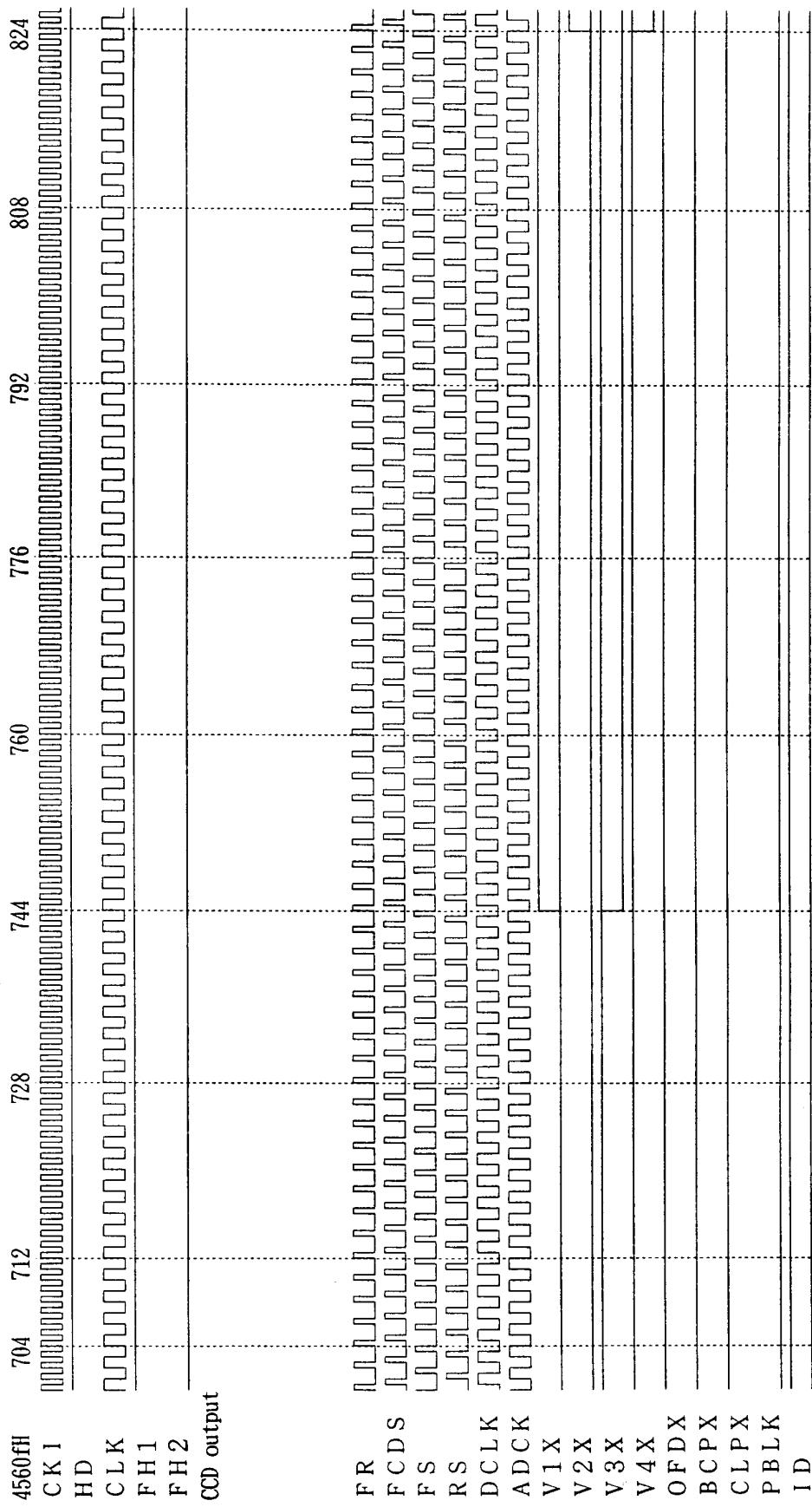
Horizontal pulse timing (Monitoring mode) -3
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H

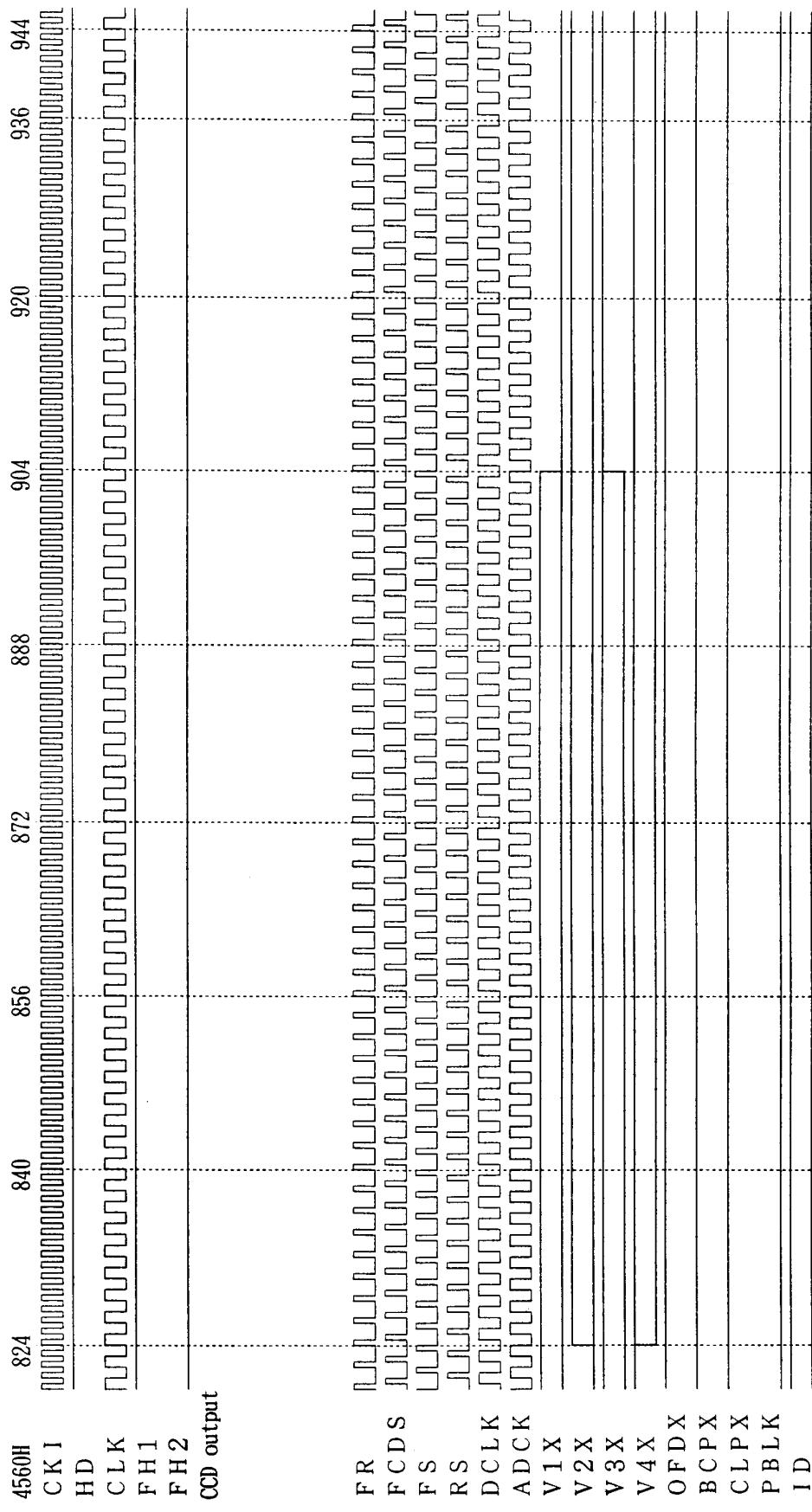
Horizontal pulse timing (Monitoring mode) -4
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H

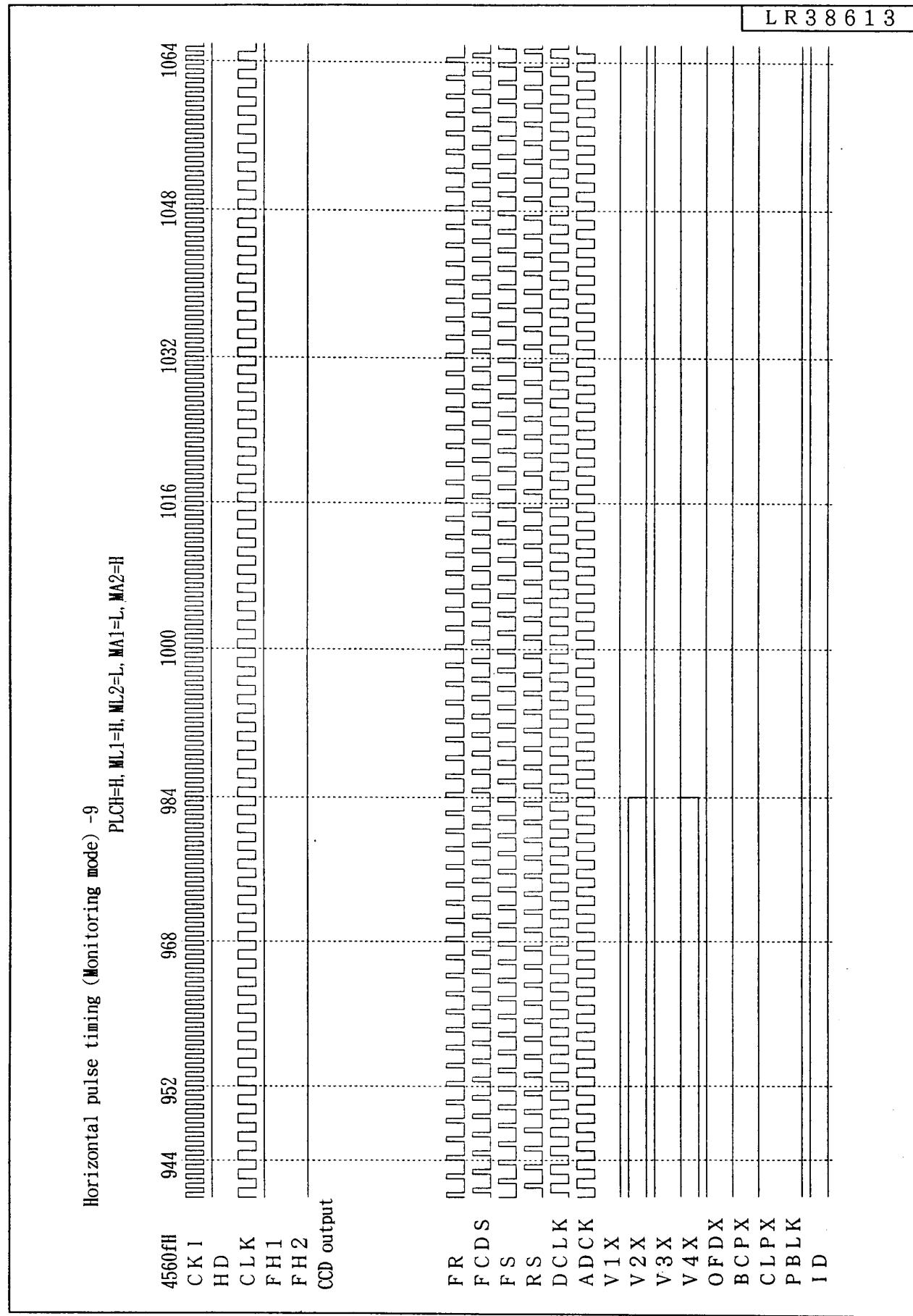
Horizontal pulse timing (Monitoring mode) -5
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H

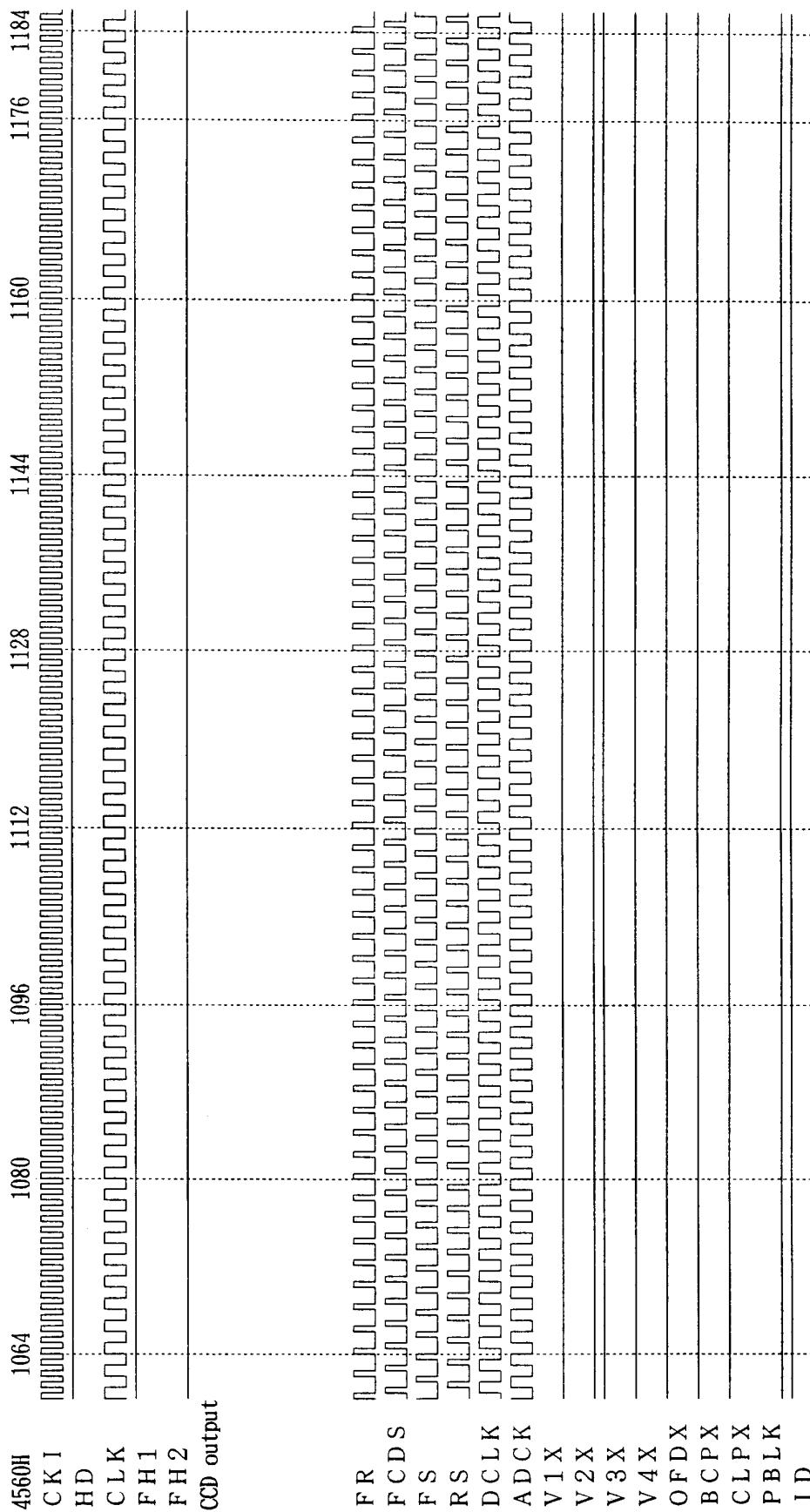


Horizontal pulse timing (Monitoring mode) -6
PLCI=H, ML1=H, ML2=L, MA1=L, MA2=H

Horizontal pulse timing (Monitoring mode) -7
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H

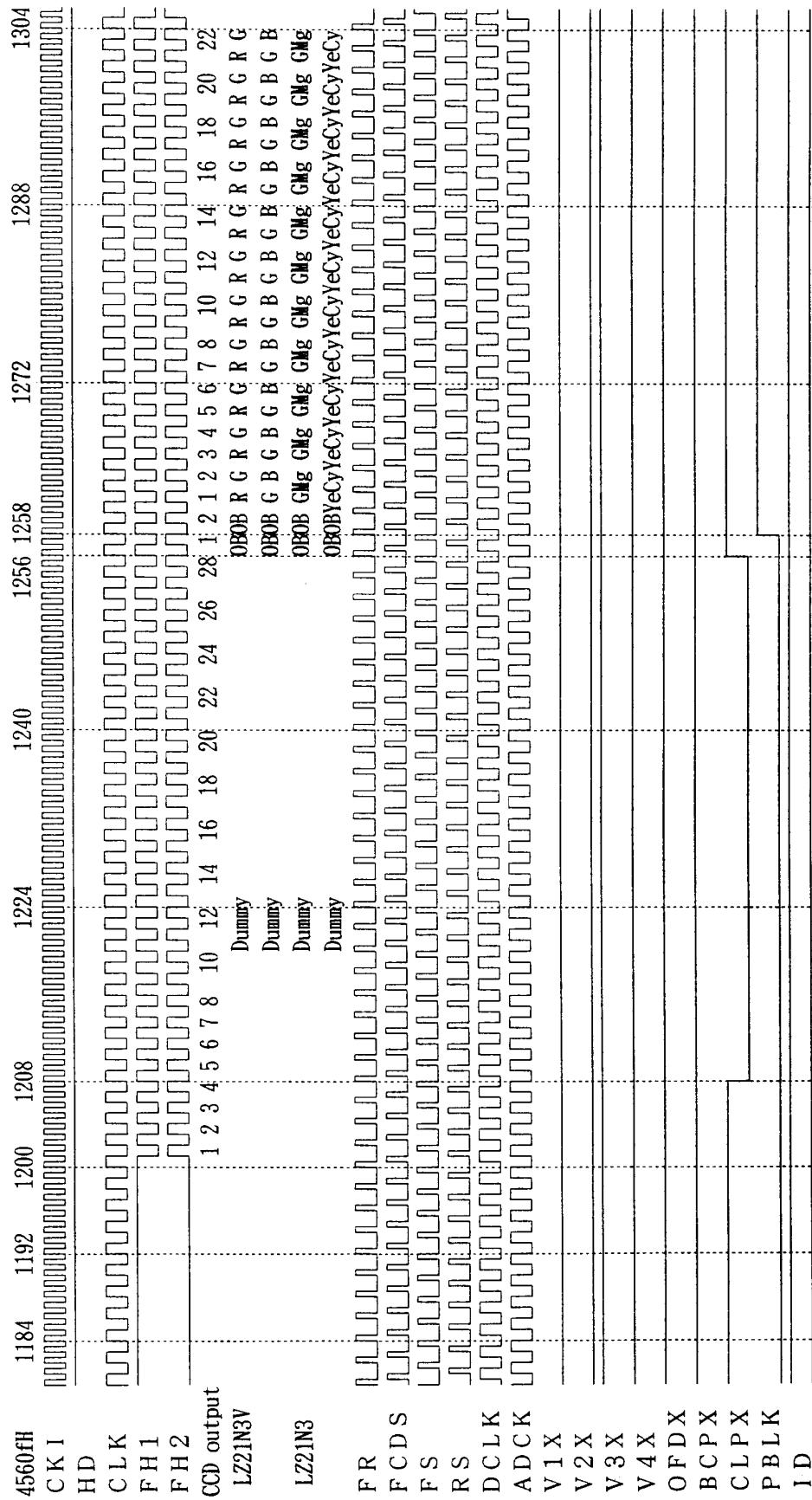
Horizontal pulse timing (Monitoring mode) -8
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H



Horizontal pulse timing (Monitoring mode) -10
PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H

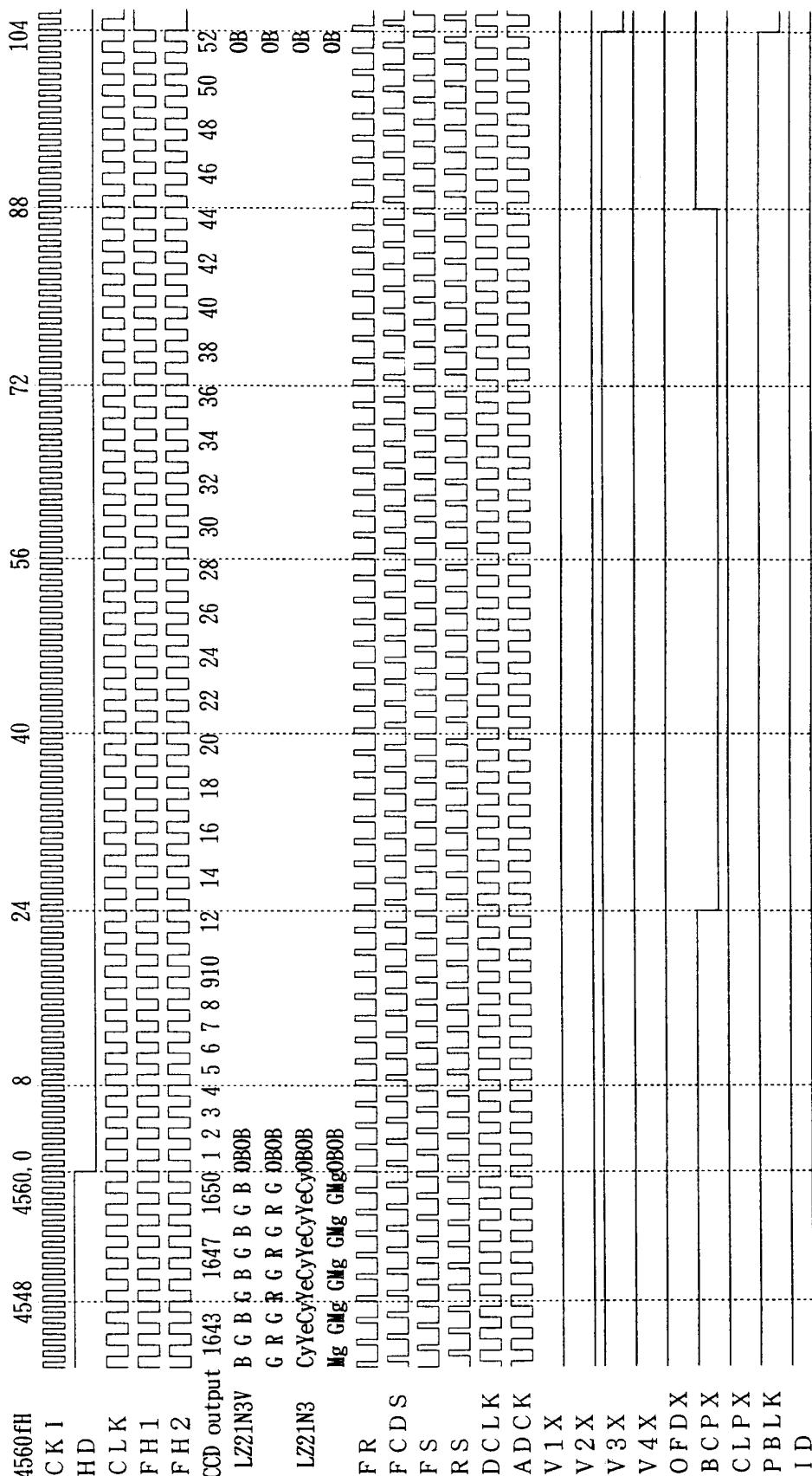
Horizontal pulse timing (Monitoring mode) -11

PLCH=H, ML1=H, ML2=L, MA1=L, MA2=H



(2) Horizontal pulse timing (Still mode) -1

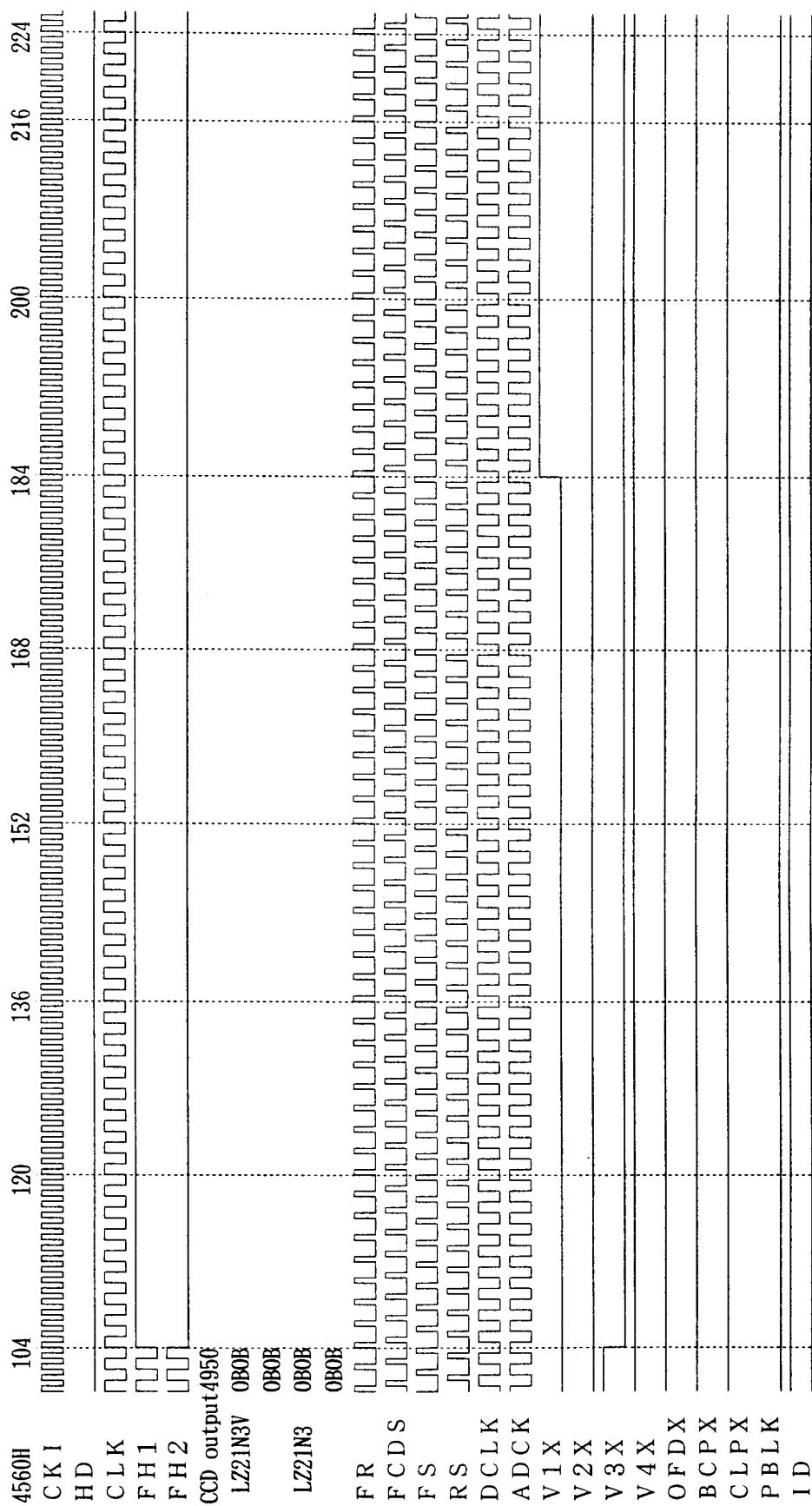
PLCH=H, $M_1=H$, $M_2=I$, $MA_1=H$, $MA_2=H$



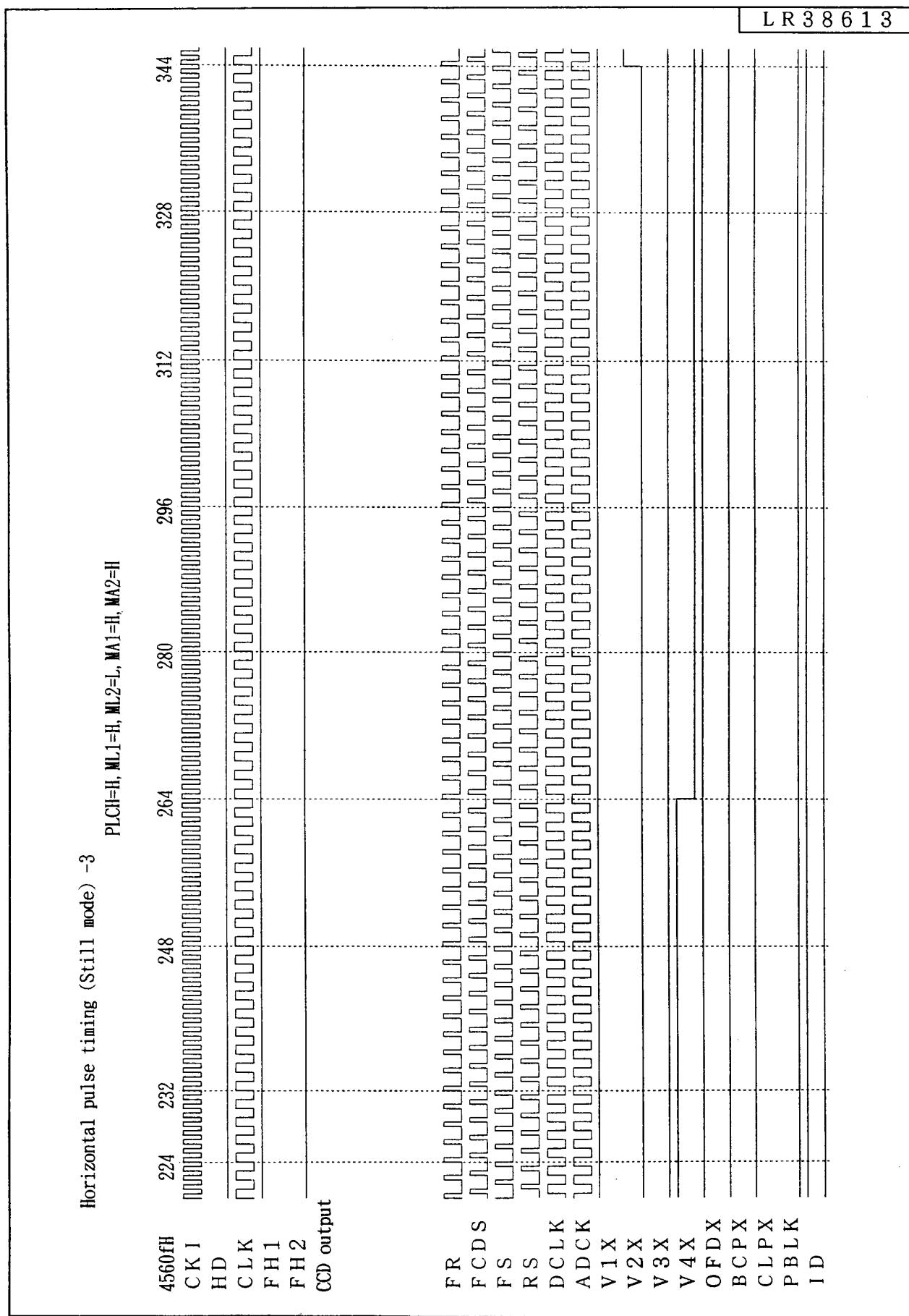
LR38613

Horizontal pulse timing (Still mode) -2

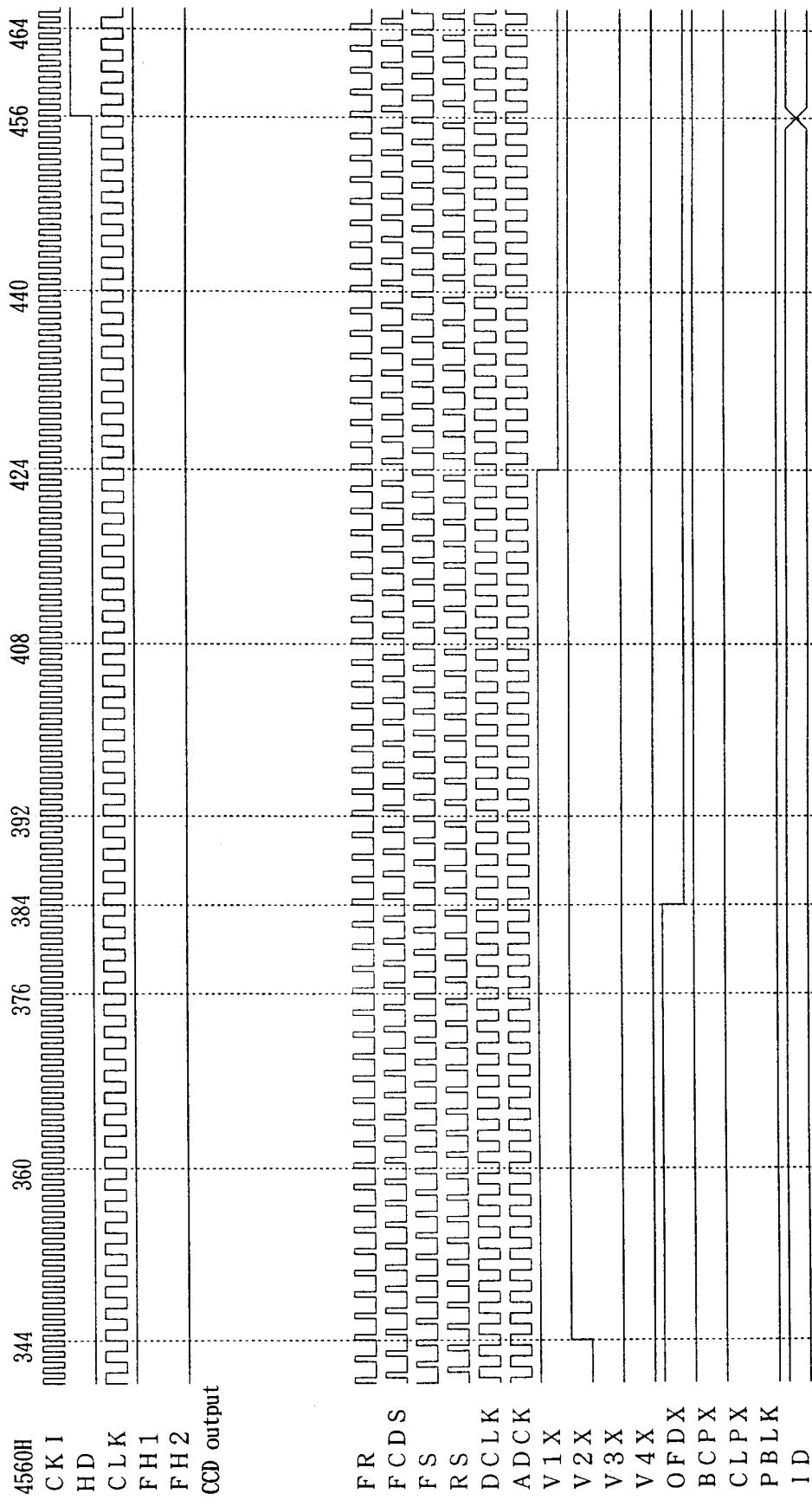
PLCH=H, ML1=H, ML2=L, MA1=H, MA2=H

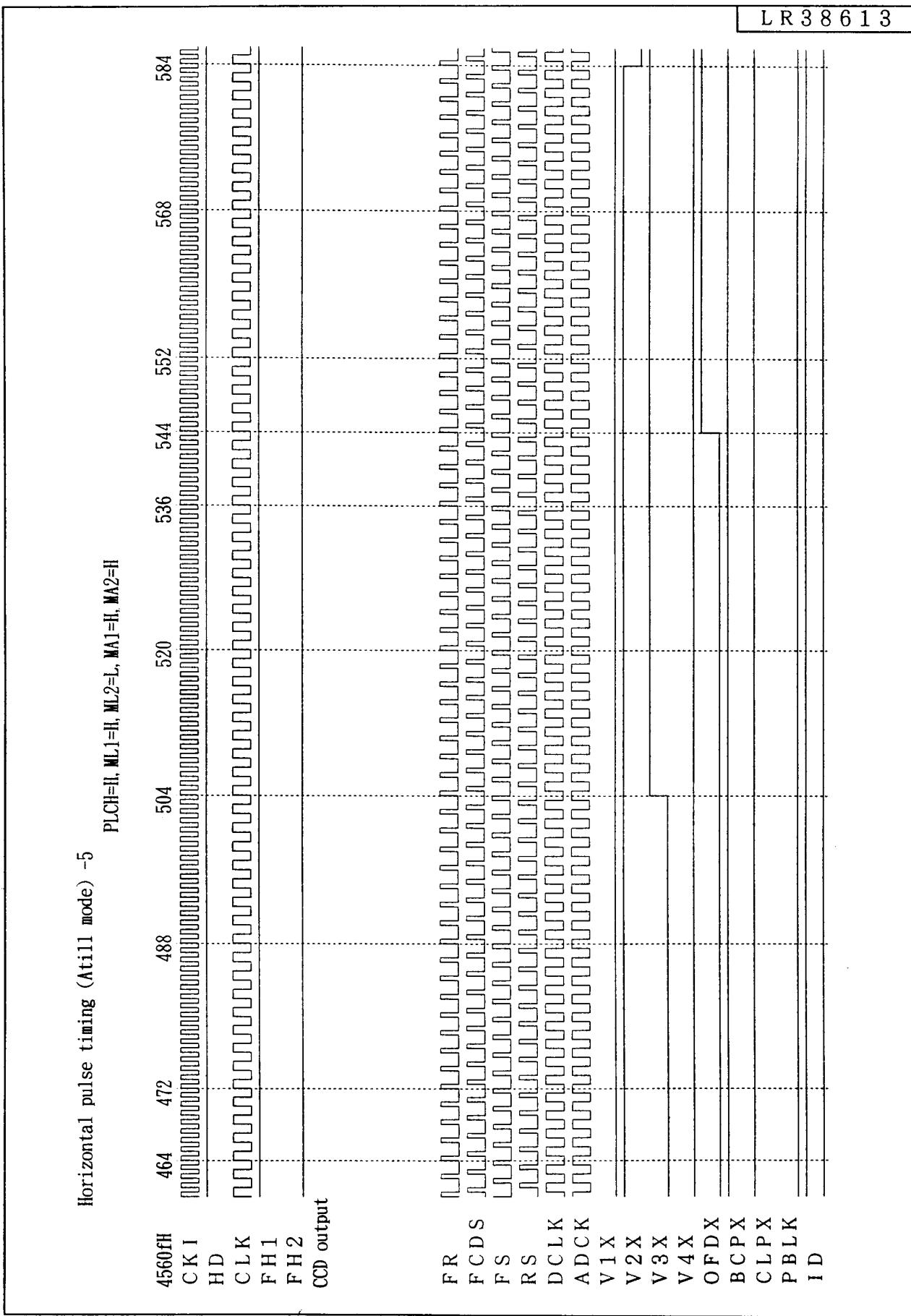


L R 3 8 6 1 3



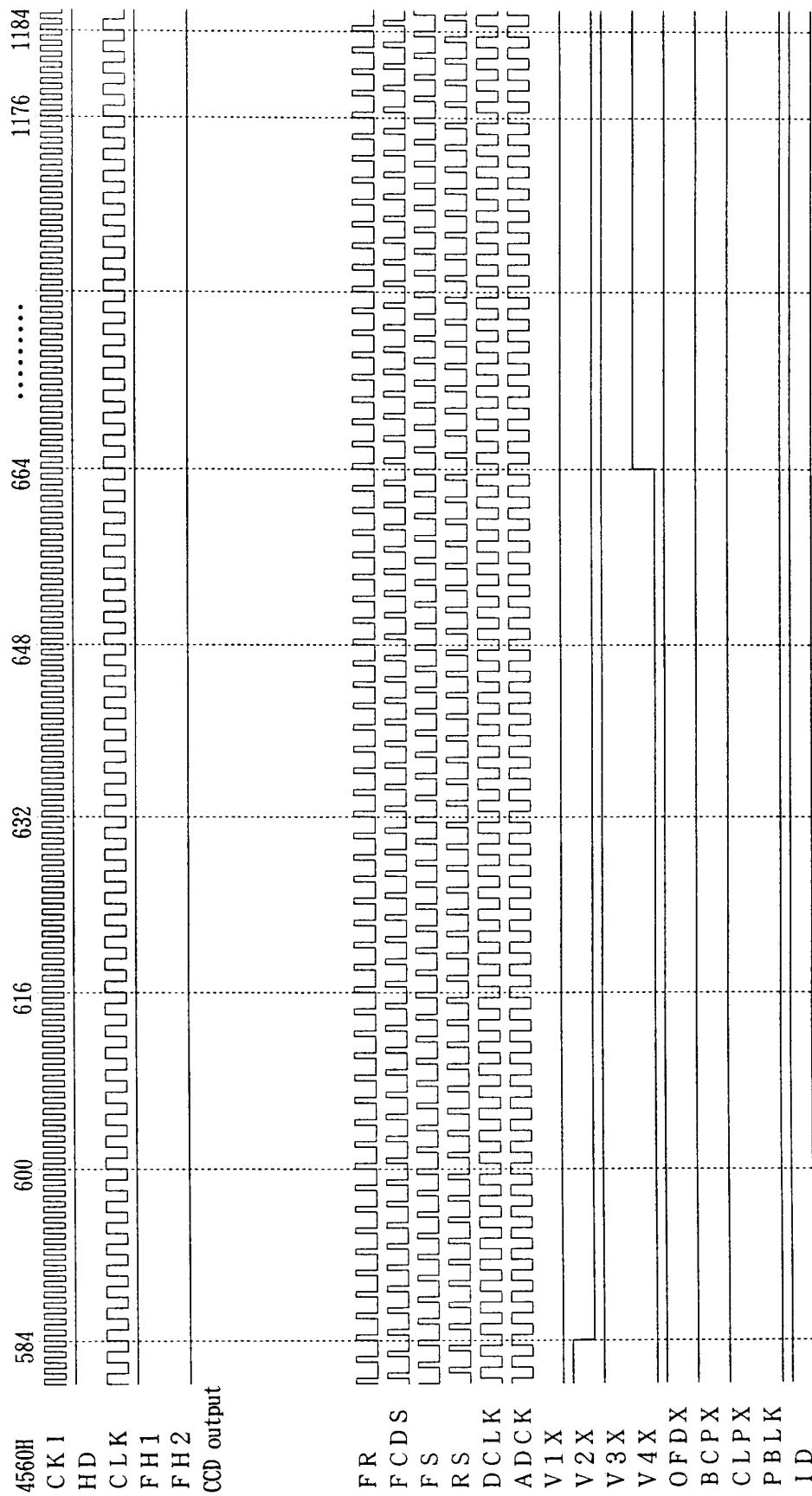
Horizontal pulse timing (Still mode) -4
PLCH=H, ML1=H, ML2=L, MA1=H, MA2=H





Horizontal pulse timing (Still mode) -6

PLCH=H, ML1=H, ML2=L, MA1=H, MA2=H



L R 3 8 6 1 3

Horizontal pulse timing (Still mode) -7

PI,CH=H, WI,1=H, WI,2=I, WA1=H, WA2=H

The figure is a timing diagram illustrating the temporal sequence of various digital signals across 28 time steps. The signals are categorized into several groups:

- Clock and Control:** CLK, HD, F1, F2, CCD output, L221N3V, L221N3.
- Frame Data:** FR, FCDS, FS, RS.
- Address and Clock:** DCLK, ADCK.
- Video Data:** V1X, V2X, V3X, V4X.
- Output and Bus:** OFDX, BCPX, CLPX, PBLK.

Annotations labeled "Dummy" are present in the following time steps:

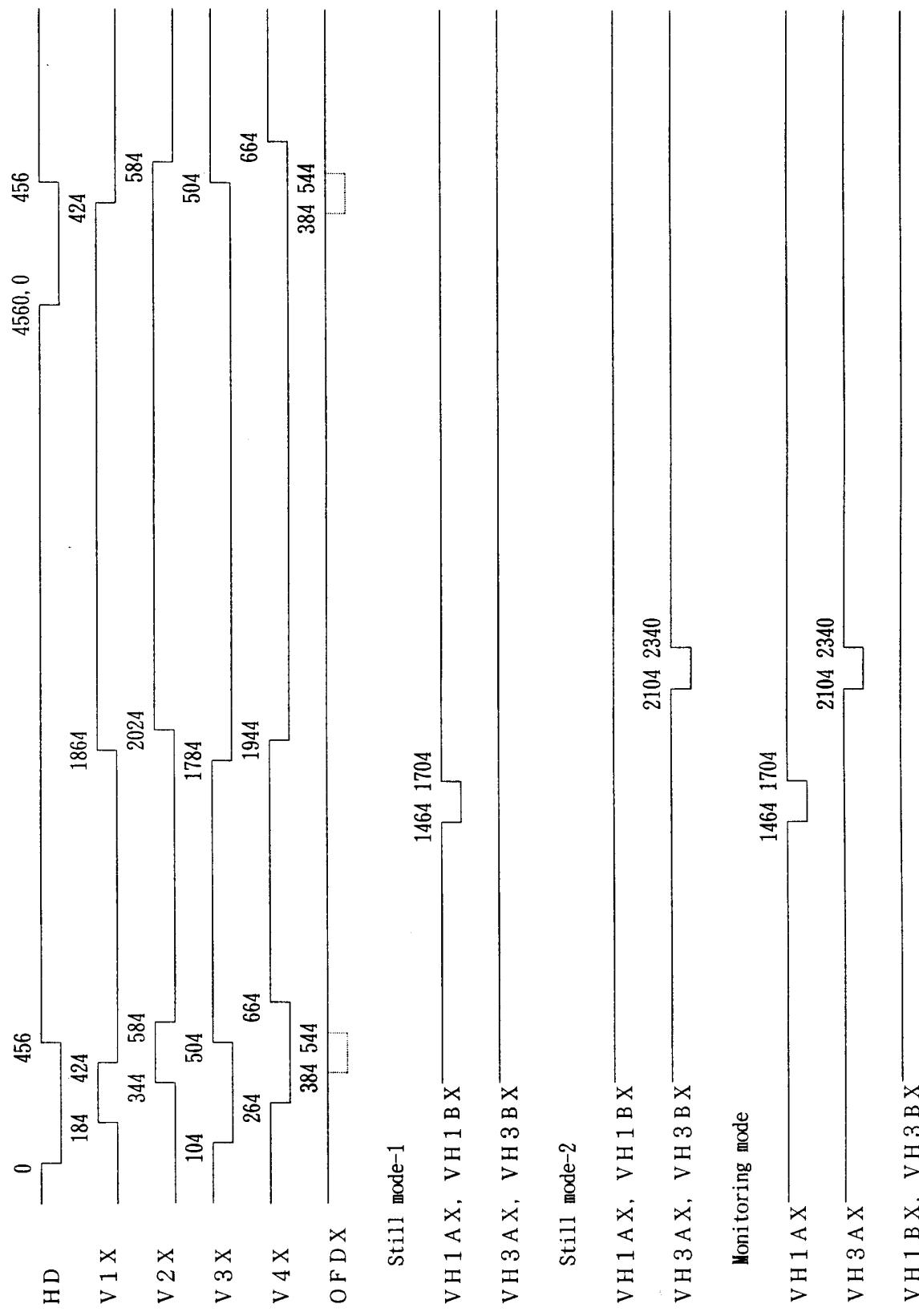
- CCD output: Step 12
- L221N3V: Steps 12, 16, 20
- L221N3: Step 12
- FR: Step 12
- FCDS: Step 12
- FS: Step 12
- RS: Step 12
- DCLK: Step 12
- ADCK: Step 12
- V1X: Step 12
- V2X: Step 12
- V3X: Step 12
- V4X: Step 12
- OFDX: Step 12
- BCPX: Step 12
- CLPX: Step 12
- PBLK: Step 12

Step numbers are also indicated for several signals:

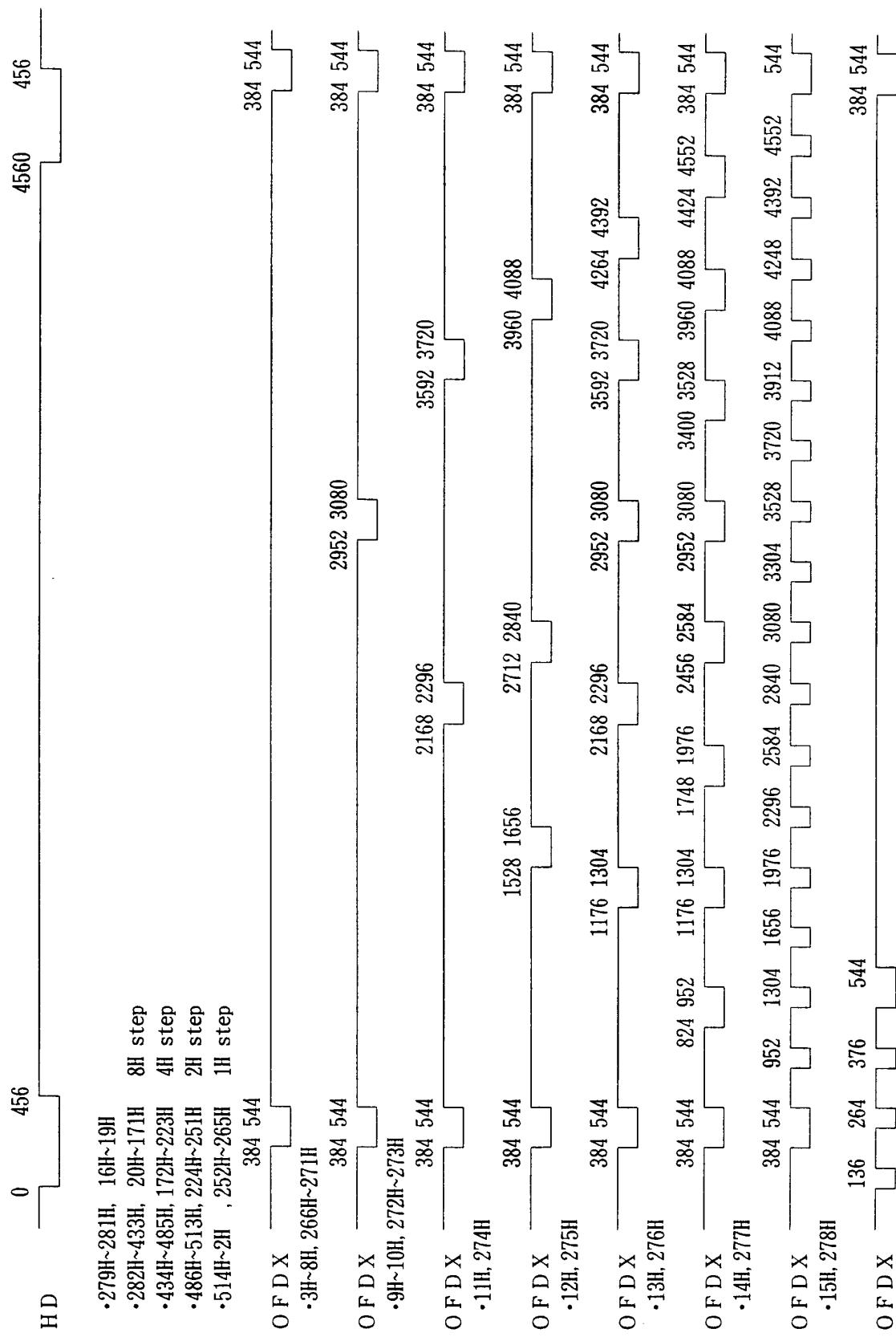
- CLK: 1184, 1192, 1200, 1208, 1224, 1240, 1256, 1258, 1272, 1288
- HD: 1304
- F1: 12
- F2: 12, 3, 4, 5, 6, 7, 8
- CCD output: 10, 12, 14, 16, 18, 20, 22
- L221N3V: 12, 16, 20
- L221N3: 12
- FR: 12
- FCDS: 12
- FS: 12
- RS: 12
- DCLK: 12
- ADCK: 12
- V1X: 12
- V2X: 12
- V3X: 12
- V4X: 12
- OFDX: 12
- BCPX: 12
- CLPX: 12
- PBLK: 12

L R 3 8 6 1 3

6-4. Read-out pulse timing

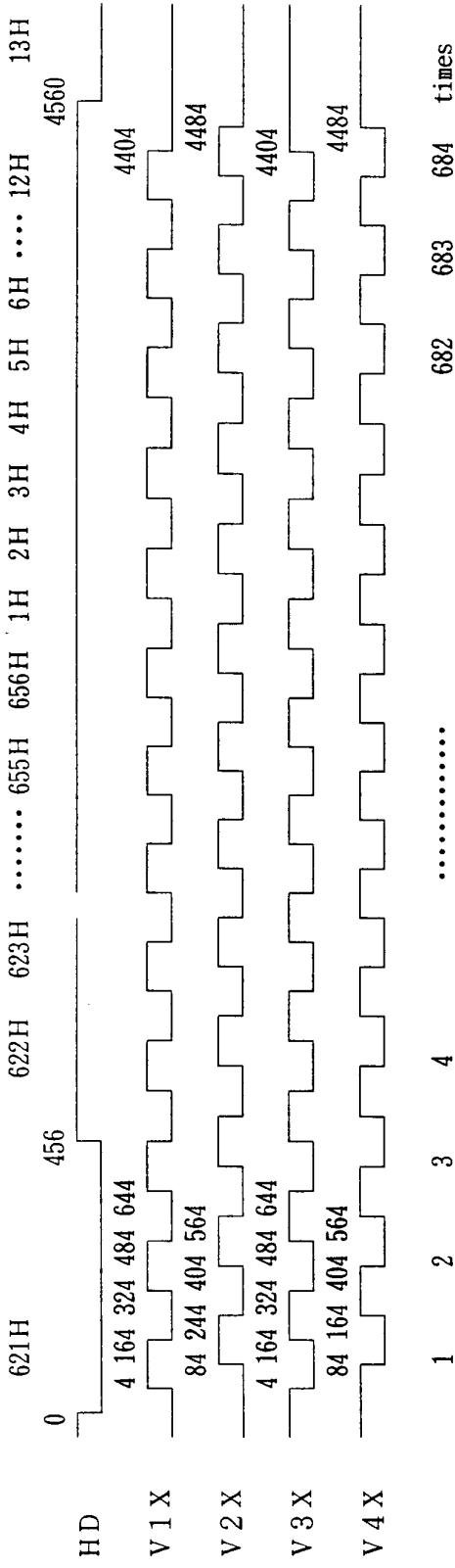


6-5. Electronic shutter pulse timing

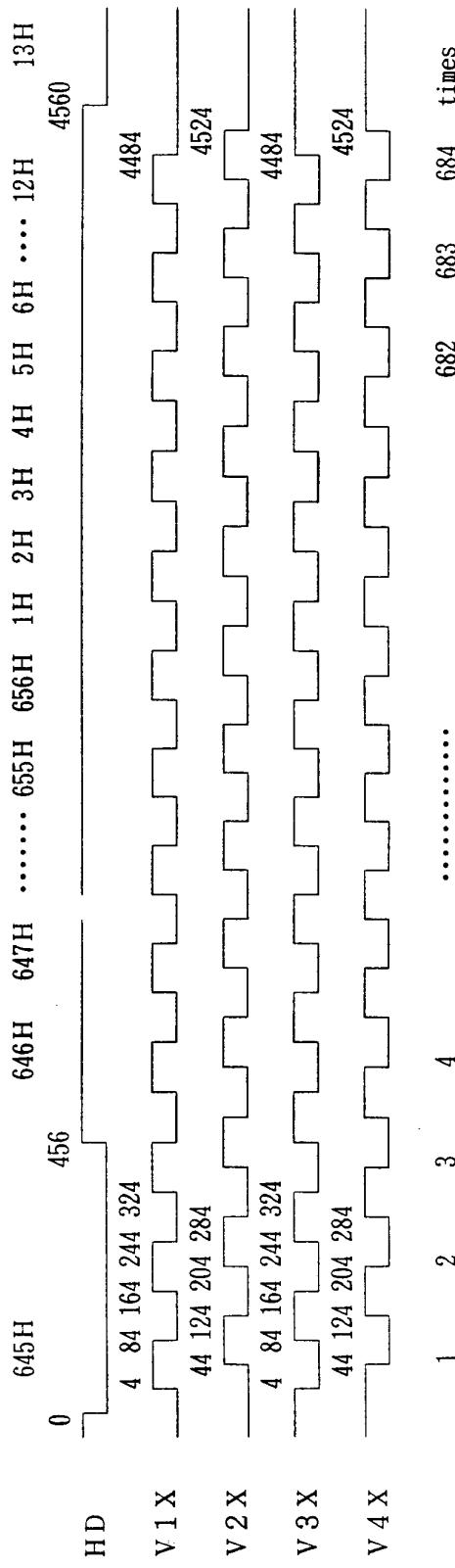


6-6. Sweep-out pulse timing

1st field of still picture



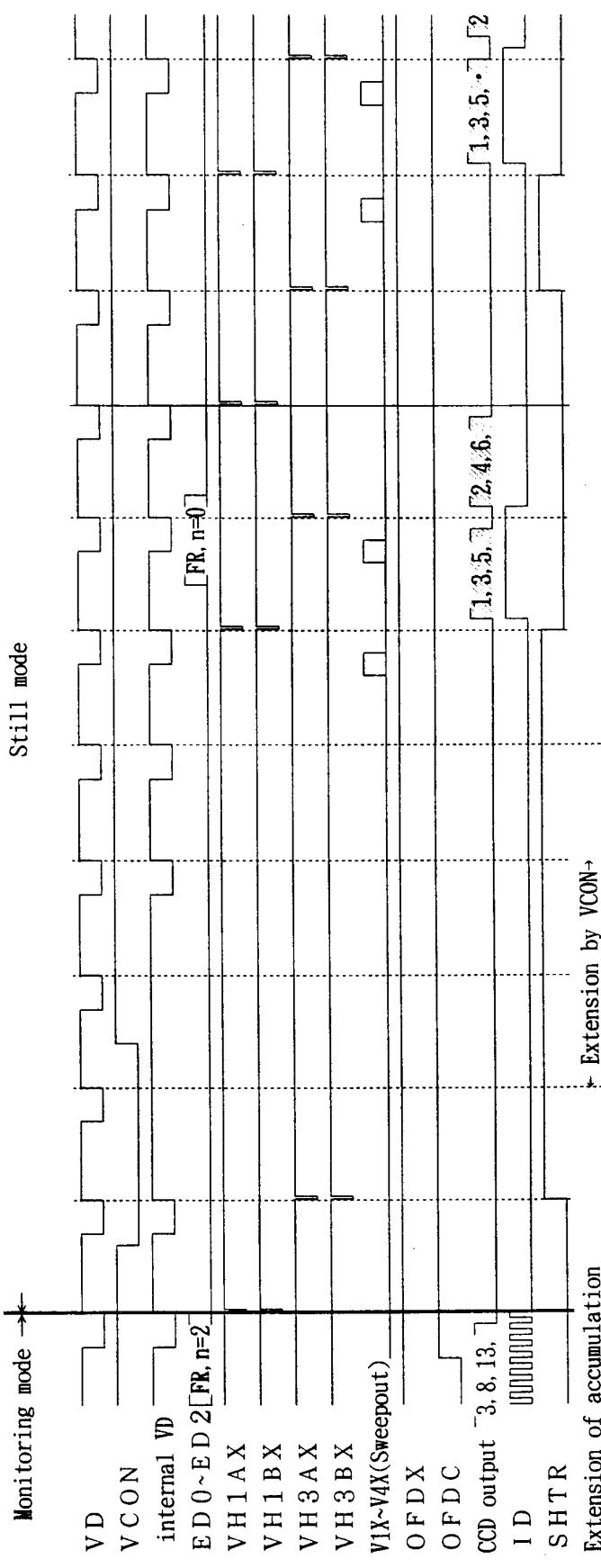
2nd First field of still picture

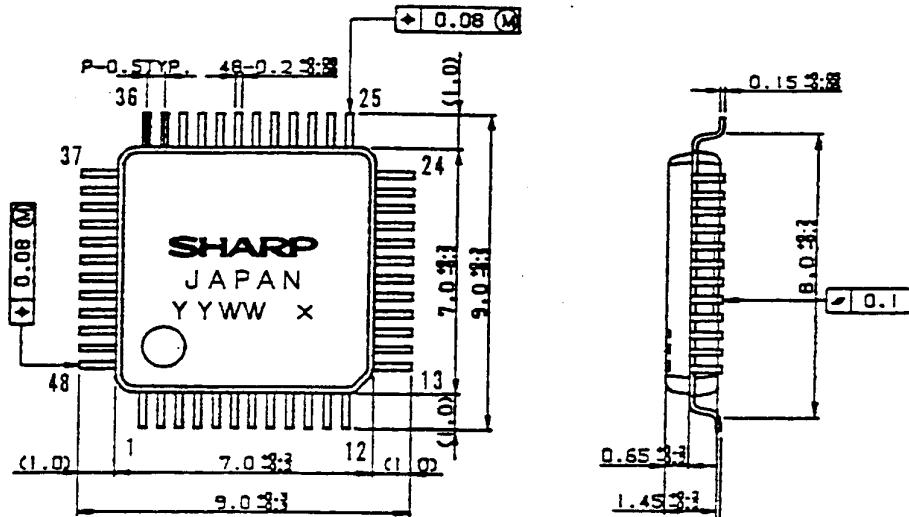


L R 3 8 6 1 3

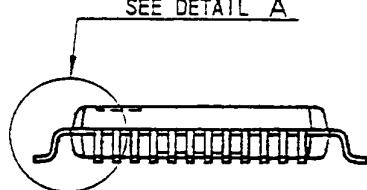
- 6-7. Input pulse timing of VCON
 It's should be set fields data $n \geq 2$ for long accumulation

3 fields accumulation($n=2$) of still mode



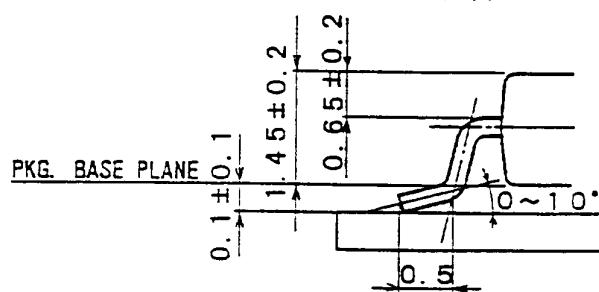


SEE DETAIL A



PKG. BASE PLANE

DETAIL A



名称 NAME	QFP48-P-0707	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE
DRAWING NO.	AA1035	単位 UNIT	mm	プラスチックパッケージの寸法、バーリを含まないものとする。 Plastic body dimensions do not include burr of resin.

Timing IC for 2.0M CCD, LR38613