Product Brief, Rev. 1
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU6X31FT
1.0—1.34 Gbits/s or 2.0—2.68 Gbits/s Serializer and Deserializer

Features

- Designed to operate in Ethernet, fibre channel (HSPI compatible), *Infiniband**, or backplane applications.
- Operationally compliant with the fibre channel X3T11. Provides FC-0 services at 1.0 Gbit/s—1.34 Gbits/s and 2.0 Gbits/s—2.68 Gbits/s.
- Selectable data rate (1.0 Gbit/s—1.34 Gbits/s or 2.0 Gbits/s—2.68 Gbits/s).
- 100 MHz—134 MHz differential PECL or single-ended TTL reference clock.
- 10-bit parallel SSTL-3 input interface.
- 10-bit parallel TTL output interface.
- Compatible with 8B/10B encoded data.
- Comma character recognition (K28.1, K28.5, K28.7) for alignment to word boundary.
- Two 50.0 MHz—67.0 MHz receive byte clocks (1.0 Gbit/s—1.34 Gbits/s) or two 100 MHz—134 MHz receive byte clocks (2.0 Gbits/s—2.68 Gbits/s).
- Automatic lock to reference in absence of receive data.
- Receive serial-data signal-detect output.
- PECL high-speed interface I/O for use with optical transceiver, coaxial copper media, or shielded twisted pairs.
- Requires one external resistor for PECL output reference level definition and one external resistor for bias current generation.
- Requires no external components for clock recovery and frequency synthesis.
- 100-pin, 14 mm TQFP package.
- Under 1 W per transceiver.
- Low powerdown dissipation.
- 3.3 V ± 5% power supply.
- 0 °C—70 °C ambient temperature.

Potential LU6X31FT Applications:

- Stand-alone transceiver product.
- Transceiver macrocell template.

Description

The LU6X31FT transceiver provides for serial data transmission over fiber or coaxial media at 1.0 Gbit/s to 1.34 Gbits/s or 2.0 Gbits/s to 2.68 Gbits/s. The device is available in a 100-pin, 14 mm TQFP package for single-channel applications. The block diagram of the chip is shown in Figure 1.

The transmitter section accepts SSTL-3 data at the parallel input port. It also accepts the low-speed TTL/PECL compatible system clock and uses this clock to synthesize the internal high-speed serial bit clock. In the 1.0 Gbit/s to 1.34 Gbits/s mode, the parallel input data are latched on the falling edge of the low-speed TBC clock. In the 2.0 Gbits/s to 2.68 Gbits/s mode, the parallel input data are framed by the rising and falling edges of the low-speed TBC clock. The serialized data are then available at the differential PECL output terminated in 50 Ω or 75 Ω to drive either an optical transmitter or coaxial media.

The receive section receives high-speed serial data at its differential PECL input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. The retimed data are deserialized and presented as 10-bit parallel data on the output port. A divided-down version of the recovered clock, synchronous with parallel data characters, is also available as a TTL-compatible output. The receive section recognizes the comma sequence and aligns the comma-containing character on the word boundary.

Critical analog and digital circuits in the transceiver are implemented with differential topologies for immunity to power supply, substrate, and other common-mode noise sources. Pseudo-ECL logic, implemented with BiCMOS circuits, is used in the timing recovery circuits of the receiver. Once the data have been retimed, conventional low-power CMOS logic is used to further process the data.

* *InfiniBand* is a trademark of the InfiniBand Trade Association.

Description (continued)

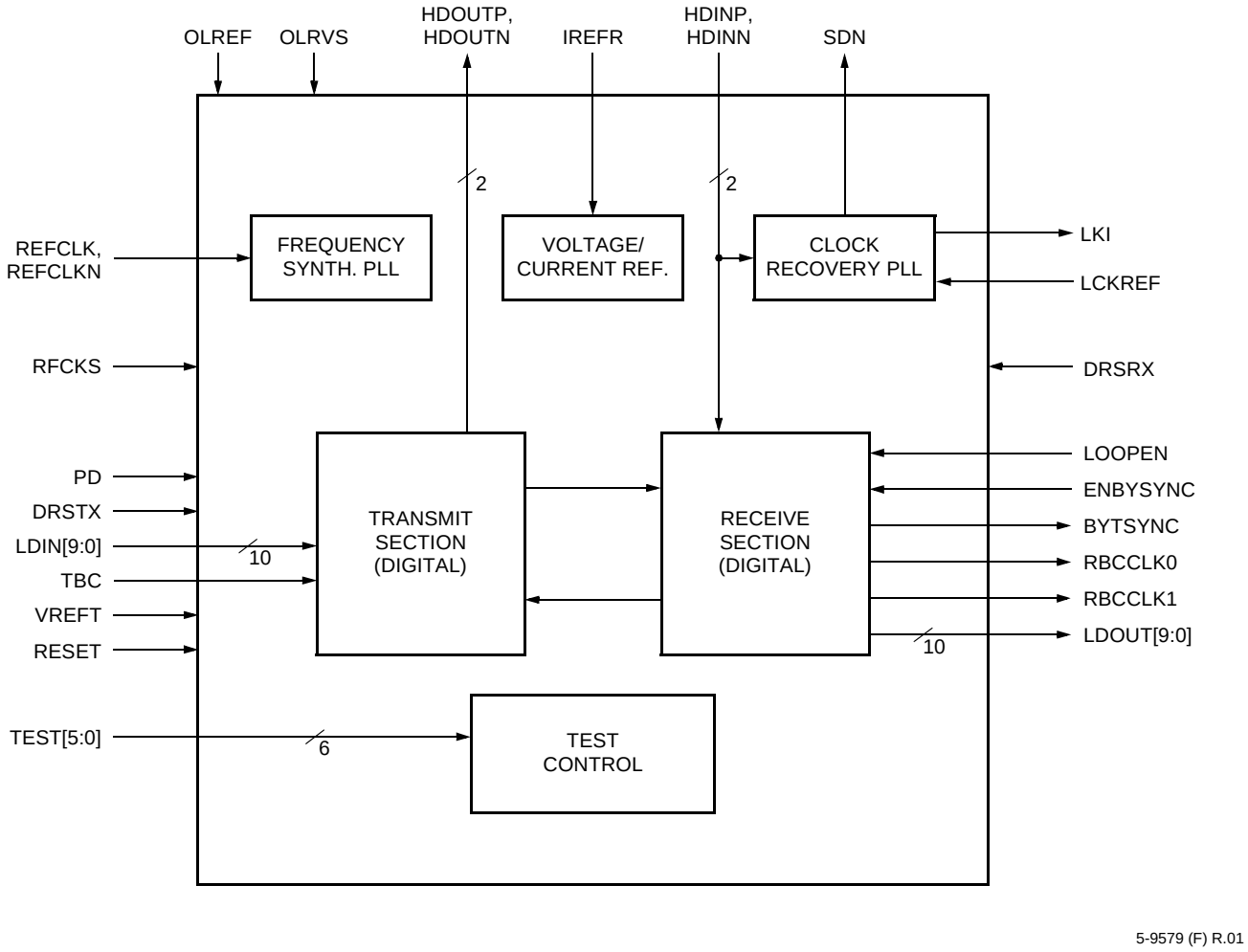

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Figure 1. LU6X31FT Functional Block Diagram

Description (continued)

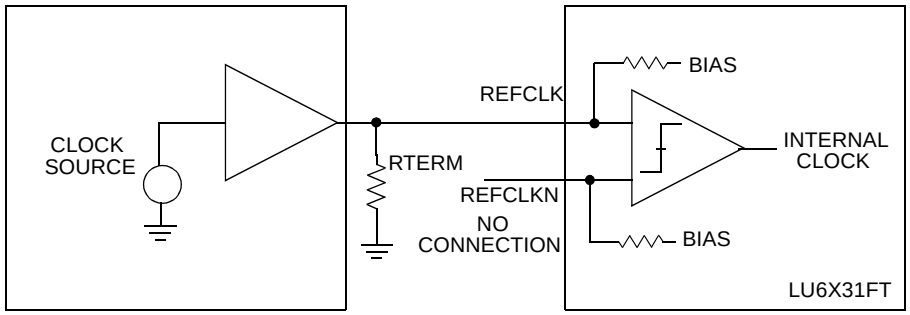

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Figure 2. Reference Clock Connections with Single-Ended TTL Source (RFCKS = 1)

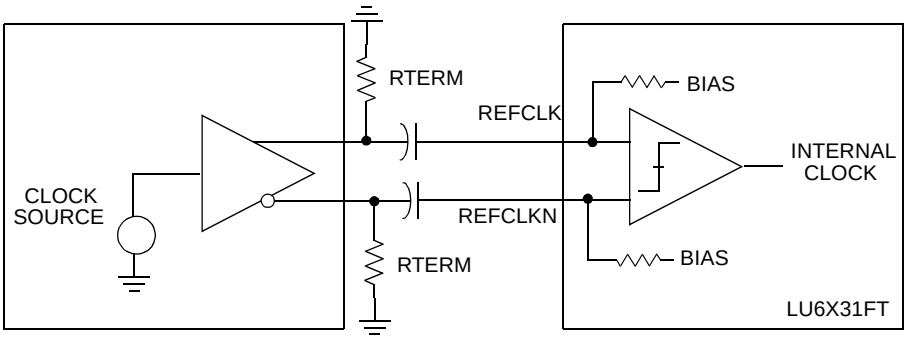

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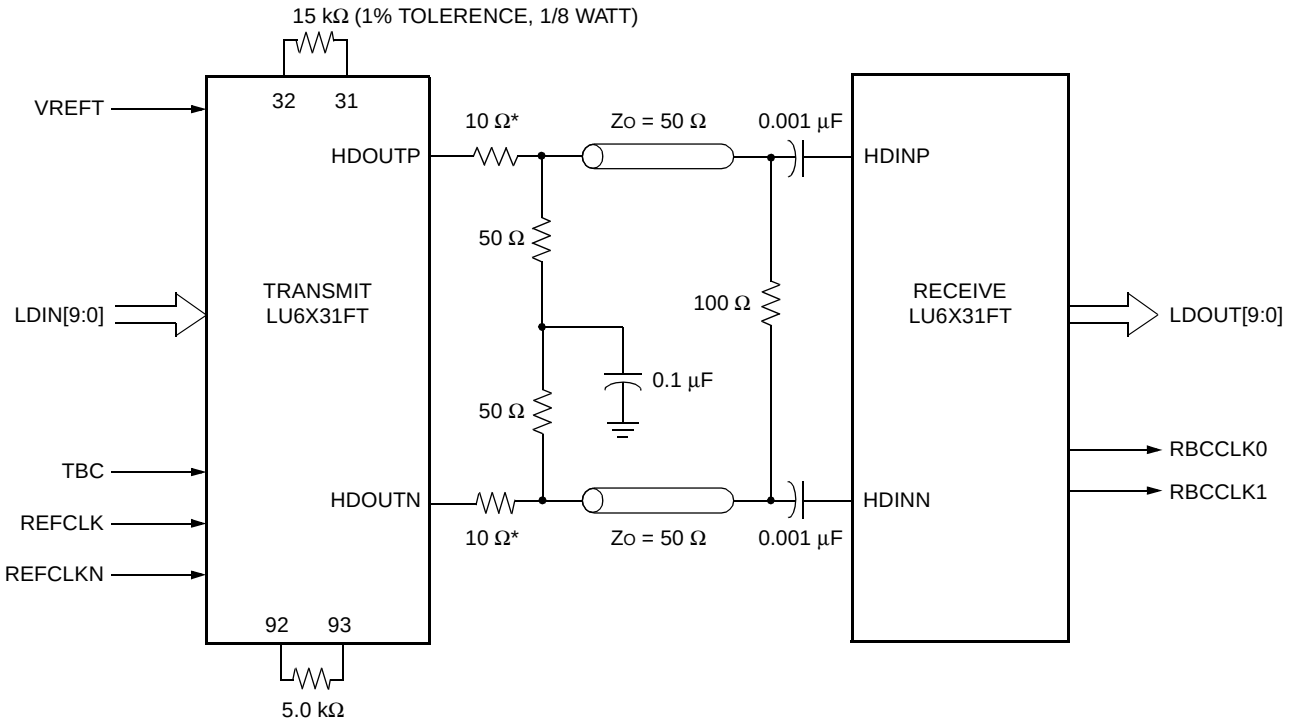
Figure 3. Reference Clock Connections with Differential PECL Source (RFCKS = 0)

Description (continued)



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* External damping resistor (10 Ω maximum).

Figure 4. Typical Configuration

Table 1. External Resistor Value vs. Differential Output Level Viewing

Resistor Value	Termination Impedance	Differential Output Voltage
7.5 kΩ/11.25 kΩ	50 Ω/75 Ω	0.8 V
5 kΩ/7.5 kΩ		1.2 V
4 kΩ/6 kΩ		1.6 V

Functional Description

Transmitter Section

The transmitter brings in 8B/10B encoded bits in 10-bit parallel form for 1.0—1.34 Gbits/s or 2.0—2.68 Gbits/s transmission and converts the data to serial format. The serial nonreturn to zero (NRZ) bits are then shifted out of the chip at a maximum rate of 2.68 Gbits/s. Internally, the chip uses two parallel shift registers that operate at half rate (i.e., a maximum of 1.34 GHz) for reduced power consumption. The two shift registers drive the PECL output buffer in an interleaved manner to construct the serial output data stream.

The transmit shift register and other circuits are driven with clocks generated from a 1.0 GHz to 1.34 GHz internal clock. This internal clock is sourced from a voltage-controlled oscillator (VCO) that is locked to the external reference of 100 MHz to 134 MHz. The internal transmit phase-locked loop multiplies the frequency of the input reference clock by a factor of 10, and controls the transmit jitter bandwidth with appropriate design of the jitter transfer function.

Receiver Section

The receiver circuit extracts the clock from the serial input data and retimes the data with the clock. The data are input to the receiver on a differential PECL buffer. External termination resistors are supplied by the user in accordance with *ANSI* standard, X3T11. The serial differential inputs, HDINP and HDINN, are ac coupled to the chip and internally biased to the PECL input common-mode level.

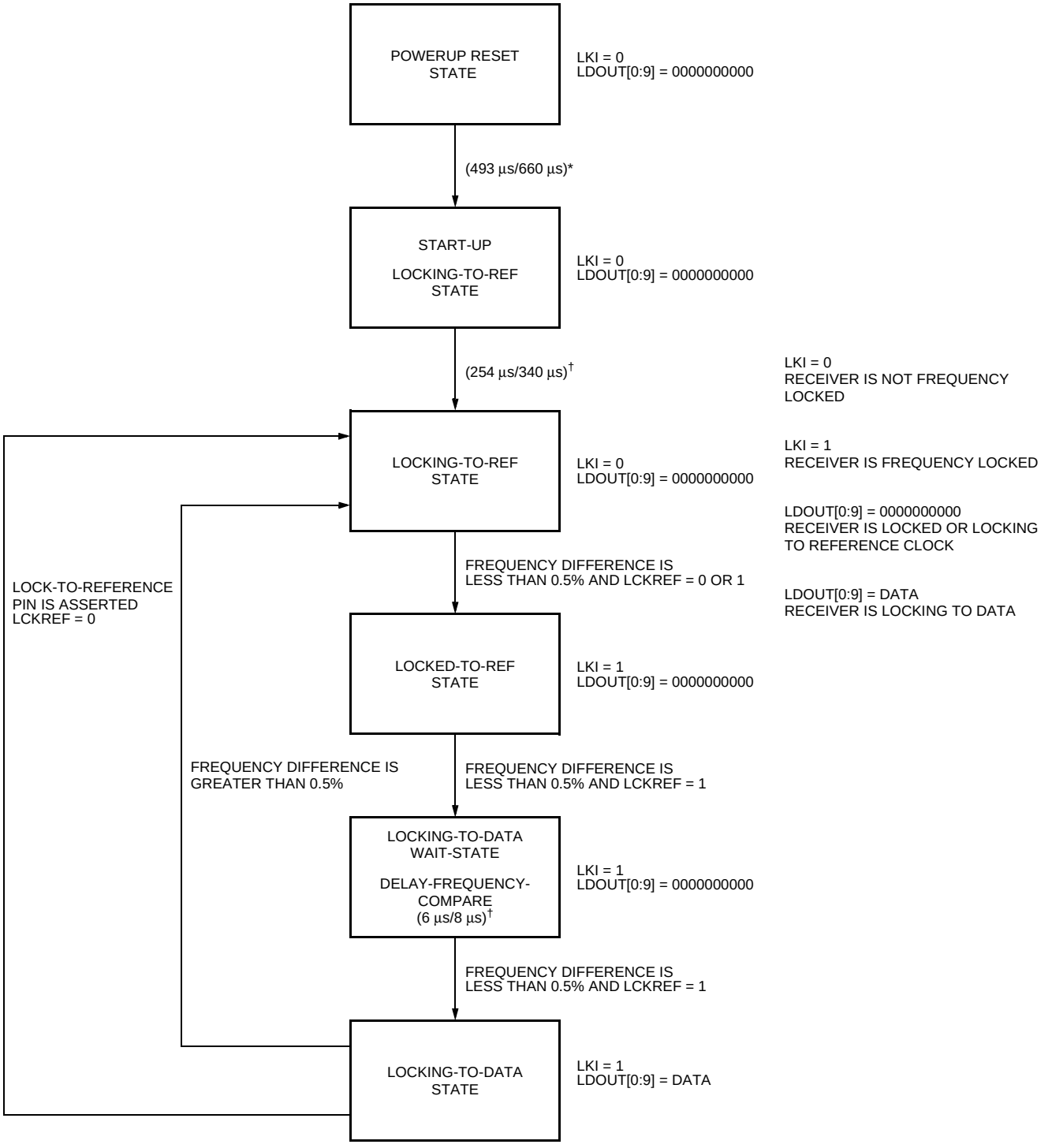
The receive PLL has two modes of operation: lock to reference and lock to data with retiming. When no data or invalid data is present on the HDINP and HDINN pins, the receive VCO will not lock and its frequency can drift outside of the nominal ±100 ppm range. Under this condition, the receive PLL will lock to REFCLK for a fixed time interval and then will reattempt to lock to receive data. The process of attempting to lock to data and then locking to clock will repeat until valid input data exists.

After the on-chip powerup sequence is complete, the receiver will remain in the locked-to-REF state until frequency lock is attained. Frequency lock is defined as the situation in which the divided-by-10 receiver VCO clock frequency is within ±0.5% of the reference clock frequency. Both of these clocks are monitored by a frequency comparator. Once frequency lock is attained, the receiver will begin to accept serial data input and lock to the frequency of that data. See the following state diagram which indicates the state of the frequency lock indicator pin (LKI) and the parallel data output port LDOUT[0:9] during the lock in sequence.

In the lock to data mode, the timing recovery loop compares the phase of the input data with a pseudo-ECL multiplying phase detector. Phase comparison between data and regenerated clock occurs only on the positive-going data edge so that data pulse width distortion will not affect the clock recovery performance. A charge pump then updates the on-chip loop filter and gradually locks the receive clock to the data.

* *ANSI* is a registered trademark of the American Standards Institute, Inc.

Functional Description (continued)



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* The period is dependent on the speed of REFCLK (134 MHz/100 MHz).
Additional requirement: V_{DD} must be ≥ 2.0 V and REFCLK must be active.

† The period is dependent on the speed of REFCLK (134 MHz/100 MHz).

Figure 5. Receiver PLL Lock-In Sequence State Diagram

Functional Description (continued)

The active-high RESET pin resets the chip and can aid in rapid lock-in of the internal PLL circuitry. A chip reset is not necessary for normal operation.

Byte Alignment

When ENBYSYNC = 1, the LU6X31FT recognizes the comma sequence and aligns the 10-bit comma-containing character to the word boundary, bits LDOUT[0:9].

BYTSYNC = 1 when the parallel output character contains a byte-aligned comma-containing character. The BYTSYNC flag will continue to output a logic 1 whenever a byte-aligned comma-containing character is at the parallel output port, independent of ENBYSYNC. When ENBYSYNC = 0, there are two possible scenarios depending upon when the comma sequence is received:

1. If byte alignment had been previously achieved when ENBYSYNC had been a logic 1, the BYTSYNC flag will continue to output a logic 1 whenever a byte aligned comma-containing character is at the parallel output port. If a comma-containing character occurs that is not on the word boundary, no attempt will be made to align this comma character and the BYTSYNC flag will remain at a logic 0.
2. If byte alignment had **not** been previously achieved when ENBYSYNC had been a logic 1, then the first (and only the first) comma-containing character received will be aligned to the word boundary. BYTSYNC will output a logic 1 whenever a comma-containing character is aligned to the word boundary.

Parallel Output Port

Two low data rate receive byte clocks are available as TTL-compatible outputs during use of the parallel output port. RBCCLK1 is the receive byte clock used by the protocol device to register bytes 0 and 2. RBCCLK0 is the receive byte clock used by the protocol device to register bytes 1 and 3, and it is 180 degrees out of phase with RBCCLK1. Both RBCCLK1 and RBCCLK0 can be stretched during byte alignment but not truncated or slivered.

After the powerup-reset sequence, the receive byte clocks (RBCCLK0, RBCCLK1) will become active and remain active. The RBCCLK0 and RBCCLK1 outputs will be synchronous with the REFCLK frequency during the locked-to-ref state. The RBCCLK0 and RBCCLK1 outputs will be synchronous with the serial data input frequency during the locking-to-data state. RBCCLK phase changes will accompany transitions between the locked-to-ref and locking-to-data states, until phase lock is attained. During the switch over from the locked-to-ref state to the locking-to-data state and vice versa, the receive byte clocks will be continuous and there will be no truncation or slivering of these clocks.

Receive Serial Data Signal Detect Function

A signal detect circuit monitors the receive serial data signal HDINP/HDINN. When the peak-to-peak differential input signal drops below VHDINsig-min, the TTL compatible output pin SDN will output a logic-high level (valid data signal level absent). When the peak-to-peak differential input signal increases to larger than VHDINsig-min, the TTL compatible output pin SDN will output a logic-low level (valid data signal present). This output pin can be monitored and/or used to drive the power down input pin PD.

Transmit/Receive Data Rate Selection

The high-speed transmit and receive serial data can operate in the range of 1.0 Gbit/s to 1.34 Gbits/s or 2.0 Gbits/s to 2.68 Gbits/s depending on the state of the DRSTX and DRSRX inputs. The REFCLK frequency is always kept in the range of 100 MHz to 134 MHz.

Loopback Mode Operation

A selector pin (LOOPEN) selects between two possible sets of inputs: normal data (HDINP, HDINN) or internal loopback data. When LOOPEN = 1, HDOUTP = logic 1 and HDOUTN = logic 0. The serial transmit data prior to the PECL output driver is directed to the data recovery circuit, where clock is recovered and data is resynchronized to the recovered clock. Retimed data and clock then go to the serial-to-parallel converter.

Functional Description (continued)

Table 2. Data Rate Selection

DRSRX Input (Receive Data Rate Selection)	DRSTX Input (Transmit Data Rate Selection)	Serial Receive Rate (Gbits/s)	Serial Transmit Rate (Gbits/s)	LDIN[9:0]	LDOUT[9:0]
0	0	1.0 to 1.34	1.0 to 1.34	LDIN[0] bit transmitted first	LDOUT[0] bit received first
0	1	1.0 to 1.34	2.0 to 2.68		
1	0	2.0 to 2.68	1.0 to 1.34	LDIN[0] bit transmitted first	LDOUT[0] bit received first
1	1	2.0 to 2.68	2.0 to 2.68		

Test Modes—For Manufacture Test Only

Note: Test modes are not guaranteed to be operational and may be modified or eliminated without prior notice.

Test Mode 0 (TM0)—Normal Operation

This mode is for normal operation.

Test Mode 1 (TM 1)—High-Speed Serial Loopback

The transmit signal at the serial interface is looped back internally to the receive circuitry. The serial loopback path does **not** include the PECL input buffers. The HDOUTP, HDOUTN outputs are active. The output of the PECL input buffer driven by HDINP, HDINN is ignored.

Data is sourced at the LDIN[9:0] pins and detected at the LDOUT[9:0] pins. All other operation is normal.

Test mode is the same as the operational mode of LOOPEN = 1 with HDOUTP/N active.

Test Mode 2 (TM2)—Immediate PECL I/O Loopback

Data are input via the HDINP and HDINN PECL inputs. The output of this buffer is looped internally to the PECL output buffer, and the data are detected at the HDOUTP and HDOUTN pins.

Test Mode 3 (TM3)—High-Speed Parallel Loopback

Loopback is performed at the parallel bus. The loopback connection is made so that logically:

LDIN[9:0] = LDOUT[9:0]

The LDOUT[9:0] pins remain active. Data are sourced at HDINP, HDINN and detected at HDOUTP, HDOUTN.

Test Mode 4 (TM4)—Transmit Data 0101010101

The LDIN[9:0] pins are bypassed, and internally, the data equivalent to LDIN[9:0] = 0101010101 are sourced. Transmit data is measured at HDOUTP, HDOUTN.

This test mode simplifies data sourcing when the transceiver is embedded in a larger chip and access to the parallel input bus is limited.

Test Mode 5 (TM5)—Transmit Data 0000011111

The LDIN[9:0] pins are bypassed, and internally, the data equivalent to LDIN[9:0] = 0000011111 are sourced. Transmit data are measured at HDOUTP and HDOUTN.

This test mode simplifies data sourcing when the transceiver is embedded in a larger chip and access to the parallel input bus is limited.

Test Modes—For Manufacture Test Only (continued)

Test Mode 6 (TM6)—Transmit/Receive PLL Bypass (Low-Speed)

The outputs of the transmit and receive VCOs are not used in this test mode. A low-speed clock and quadrature clock are applied on the LCKREF input and ENBYSYNC pins. The clock inputs on the LCKREF and ENBYSYNC pins should be 10 times the TBC signal. Data are sourced at the LDIN[9:0] pins and detected at the HDOUTP, HDOUTN outputs for the transmitter. Data are sourced at the HDINP, HDINN pins and detected at the LDOUT[9:0] pins.

Test Mode 7 (TM7)—Transmit/Receive PLL Bypass (Version Identifier to High-Speed Serial Output)

Same as TM6 except that the LDIN[9:0] pins are bypassed and the chip version is encoded as:

LDIN[9:0] = a9a8a7a6a5 a4a3a2a1a0.

Where:

a9a8a7a6a5 a4a3a2a1a0 is the chip identifier.

Note that the transmit data will be permitted to violate the 8B/10B run length limited code in this mode.

Test Mode 8 (TM8)—Immediate Parallel Loopback

Loopback at the low-speed parallel interface is provided such that:

LDOUT[9:0] = LDIN[9:0]

Test Mode 9 (TM9) Chip Version Identifier Sourced to Parallel Bus

This test mode is similar to test mode 7, except the chip version identifier is sent to the LDOUT[9:0] pins. When the test is operating:

LDOUT[9:0] = a9a8a7a6a5 a4a3a2a1a0

Test Mode 10 (TM10)—Receiver Powerdown

In this mode, the input PECL buffer and receive PLL are completely powered down to create a quiet environment for measuring the intrinsic jitter of the transmitter. The LDOUT[9:0] pins will be forced to a logic zero.

Test Mode 11 (TM11)—Receiver Locked to Data

The receive PLL is forced to lock to data, even if the input data frequency is off by more than the ±0.5% threshold normally used to enter the lock to reference mode. This test mode is used to measure the hold range of the receive PLL in data mode.

Test Modes—For Manufacture Test Only (continued)

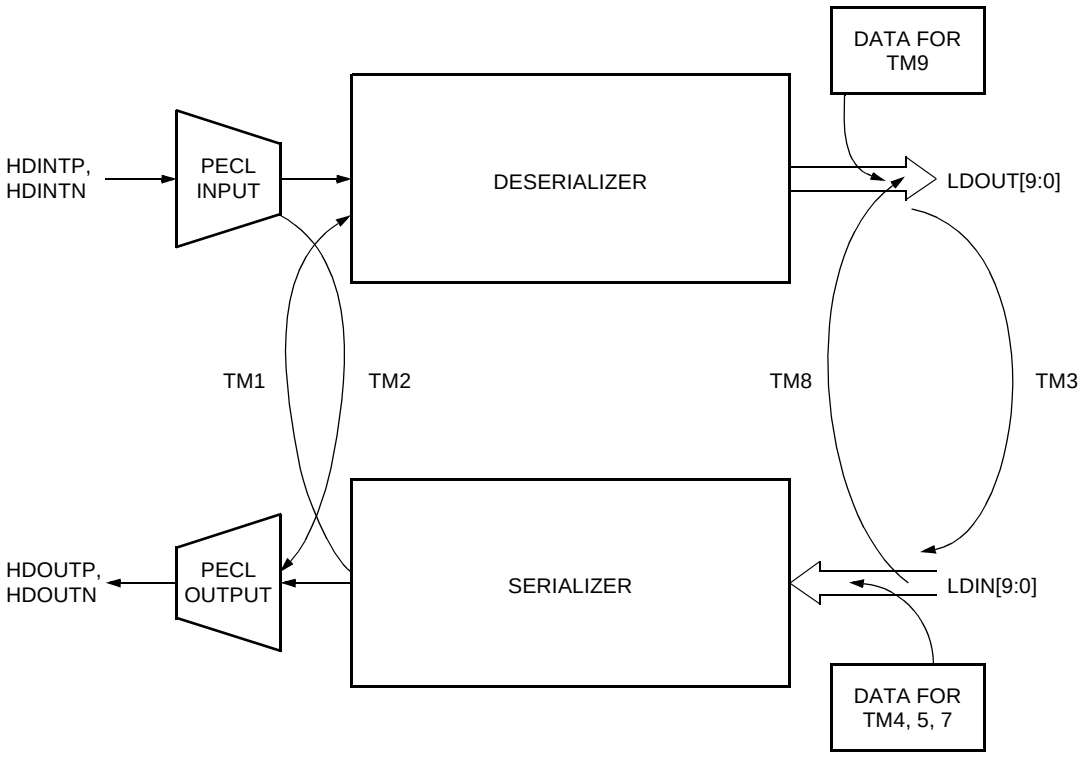

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Figure 6. Test Modes for Looping and Sourcing Data

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

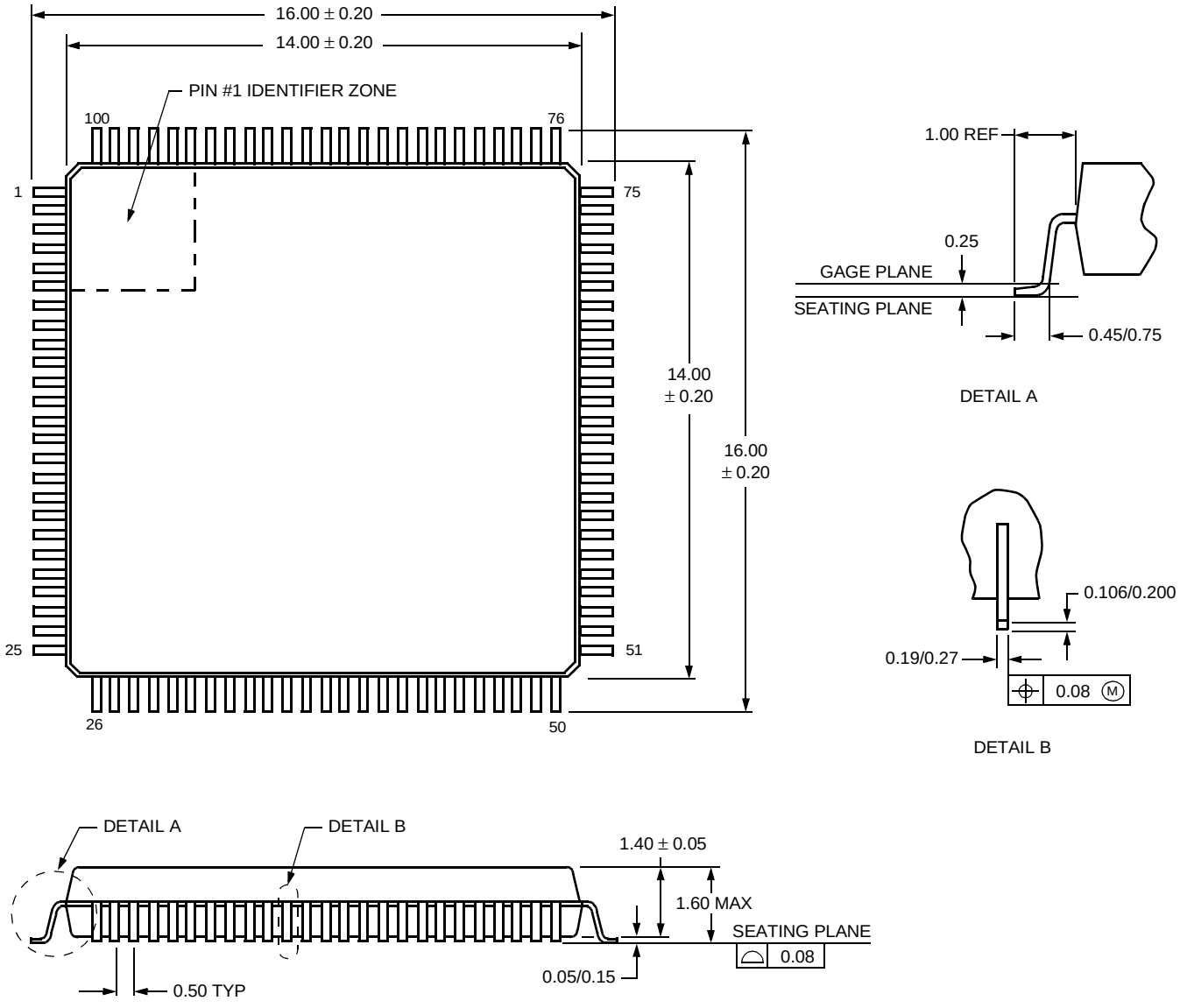
Table 3. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage	3.135	3.465	V
TTL High Input Voltage	3.3	3.6	V
Junction Operating Temperature	0	125	°C
Storage Temperature	–65	150	°C

Outline Diagram

100-Pin TQFP

Dimensions are in millimeters.



Ordering Information

Device Code	Package	Comcode
LU6X31FT	100-Pin TQFP	108560830

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