LXP730

Multi-Rate DSL Framer

Datasheet

The LXP730 is a multi-purpose Digital Subscriber Line (DSL) framer which complements the Level One SK70725/21 Enhanced MDSL Data Pump (EMDP) to provide seamless transport of data and voice signals over one or more DSL datapaths.

Applications

The LXP730 in combination with the EMDP chipset is optimized for use as a framer or I/O interface device for the following applications:

- Digital Pair Gain Systems
- Ethernet Modems
- T1/E1 Fractional Transport Systems
- Videoconferencing Systems
- Simultaneous Data - Voice Transport Systems
- Wireless Base Station Access Systems

Product Features

The LXP730 provides the basic functions required of a DSL framer:

- Synchronization of external data streams to the DSL line
- Multiplexing and demultiplexing of independent data streams for voice and data
- Loopback of payload data at the DSL interface
- Creation, insertion, and recovery of the MDSL Overhead (MOH) structure, performance monitoring, and message transport required in a DSL system with a capacity of up to 32 kbps
- Supports two input/output data streams simultaneously
  - —Slave mode: external clock determines the rate at which data will be transferred to and from the framer
  - —Master mode: clock derived from received DSL clock or external oscillator
- Single part architecture allows one chip to be used economically in both central and remote locations
- Supports systems with point-to-point architectures
- Alternate Hardware Control mode (HWC) for operation without an external microprocessor

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Datasheet

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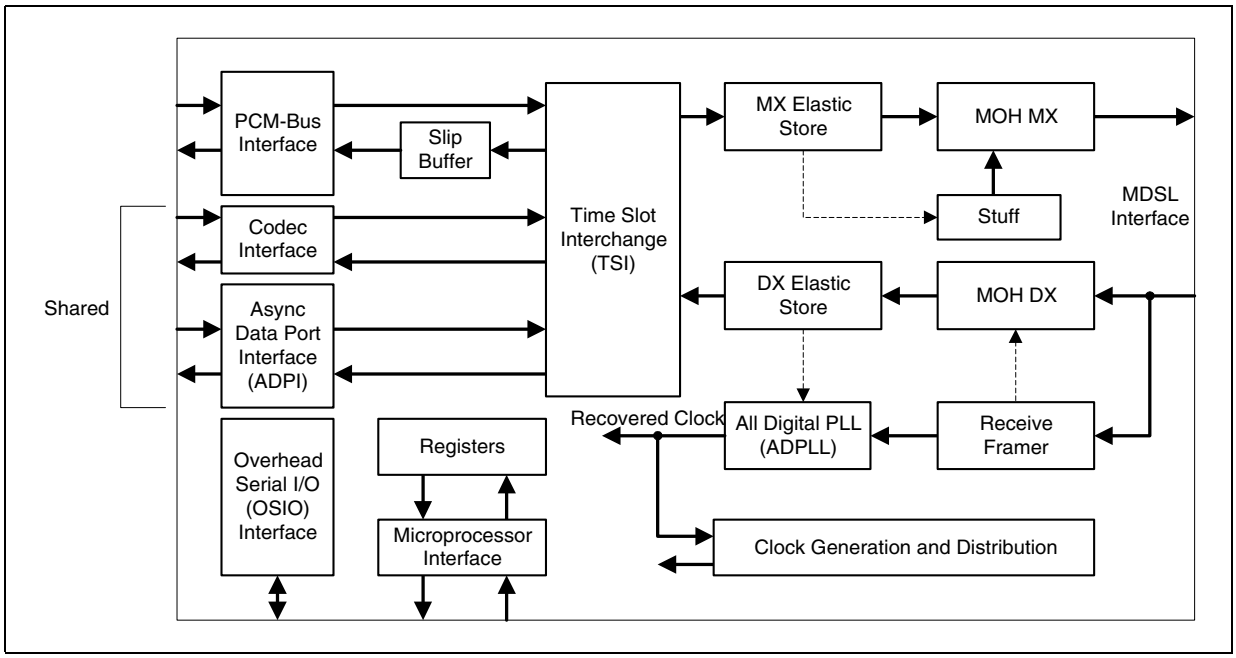
Revision History

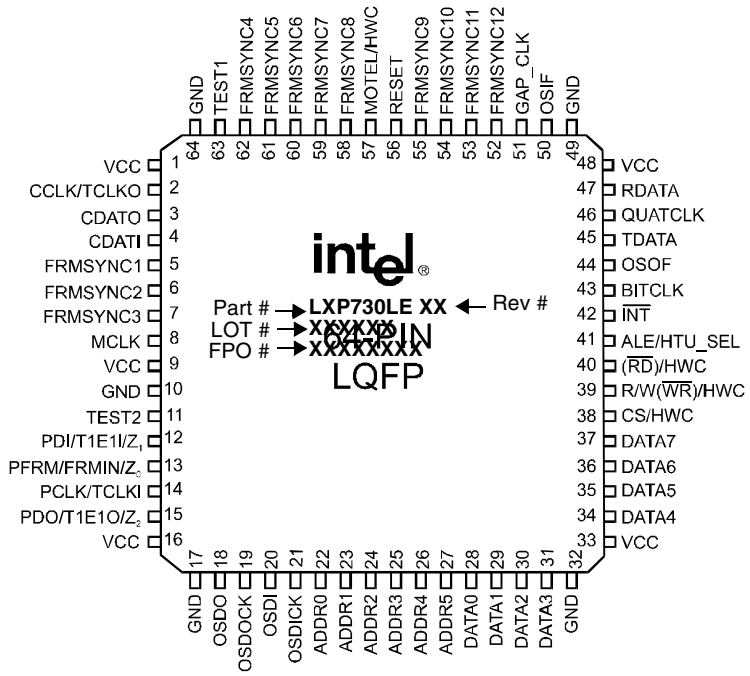
Revision	Date	Description

Figure 1. LXP730 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXP730 Pin Assignments



Package Topside Markings	
Marking	**Definition**
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. LXP730 Pin Descriptions

Pin	Symbol	Type[1]	Description
1, 9, 16, 33, 48	VCC	_	**Power Supply.**
10, 17, 32, 49, 64	GND	_	**Ground.**
28	DATA0/ CRC_ERROR	DI/O, DO	**DATA0.** MPC mode/**CRC_ERROR.** flag HWC mode, indicates an error was detected in the previous frame.
29	DATA1/FEBE	DI/O, DO	**DATA1.** MPC mode/**FEBE.** flag HWC mode, indicates the other side of the DSL link encountered a CRC error.
30	DATA2/ LINK_ACTIVE	DI/O, DO	**DATA2.** MPC mode/**LINK_ACTIVE.** HWC mode, indicates that the DSL link is active and ready to transport data.
31	DATA3/RUN-STOP	DI/O, DI	**DATA3.** MPC mode/**RUN-STOP.** HWC mode, set to low to activate the DSL link, edge triggered input.
34	DATA4/ FRMSYNC15	DI/O, DO	**DATA4.** MPC mode /**FRMSYNC15.** HWC mode, Frame Sync Pulse, channel 15.
35	DATA5/ FRMSYNC16	DI/O, DO	**DATA5.** MPC mode /**FRMSYNC16.** HWC mode. Frame Sync Pulse, channel 16.
36	DATA6/ FRMSYNC17	DI/O, DO	**DATA6.** MPC mode /**FRMSYNC17.** HWC mode. Frame Sync Pulse, channel 17.
37	DATA7/ FRMSYNC18	DI/O, DO	**DATA7.** MPC mode /**FRMSYNC18.** HWC mode. Frame Sync Pulse, channel 17.
22	ADDR0/ FRMSYNC13	DI, DO	**ADDR0.** MPC mode/**FRMSYNC13.** HWC mode. Frame Sync Pulse, channel 13, output.
23	ADDR1/N1	DI	**ADDR1.** MPC mode/**N1.** DSL rate select, HWC mode.
24	ADDR2/N2	DI	**ADDR2.** MPC mode/**N2.** DSL rate select, HWC mode.
25	ADDR3/N3	DI	**ADDR3.** MPC mode/**N3.** DSL rate select, HWC mode.
26	ADDR4/N4	DI	**ADDR4.** MPC mode/**N4.** DSL rate select, HWC mode.
27	ADDR5/ FRMSYNC14	DI, DO	**ADDR5.** MPC mode**/FRMSYNC14.** Frame Sync Pulse, channel 14, output, HWC mode.
57	MOTEL/HWC	DI	**MOTEL/HWC.** Set high for Motorola mode, set low for Intel mode, Micro Processor Control (MPC) mode, input **/HWC.** pull high for HWC mode, input.
39	R/W($\overline{WR}$)/HWC select	DI	**R/W($\overline{WR}$).** R/W for Motorola interface, $\overline{WR}$ for Intel interface /HWC select, set low for HWC mode.
40	($\overline{RD}$)/HWC select	DI	**($\overline{RD}$).** Unused for Motorola interface, $\overline{RD}$ for Intel interface /HWC select, set low for HWC mode.
38	CS /HWC select	DI	**$\overline{CS}$.** Chip select, HWC select, set low for HWC mode.
41	ALE/HTU_SEL	DI	**ALE.** Address latch enable for Intel interface, MPC mode, input **/HTU_SEL.** HTUC/ HTUR select, High for HTUC, Low for HTUR, HWC mode, input.

1. AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; NC = No Clamp. Pad will not clamp input in the absence of power; PU = Input contains pull-up; PD = Input contains pull-down; I/O = Input/Output; OD = Open Drain Output;
TO = Tri-State Output.

Table 1. LXP730 Pin Descriptions (Continued)

Pin	Symbol	Type[1]	Description
42	$\overline{\text{INT}}$	DO	**$\overline{\text{INT}}$.** Interrupt output. Programmed by setting bits in the INT_EN register.
56	RESET	DI	**$\overline{\text{RESET}}$.** Active low input. All registers revert to their default values.
8	MCLK	DI	**MCLK.** Master Clock.
4	CDATI	DI	**CDATI.** Codec Data In.
3	CDATO	TO	**CDATO.** Codec Data Out, Tri-state.
2	CCLK/TCLKO	TO	**CCLK.** Codec Clock, Nominal 2.048 MHz, tri-state. /**TCLKO.** Transport Clock for T1/E1: 1.544 MHz or 2.048 MHz clock derived from line rate.
5	FRMSYNC1/ FRMOUT	DO	**FRMSYNC1.** Frame Sync Pulse, channel 1, output. /FRMOUT. Frame Out, for T1/E1 application, output.
6	FRMSYNC2	DO	**FRMSYNC2.** Frame Sync Pulse, channel 2, output.
7	FRMSYNC3	DO	**FRMSYNC3.** Frame Sync Pulse, channel 3, output.
62	FRMSYNC4	DO	**FRMSYNC4.** Frame Sync Pulse, channel 4, output.
61	FRMSYNC5	DO	**FRMSYNC5.** Frame Sync Pulse, channel 5, output.
60	FRMSYNC6	DO	**FRMSYNC6.** Frame Sync Pulse, channel 6, output.
59	FRMSYNC7/ SDOCK	DO	**FRMSYNC7.** Frame Sync Pulse, channel 7, output. **/SDOCK.** Serial Data Out Clock, ADPI serial mode, output.
58	FRMSYNC8/ SDO	DO	**FRMSYNC8.** Frame Sync Pulse, channel 8, output. **/SDO.** Serial Data Out, ADPI serial mode, output.
55	FRMSYNC9 SDICK	DO	**FRMSYNC9.** Frame Sync Pulse, channel 9, output. **/SDICK.** Serial Data In Clock, ADPI serial mode, output.
54	FRMSYNC10/ SDI	DO, DI	**FRMSYNC10.** Frame Sync Pulse, channel 10, output. /**SDI.** Serial Data In, ADPI serial mode, input.
53	FRMSYNC11	DO	**FRMSYNC11.** Frame Sync Pulse, channel 11, output.
52	FRMSYNC12/ PDOE	DO	**FRMSYNC12.** Frame Sync Pulse, channel 12, output. /**PDOE.** PCM Data Output Enable, control for external PCM interface buffer, output. Enabled by bit-3 of Register 23h.
51	GAP_CLK	DO	**GAP_CLK.** Gapped Clock, N x 64 kHz recovered from DSL for optional external ADPLL, output. Output is high when option not selected.
63	TEST1	DI	**TEST1.** Factory Test Pin 1, input; should be tied to GND.
11	TEST2	DI	**TEST2.** Factory Test Pin 2, input; should be tied to VCC.
21	OSDICK	DO	**OSDCKI.** Overhead Serial Data In Clock, output.
20	OSDI	PU	**OSDI.** Overhead Serial Data In, input.
19	OSDOCK	DO	**OSDOCK.** Overhead Serial Data Out Clock, output.
18	OSDO	DO	**OSDO.** Overhead Serial Data Out, output.

1. AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; NC = No Clamp. Pad will not clamp input in the absence of power; PU = Input contains pull-up; PD = Input contains pull-down; I/O = Input/Output; OD = Open Drain Output;
TO = Tri-State Output.

Table 1. LXP730 Pin Descriptions (Continued)

Pin	Symbol	Type[1]	Description
44	OSOF	DO	**OSOF.** Overhead Serial Output Flag, output. Indicates the first bit of OSIO output frame.
50	OSIF	DO	**OSIF.** Overhead Serial Input Flag, output. Indicates the first bit of OSIO input frame.
45	TDATA	DO	**TDATA.** Transmit Data, output. Connect to SK70725.
47	RDATA	DI	**RDATA.** Receive Data, input. Connect to SK70725.
46	QUATCLK	DI	**QUATCLK.** Quaternary alignment Clock, input. Connect to SK70725.
43	BITCLK	DI	**BITCLK.** Bit Clock, input. Connect to SK70725.
13	PFRM / FRMIN / Z_0	DI,DO,DI	**PFRM.** PCM frame pulse: input for PCM slave, output for PCM master. Alignment signal for the first time slot for both PDI and PDO. /FRMIN. Frame In, for T1/E1 application, input. /Z_o. Bit zero of the 3-bit word used to specify the number of Z bits in the Hardware mode, input.
12	PDI / T1E1I / Z_1	PU,DI, DI	**PDI.** PCM Data In, input. **/T1E1I.** T1 or E1 Input data, input. /**Z_1.** Bit one of the 3-bit word used to specify the number of Z bits in the Hardware mode, input.
15	PDO / T1E1O / Z_2	TO,TO,DI	**PDO.** PCM Data Out, tri-stateable output. **/T1E1O.** T1 or E1 Output data, tri-stateable output. /**Z_2.** Bit two of the 3-bit word used to specify the number of Z bits in the Hardware mode, input.
14	PCLK/TCLKI	DI/O	**PCLK.** PCM clock: input for PCM slave, output for PCM master. **/TCLKI.** Transport Clock In, for T1/E1 application, 1.544MHZ - T1, 2.048MHz - E1, input.

1. AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; NC = No Clamp. Pad will not clamp input in the absence of power; PU = Input contains pull-up; PD = Input contains pull-down; I/O = Input/Output; OD = Open Drain Output;
TO = Tri-State Output.

2.0 Functional Description

2.1 LXP730 Nx64 Framer

The LXP730 is designed to multiplex/demultiplex two payload sources to/from a DSL stream, and add/recover overhead data for link control. Several popular interfaces are provided to support a variety of applications.

The two major categories of payload supported are synchronous (i.e. voice-frequency data - PCM) and asynchronous (i.e. digital data - Packet/Cell). The LXP730 supports *N*x64 kbps channels in the DSL with *N* = 4 to 18. The LXP730 consists of the following functional blocks as shown on page 1:

- Time Slot Interchange (TSI)
- PCM-Bus Interface
- Codec Interface
- T1/E1 Interface
- Asynchronous Data Port Interface (ADPI)
- Microprocessor Interface
- Overhead Serial I/O (OSIO) Interface
- SK70725/SK70721 (MDSL) Interface
- All Digital PLL (ADPLL)
- Clock Generation and Distribution

The terms Local and Remote are used in this document to designate the two ends of a DSL link. The Local is usually the master in that it initiates the link startup and can control the actions and configuration of the Remote. There are several equivalent nomenclatures in the Telecom industry. Some of these are, respectively: CO and CPE, or HTU-C and HTU-R, or LTU and NTU.

The following is a description of the LXP730 functional blocks.

2.2 Time Slot Interchange (TSI)

The Time Slot Interchange (TSI) is the central module of the LXP730 Nx64 framer. The TSI maps payload to the available DSL N-channels for transport across the loop.

The TSI uses register settings to select time slots to map into the N MDSL channels. The total number of available payload channels is *N* and is set by the N_MDSL register (00h), with selected valid values from 4 to 18. Each of the 18 Nx registers (01h -012h) is used to select the payload source, and if applicable, the PCM time slot assigned to the register's corresponding MDSL channel.

In the MX direction (from the TSI to the MDSL Interface), the TSI multiplexes the payload sources into the MX elastic store (MX ES). The payload and overhead are multiplexed into the DSL stream for loop transport.

In the DX direction (from the MSDL Interface to the TSI), the TSI reads from the DX elastic store (DX ES) and demultiplexes the loop data into its payload data sources.

Synchronous payload sources are typically 8-bit serial time slots, cascaded together with each source repeating every 125 µsec (i.e. 8 kHz). A framing pulse, separate from the data signal, signifies the start of a frame. A 2.048 Mbps data stream has 32 time slot sources, while a 1.544 Mbps data stream has 24 time slot sources plus one extra bit for framing.

When the PCM or codec interfaces are running, the framing pulses are used by the TSI to initialize operation to the MX ES. The MX ES and DX ES have triple buffering schemes that prevent the loss of data. The PCM/codec interfaces typically produce high speed data bursts while the MDSL interface runs at a slower though irregular rate.

Asynchronous data is typically a sequence of bytes which have no explicit timing relationship between them. Asynchronous Data Port Interface (ADPI) bytes may be inserted into payload slots that are not carrying PCM data. ADPI bytes are inserted into the DSL stream in the order they are received from the interface.

Channel blocking on a MDSL channel is achieved by setting the CH_CFG bits in the Nx register to 01. The transported value for that MDSL channel will be the one stored in the IDLE register.

The TSI uses the MCLK clock to synchronize to the various interfaces. The MCLK frequency must be at least three times the highest interface clock frequency for the TSI to function properly. There are other considerations to select the operating frequency of MCLK when using the internal ADPLL.

2.3 PCM-Bus Interface

The LXP730 provides a generic interface for common PCM-bus configurations and can either be master or slave to these PCM busses. Some of the key features that allow flexibility are:

- Clock at 1x or 2x the data rate
- Programmable number of bytes per frame; 8, 16, 32, 64
- Programmable clock and frame pulse polarities

These features allow interfacing to standard PCM styles such as: ST, IOM, IOM2 (see Figure 9 for circuit) and CHI. The data rates can range from 256 kbps to 4096 kbps. The clock rates can range from 256 kHz to 8196 kHz.

The range of permissible PCM time slots are 0 to 31 for a 2.048 Mbps backplane and 0 to 63 for a 4.096 Mbps backplane for a total number of time slots up to the maximum number N. PCM time slots must be assigned in ascending order to MDSL channels. The value set in the TS-bits in the Nx registers select the PCM timeslot to go into the xth MDSL channel.

There is a limitation of the disparity allowed between the PCM clock and the BIT_CLK. For N = 4, the PCM bit rate cannot exceed 2 Mbps. To use a 4 Mbps PCM interface the NMDSL setting must be at least 6 channels.

On these busses, the input and output data streams are synchronized to the same clock. A slip buffer is present on the receive side to accommodate the differences in the PCM clock frequencies of the two ends of the MDSL line.

The slip buffer is two frame lengths long. The buffer will empty if the PCM clock is reading data out of the slip buffer faster than the TSI is writing into it. When the last bit for the frame has been read and there is not another byte from the next frame to clock out, the read pointer is set back to the beginning of the current frame and repeated. The other slip situation occurs when the TSI is writing data faster than the PCM is clocking it out. When the write pointer gets close to the read pointer that hasn't finished a frame, then the read pointer is allowed to finish the current frame and then is advanced to skip the next frame.

The slip buffer may be bypassed by setting the SBBP bit, (bit 0, in the PCM_CFG1, register). Slip occurrences are detected and signalled in the Interrupt Status register.

Normally the LXP730 PCM bus is configured as a slave in the Local unit, while the Remote LXP730 PCM bus can be either configured as slave or master off the PCM bus. When the Remote LXP730 is in PCM slave mode, the slip buffers accommodate the differences in the two PCM clocks. When the Remote LXP730 is in PCM master mode, the PCM clock and frame pulse are derived from the receive DSL clock using the internal ADPLL to provide loop timing to prevent the slip action from occurring.

The PCM bus timeslot assignments to the DSL channels may be altered while the DSL link is active. The Nx registers can be changed without interfering with other Nx registers and the effect of their settings.

The PDO pin is tri-stated except during programmed time slots.

The PFRM pulse defines the start of a PCM frame. The number of PCM time slots per frame is variable from 4 to 64. This is programmed by setting the six MAXPCHN bits in, the PCM_CFG2 register, with the value n-1 number time slots.

PCM selection for a MDSL channel is accomplished by setting the CH_CFG bits in the Nx register to '10' (binary).

2.4 Codec Interface

The LXP730 primarily supports the COMBO codec I style devices. The LXP730 codec interface is programmable to allow the use of other codec type devices that require a positive frame pulse. The LXP730 provides a separate set of pins for this interface allowing simultaneous operation with a PCM bus with the following characteristics:

- Short frame positive sync pulse
- Clock at 1x or 2x the data rate
- Programmable number of bytes per frame in MPC; 8, 16, 32, 64

The data rates can range from 256 kbps to 4096 kbps. The clock rates can range from 256 kHz to 8196 kHz. Under HWC mode, the number of bytes per frame is limited to 32.

The input and output data from the TSI are connected to the codec CDATI and CDATO pins for the appropriate time slot. The CDATO pin is tri-stated except during programmed time slots. Only twelve (12) codecs are supported in the MPC mode.

The LXP730 is always the master on the codec bus. The LXP730 can be configured to derive the clock and frame pulse from either MCLK (in codec Master mode) or from the DSL clock using the internal ADPLL (in codec Slave mode). One LXP730 of the DSL link must be in the Master codec mode and the other in the Slave codec mode.

The LXP730 generates the codec clock and the framing pulses for eighteen (18) codecs from the selected reference. Selecting codec timeslot 0 in an Nx register corresponds to FRMSYNC1, 1 to FRMSYNC2, etc. In HWC mode, the FRMSYNC pins are automatically assigned with the programming of the Nx pins. The number of codec time slots per frame is variable from 4 to 64. This is programmed by setting the six MAXCCHN bits in the COD_CFG register (22h) with the value n-1 number time slots.

Codec selection for a MDSL channel is accomplished by setting the CH_CFG bits in the Nx register to '00' (binary).

2.5 T1/E1 Interface

The LXP730 supports T1/E1 framer interfaces by using a hybrid of the PCM and codec interfaces to transport pleisiochronous data.

The PCM interface is used in its slave mode to connect a T1/E1 framer and its TxData (T1E1O), RxData (T1E1I), RxCLK (TCLKI) and FramePulseOut (FRMIN). The slip buffer must be in the bypass mode.

The codec interface is used in its slave mode to derive the FramePulseIn (FRMOUT) and TxCLK (TCLKO) to the T1/E1 framer. The derived T1/E1 FRMOUT tracks the MDSL frame rate from the DSL, and in cases where framing is lost, the DX tracking circuits slowly reacquire to prevent a drastic change in the output frame frequency.

The PCM and codec sections must each be configured through registers to handle the T1/E1 pleisiochronous data.

For T1, only *N*=12 or fractional T1 is supported. In T1, the only workable value for the PCM_CFG2 register is 98h. The MX T1 F-bits must be part of the data stream coming from the external T1 framer. The 12 unused DX T1 time slots are filled with the value programmed in the IDLE register if the TFI bit (bit 0) is set to 0.

Key features of the T1E1 interface are:

- Framer interfaces: DS2141and DS2143
- Data rates: 1544 and 2048 kbps
- Clock rates: 1544 and 2048 kHz

2.6 Asynchronous Data Port Interface (ADPI)

The LXP730 supports a serial method for the Asynchronous Data Port Interface (ADPI). The ADPI is available only in the MPC operating mode. MDSL channels are programmed for ADPI by setting the CH_CFG bits to '11' (binary) in the desired Nx register. The operation of the ADPI is mutually exclusive with the LXP730 codec frame sync pins (FRMSYNC7-10).

The serial ADPI mode provides separate pins for data in, data out, clock-in and clock-out. This is compatible with the bit operation protocol (BOP) for HDLC devices. The LXP730 controls both of the clocks, and therefore, the data flow. The LXP730 moves the bits in and out in 8-bit groups. The maximum clock rate for the bit-to-bit transfer is set by the SAPCLKDIV bits in the FIFO_MISC register. This allows the clocks to run at MCLK ÷ 2 or slower. The groups of clock pulses will be gapped due to the availability of bit positions in the DSL data stream.

2.7 Overhead Interface

The LXP730 provides two options for the interface to insert and receive overhead data for the link: via an external serial interface or through the microprocessor register interface. The data can either be user defined or partially predefined as described in "MDSL Overhead Definition" on page 23. The overhead channel is used for signalling, status flags, loopback control, and diagnostic messaging between the Local and Remote ends of a MDSL link. The LXP730 provides the transparent channel for the overhead data and does not interpret the protocol operation.

The F-bits in the fractional T1 mode are not part of the overhead.

2.7.1 Overhead Serial I/O (OSIO)

The OSIO interface is the default overhead access for both the MPC and HWC operational modes. The serial interface provides six separate pins for data in (OSDI), data out (OSDO), clock-in (OSDICK) clock-out (OSDOCK), start flag in (OSIF), and start flag out (OSOF). The use of the first four pins is compatible with the bit operation protocol (BOP) for HDLC devices. The two flag pins (OSIF and OSOF) provide indications of the start of a MDSL frame and may used with custom overhead handling devices. The flag signals are coincident with the first overhead bit in the MDSL frame.

The LXP730 controls both of the clocks, and thus, the data flow. The clocks will be gapped due to the availability of bit positions in the DSL data stream. The OSIO may be disabled in the MPC mode by setting the Par/Ser bit in the OVRHD_SEL register (24h). OSIF and OSOF will continue to operate.

The defined bits (except the indc_r bit) go to the microprocessor interface registers. The undefined bits (plus the indc_r bit) go to the OSIO interface. This allows a separate transport for HDLC devices while maintaining DSL performance monitoring.

2.7.2 MDSL Overhead Microprocessor Interface

The MDSL overhead microprocessor interface mode uses internal registers to provide the access to insert and receive overhead data for the link. The Par/Ser bit must be set to access the contents of the overhead and Z bit registers. Interrupts may be used to synchronize the contents with the MDSL link. The data can either be user defined or partially predefined as described in "MDSL Overhead Definition" on page 23. Microprocessor writes to defined bits have no effect, with the exception of the indc_r bit.

The registers for the OH and Z bits are double buffered for both the MX and DX sections. When the OHMX bit is set in the INT_STAT, 3Fh, register, the values in the user assessable MX registers are latched into an internal set of registers, and then serially shift throughout the frame. The user has a nominal 6 ms to update the MX registers before they are latched again for transport. Likewise, the DX registers hold their values until the OHDX bit is set, then the overhead data from the latest frame is available. The user again has a nominal 6 ms to read the DX data before it is over written.

2.8 MDSL Interface

Each LXP730 device works directly with one SK70725/21 data pump chip set. The SK70725/21 chip set must be in Mode 0 to work with the LXP730. Refer to the SK70725/21 data sheet for details.

The LXP730 provides TDATA to the data pump and accepts QUATCLK, BITCLK and RDATA signals from the data pump. The framer supports line data rates from 272 kbps to 1168 kbps. Table 2 shows some of the common even-numbered transport, nominal line rates and the number of bits per frame. Odd numbered N values may also be used.

The first value in the Bits/Frame column is the number of bits in an unstuffed frame, and the second value is with stuffing. MDSL Frame periods are a nominal 6 ms regardless of the nominal line rate.

Table 2. Common Transport & Line Rates

Data Rate (kbps)	Nominal Line Rate (kbps)	64 kbps Channels (N)	Bits/Frame
256	272	4	1630/1634
384	400	6	2398/2402
512	528	8	3166/3170
640	656	10	3934/3938
768	784	12	4702/4706
1152	1168	18	7006/7010

The line rate is calculated as *N* x 64 kbps + 16 kbps, where *N* is the number of 64 kbps channels to be transported. The 16 kbps is the total overhead provided by the MDSL transport system.

The 16 kbps holds true as long there is one Z bit per block as described in "MDSL Frame Format" on page 25. The LXP730 supports up to eight Z bits per block, but when greater than one, the overhead rate increases. This causes the line rate to increase accordingly. The equation to calculate the DSL line rate is as follows:

Line rate (kbps) = 8[Z + 1 + (N x 8)]

The LXP730 will scramble payload data, but pass the sync word in the clear. In the Local mode, the LXP730 uses the following scrambling polynomial:

$x^{-23} + x^{-5} + 1$,

In the Remote mode the scrambling polynomial is:

$x^{-23} + x^{-18} + 1$.

In transparent mode, the LXP730 uses the quat alignment signal (QUATCLK) from the data pump to align the sign and magnitude bits in both the transmit and receive directions.

The overhead bits are described in "MDSL Overhead Definition" on page 23.

Before routing the data to the descrambler, the LXP730 will invert the sign bits of the received data stream, if the detected frame sync word has inverted sign bits.

The MDSL interface provides loopback of TDATA, bypassing the external RDATA. Loopback is activated by setting the DSL_LB bit in the OVRHD_CFG register (24h). This routes the 64 kbps channels and MDSL Overhead (MOH) from the MX section to the DX section. When using an external loopback configuration, such as FELB in the SK70725, it is necessary to switch the DX de-scrambling polynomial to the MX polynomial. The descrambling polynomial is inverted by setting the REMOTE_LB bit of the FIFO_MISC register (17h). The BITCLK and QUATCLK control the transfer of data from the MX to the DX section.

2.9 All Digital PLL (ADPLL)

The LXP730 ADPLL is necessary for clock recovery and to control output jitter and wander produced in the DSL environment.

The ADPLL uses MCLK to drive the NCO circuitry, while the reference frequency comes from the received DSL frame rate that has a nominal 6 ms period.

2.9.1 ADPLL Performance: The Selection of K_{loop}

The performance of the ADPLL is user programmable via a register. As shown in Table 3, the 5-bit value, K_{loop}, in PLLCTL3 register controls the lock time and the bandwidth of the ADPLL. The lock time is the amount of time required for the ADPLL to acquire and synchronize to the input MDSL signal. The bandwidth of the ADPLL determines the jitter rejection characteristics of the ADPLL. The bandwidth and lock time are inversely related: $BW = 3/T_{lock}$.

Table 3. K_{loop} Values

Register Bits	Kloop_Value
00000	PLL freeze
00001	2^{0}
00010	2^{-1}
00011	2^{-2}
00100	2^{-3}
...	...
11111	2^{-30}

Kloop is a 5 bit control field found in register PLLCTL3 (address 1D hex, 29 dec). The register bits are used to select a constant (Kloop_Value) that controls the loop bandwidth.

The Bandwidth of the loop filter is determined from the selected Kloop_Value and the frequency of MCLK. Loop bandwidth (BW) is calculated as follows:

$$BW\ (3db) = Kloop\_Value \times MCLK \times 3.89e\text{-}5\ Hz$$

2.9.2 ADPLL Center Frequency: The computation of CFREQ

The center frequency of the ADPLL is set by an 18-bit unsigned fractional number, CFREQ(17:0). This value is programmed in PLLCTL1, PLLCTL2, and PLLCTL3. CFREQ(17:0) is the ratio of the Numerically Controlled Oscillator (NCO) and MCLK, and is shown below. The 2^{18} is the normalizing factor to express it in integer notation. It must then be converted to hexadecimal to load into the CFREQ register.

The output of the NCO is divided by 2 before being provided to the clock multiplex circuitry and the optional PROG_DIV block. This must be taken into account when deciding upon the frequency for the NCO.

The NCO/MCLK ratio should be set to a value greater than or equal to 0.5 but less than 0.98. This ensures that there will be the maximum number of bits of accuracy for the NCO to generate the frequency. The ratio of 0.5 normalized with 2^{18} is 131072 or in hexadecimal, 20000h. This is the smallest recommended value.

Equation 1. Calculation of CFREQ

$$CFREQ = ROUND\left[\frac{(NCOFREQ \times 2^{18})}{MCLK}\right]$$

Table 4 list values for: CFREQ(17:0), Programmable Divider, and NCO frequency for a MCLK of 16.384MHz in several configurations.

2.10 Clock Generation and Distribution

The LXP730 has a flexible clock generation circuit as shown in Figure 3. The clocks for the PCM and codec interfaces can be an independent external input, a division of MCLK, a division of the ADPLL output, or the ADPLL output as selected by the PCM Configuration 1 register (PCM_CFG1) and the Codec Configuration register (COD_CFG).

The PCM port is considered to be in slave mode when its clock source is the external pin. The PCM frame pulse is also sourced from its external PFRM pin when the clock is configured as such. The PCM port is in master mode for the other three settings. The PCM frame pulse is derived from the internal PCLK and driven out on the PFRM pin.

The codec port initially has the CCLK pin tristated until it is configured as an output by setting the CCLK_OE bit in the MISC_CTL register. It is never an input. The external source for the codec clock is the PCLK pin. This allows simultaneous use of the PCM and codec interfaces with the PCM bus providing the clock and allowing MCLK to be some other frequency that may not be suitable to divide down for the codecs.

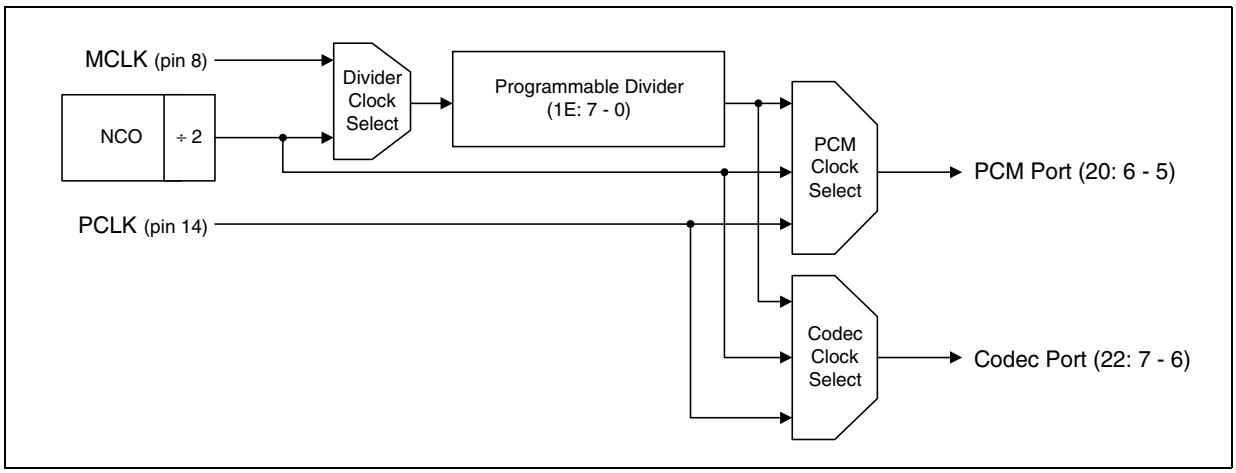
The ADPI clock is not derived from the circuit shown in Figure 3, but rather comes from the TSI module. The TSI keeps track of opportunities to transmit bytes into the DSL frame and creates a burst of eight pulses to clock a byte of data to insert in the MX direction. The TSI unloads data from the DX DSL direction and also creates a burst of eight pulses to clock a byte of data to the external device connected to the ADPI interface.

The burst frequency of the ADPI clocks is derived from MCLK and can be adjusted by the SAPCLKDIV (bits 6 & 7, in register 17h, FIFO_MISC).

Table 4. Typical ADPLL Register Settings, MCLK = 16.384MHz

PCMCLK Output (MHz)	#B PCM	#B DSL	NCO Frequency (MHz)	PROG_ DIV	NCOFREQ/ MCLK	CFREQ(17:0)
1.544	24	12	PCMCLK × 8	4	0.754	0x30400
2.048	32	18	PCMCLK × 4	2	0.5	0x20000
1.152	18	18	PCMCLK × 8	4	0.5625	0x24000
0.896	14	14	PCMCLK × 16	8	0.875	0x38000
0.768	12	12	PCMCLK × 16	8	0.75	0x30000
0.256	4	4	PCMCLK × 32	16	0.5	0x20000

Figure 3. Clock Generation and Distribution



2.11 Modes of Operation

2.11.1 Microprocessor Control (MPC) Mode

The Microprocessor Control (MPC) mode provides access for a microprocessor to configure and control the operation of the framer. The LXP730 provides an 8-bit data bus for the purpose of reading and writing internal registers. The registers are used to configure framer settings, to read and write the MDSL Overhead bits and to configure interrupts and other run-time operational functions.

The microprocessor access circuits support both MOTEL (MOTorola/IntEL) microprocessor interfaces. A chip select signal activates the interface between the device and the microprocessor. In the Motorola mode, the LXP730 supports the R/W and $\overline{CS}$ signals. The Motorola signal $\overline{DS}$ is not used in this mode. In the Intel mode, the LXP730 supports the $\overline{CS}$, ALE, $\overline{WR}$ and $\overline{RD}$ signals. In the Intel mode, the data pins conform to the Intel style Address/Data (AD) functionality. The

address is presented to the AD pins and internally latched with ALE, then the data is either read from or written to the device. ALE may be held high for non-multiplexed address and data operation in the Intel mode for use of the $\overline{WR}$ and $\overline{RD}$ signals.

One interrupt pin is provided. Registers are provided for enabling/disabling the interrupts and monitoring the status of the interrupt signals.

In the MPC mode, both the PCM and Codec/Data Port interfaces may be used simultaneously. The assignment of the 64 kbps timeslots from the interfaces to the DSL is controlled by the TSI (Time Slot Interchange) block. This feature allows data from two different sources to be transported over the DSL.

2.11.2 Hardware Control (HWC) Mode

This mode provides an operational method to run only the codec and OSIO interface without a microprocessor. Pins are provided to select the number (N) of 64 kbps channels to be transported. The following Error/Status flags output pins are provided: LINK_ACTIVE, CRC_ERR and FEBE. $\overline{RESET}$, HTUC/HUTR and RUN-STOP control signals (input pins) are provided.

These pins are shared with the microprocessor mode pins. The HWC mode is selected by pulling the $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and ALE pins Low and the MOTEL pin High.

Only the codec and OSIO interfaces are accessible in the HWC mode. The first *N* codec frame sync pins are active in sequence from 1 to N. As shown in Table 5, pins N1 through N4 are used to select the quantity of codecs supported and to select the proper MDSL frame format. The N0 pin is not used since *N* is always an even number in the HWC mode. The codec interface runs only at the 2.048 MHz 1x clock in the HWC mode.

Table 5. Pin settings for HWC DSL Line Rates

Number of MDSL Channels	Pin			
	N4	N3	N2	N1
4	0	0	0	1
6	0	0	1	0
8	0	0	1	1
10	0	1	0	0
12	0	1	0	1
18	1	0	0	0

2.12 MDSL Overhead Definition

The MDSL overhead bits do not carry any payload values but are used for exchanging messaging and signalling information between the two ends of the DSL link. The overhead bits are divided into two categories; OH and Z bits.

The OH bits are defined in both the ETSI ERT/ETS-152 and ANSI T1E1.4/94-006 standards. These usually have specific definitions. In the LXP730, the OH bits may be partially defined, according to the standards, or totally user definable which is referred to as transparent mode.

The LXP730 supports DSL OH bits in four modes:

- Transparent and register accessible.
- Transparent and OSIO accessible.
- Partially Predefined and register accessible.
- Partially Predefined and OSIO accessible.

The reset default overhead mode is number 4. The modes are selected by setting bits 7 and 6 of register 24h, OVRHD_CFG.

In the HWC mode some of the pre-defined bits' status is routed to external status pins, i.e. CRC_ERROR, FEBE, LINK_ACTIVE.

2.12.1 Predefined Overhead

Pre-defined bit-fields support: frame sync word, stuff-bits, *los*, *CRC-6*, *febe*, *indc_r*, *f* bits and user defined overhead bits. In this mode the user may write to the corresponding bits in the MXOH registers, but the LXP730 will ignore them and insert the predefined bits into the bit stream.

The frame sync word (FSW) bit pattern consists of the following 14 bits in order from left to right: (10101000001000), this generates the +3 +3 +3 -3 -3 +3 -3 quat valued sync waveform on the MDSL. Other valid sync patterns are the time-reversed, sign bit inverted, and the time reversed sign bit inverted patterns shown in Table 6. The generation and detection of the FSW is automatic.

Detection of a frame that has an inverted sign bit causes the MDSL block to invert the sign bits of the data stream before it is sent to the descrambler.

Stuff-bits are normally either four (4) bits or zero (0) bits immediately before the sync word of the next frame. The stuffing decision circuit is located in the MDSL Interface block. A special mode fixes the stuff bits at two per frame for applications that require fixed timing such as connections from a wireless base station to its remote sites. This is controlled by bit 0 in register 17h, FIFO_MISC.

The *los* bit is used to notify the other side of the DSL of a loss of source from the PCM bus.

CRC-6 bits are calculated at the transmitter for each frame and sent during the following frame. At the receiver the CRC-6 is calculated on the received frame, stored and then compared with the CRC-6 value received in the following frame. Sync word bits, stuff bits and *CRC-6* bits are the CRC-6 calculation.

The *febe* bit is set in the MX side to the other MDSL unit when a CRC-6 error detected is in the DX side.

The *indc_r* bit is set in the MX side to notify the other MDSL unit that it is ready to receive transport data.

2.12.2 Z bits

The first three Z bits in an MDSL frame are reserved for loop ID for multi-loop DSL systems by the ETSI standard. All other Z bits are user defined. One common use is to send the time slot configuration from the Local unit to the Remote unit.

The Z bits may either accessed through the registers or the OSIO interface. This is controlled by the Z_CTL bit in register 23h, MISC_CTL. When OH and Z bits both go through the OSIO, they go in order as listed in the frame structure in Table 7. For example: if transparent OH and Z bits all go through the OSIO, then the order for an MDSL frame is 2 OH bits, 12 Z bits, 10 OH bits, 12 Z bits, 10 OH bits, 12 Z bits, 10 OH bits, 12 Z bits. Switching to OH predefined, the corresponding predefined OH bits would not appear at the OSIO and there would be a gap at those time locations.

In HWC mode all the Z bits and the user definable OH bits go through the OSIO.

When the LXP730 is in fractional T1 mode, Z bits are part of the payload and not accessible, otherwise they are accessible in the Z bit registers.

2.13 MDSL Frame Format

The LXP730 has a transport frame format that adjusts automatically with the *N* setting. The overall structure remains constant while adjusting the number of time slots within the payload blocks. Table 7 and Figure 4 shows the overall frame format.

Table 6. MDSL Frame Sync Word (FSW) Patterns

Type Pattern	Bits	Quat Value
Normal	10101000001000	+3 +3 +3 -3 -3 +3 -3
Time-reversed	00100000101010	-3 +3 -3 -3 +3 +3 +3
Inverted-Sign-Bit	00000010100010	-3 -3 -3 +3 +3 -3 +3
Inverted-Sign-Time-Reversed	10001010000000	+3 -3 +3 +3 -3 -3 -3

Table 7. MDSL Frame Format

Description	Number of Bits
Sync Word	14
MOH	2
B1-B12	$[Z + (N \times 8)] \times 12$
MOH	10
B13-B24	$[Z + (N \times 8)] \times 12$
MOH	10
B25-B36	$[Z + (N \times 8)] \times 12$
MOH	10
B37-B48	$[Z + (N \times 8)] \times 12$
Stuff	0 or 4, typ avg 2

The frame is made up of a sync word, followed by alternating sets of MDSL Overhead bits and groups of data blocks. The final element of each frame is a section set aside for stuffing, used to synchronize payload with DSL framing where required.

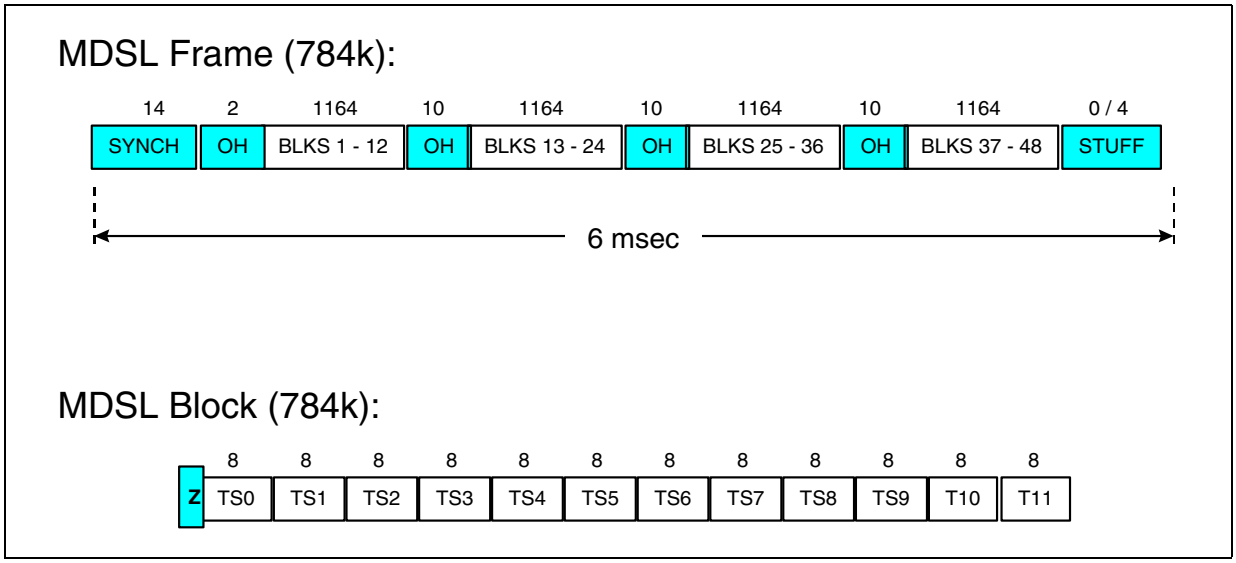
Each data block contains [Z + (N × 8)] bits. The blocks are transmitted in groups of 12. In T1 mode Z=1 and the 12 Z-bits per block group are reserved for framing/signalling and are referred to as *f*-bits. In all other modes they are user accessible overhead bits known as Z-bits. The frame structure matches the 784 kbps structure adopted by T1E1 and ETSI. For N=18 and Z=1, the frame format follows that of an 1168 kbps HDSL system compliant with ETSI standards.

2.14 Startup Operation

This description applies to the MPC mode for the LXP730. Typically the user sets most of the desired register values and then sets the RUN bit in register 24h, OVRHD_CFG. At this point the MX side of the framer is sending data to TDATA and the DX side is looking for the FSW. The next step requires clearing of INT_STAT register by writing OxFF to it. It must be ensured that the SK70725/21 chipset is in either Master or Slave mode as needed. The SK70725/21 chipset needs to be reset and the ACTIVATE bit toggled in the SK70725/21 chipsets. The main control register has to be toggled. In Master mode, the SK70725/21 will start the activation sequence with the Slave responding. In a few seconds the data pumps will have set their filter and echo coefficients and switch to transparent transport mode.

There is an additional setup to consider when the LXP730 is in PCM slave mode and N=18. If there is no clock running, then there is a halt condition when 18 PCM time slots are selected. The work around is to temporarily set the last two of the Nx registers to codec configuration, then set the RUN bit. Once that is done then change the Nx registers back to the desired PCM configuration.

Figure 4. Frame Format for N=12



The DX side of the LXP730 will go to ACTIVE upon receipt of two successive MDSL frames. When this first occurs, the ACTIVE bit in INT_STAT is set, but will stay reset once it is cleared until the framer goes to inactive and back to active again. The ACTIVE bit is edge triggered. The DSLACTIVE bit in CRC_FEBE_ST is level triggered or ‘sticky’.

Once the DSL is active, no support is required to keep it operating. At this point there are basically two tasks to perform: 1) monitor for error conditions, 2) use the overhead to pass messages/ signalling between the Local and Remote units.

Most of registers/bits can be changed while the RUN bit is set with the following exceptions:

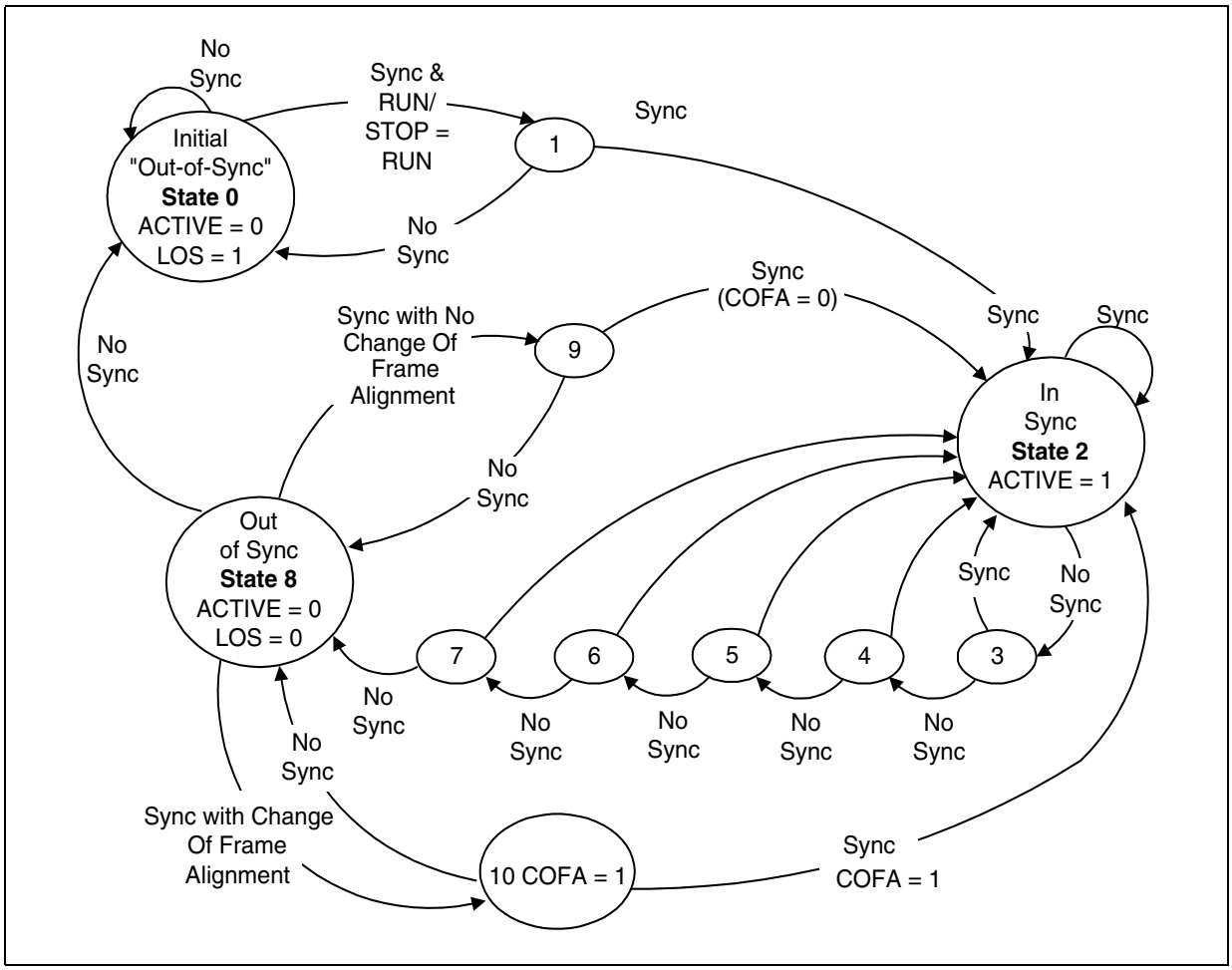
- N_MDSL register
- TX8KSSEL bit in 17h

The MX and DX FIFOs (MXFIFORXT & DXFIFORXT) should be reset whenever the PCM or codec clocks are changed while the framer is in the RUN mode. This will cause an interruption in the payload, but the DSL link will stay up.

2.15 Activation State Machine

The LXP730 framer has an ANSI T1E1.4/94-006 compatible activation state machine. The operation of the state machine is shown in Figure 5.

Figure 5. Activation State Machine



3.0 Application Information

3.1 Typical Applications

This section shows some block diagrams to serve as example applications. Connections to the LXP730 as shown emphasize those relevant for the application. Detailed connections to the processor are not shown.

Figure 6 demonstrates how the LXP730 can simultaneously handle voice from a PCM circuit and packet-type data from an HDLC style device.

Figure 7 is an example of the HWC mode. The codecs' digital interfaces connect directly to the LXP730. An external device is needed to handle signalling information for each voice line supported. In this case the Z bits could be used to carry the signalling information such as off-hook status from the CPE and ringing signal from the CO. An FPGA or a fast dedicated processor could handle these tasks.

Figure 6. High Performance Voice/Data Transport

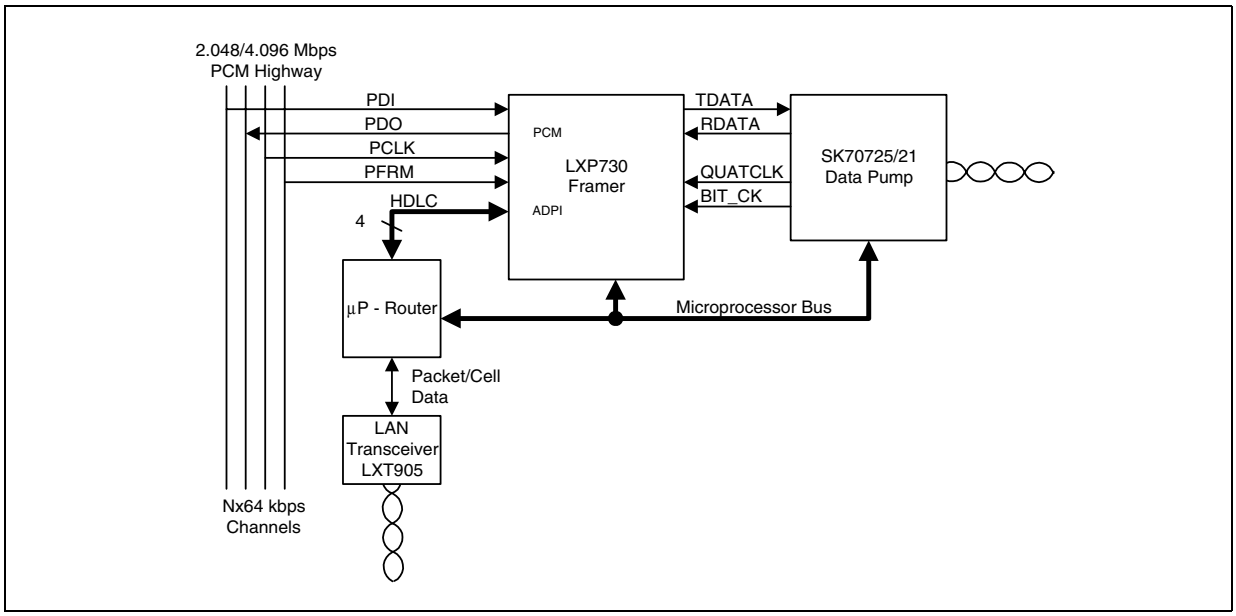


Figure 7. Pair Gain Transport

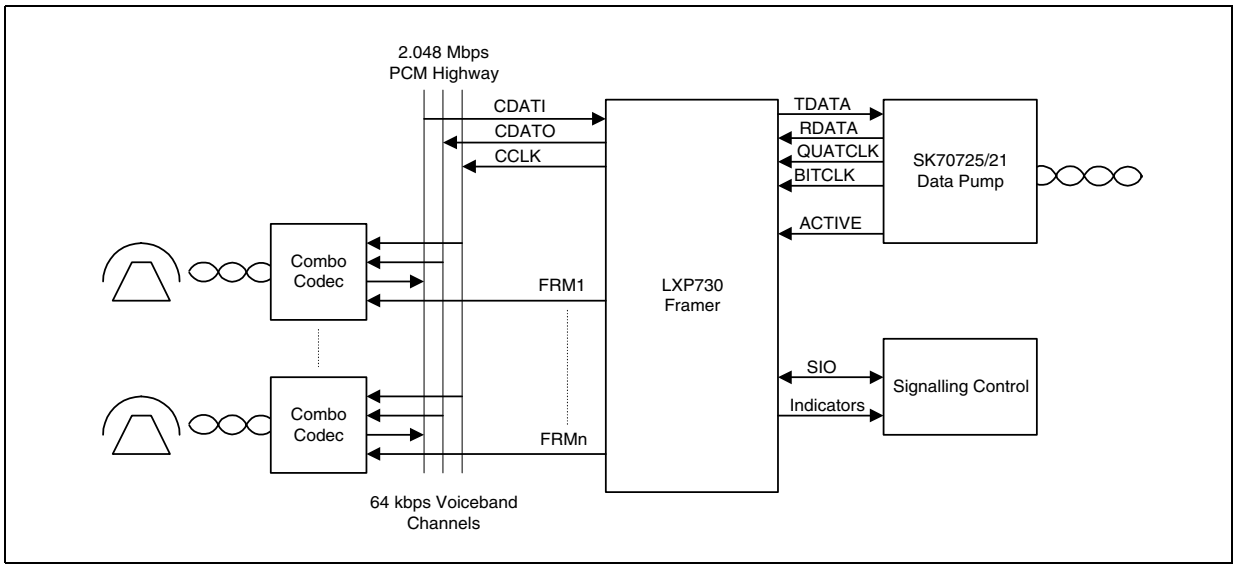


Figure 8 shows a more traditional DSL application to carry phone traffic over a longer distance on a single copper pair. The LXP730 supports the pleisiochronous nature of T1/E1 traffic.

3.1.1 IOM Interface Circuitry

The LXP730 uses a frame pulse in the second cycle of the two clocks per data bit timing. This is directly compatible with the ST electrical interface. The IOM interfaces use the first clock cycle for the frame pulse. The circuit in Figure 9 shows how to adapt the LXP730 to the IOM bus. Note that even though the circuit is the same for the PCM master or slave modes, there is a difference in the connections to the LXP730 and the IOM device.

Figure 8. T1/E1 Fractional Transport

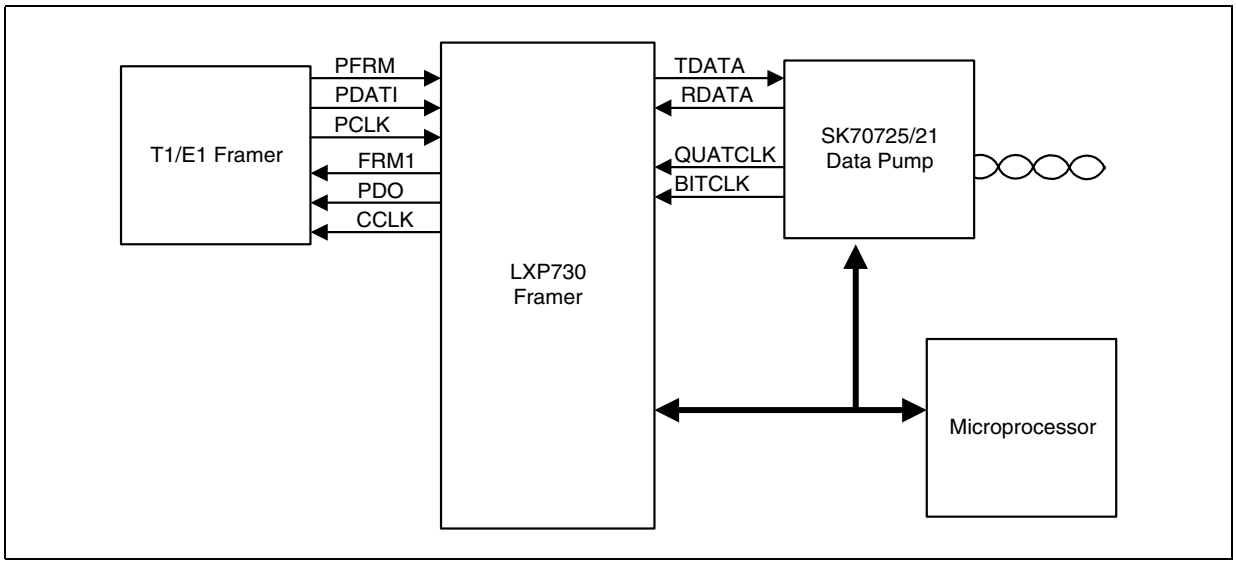
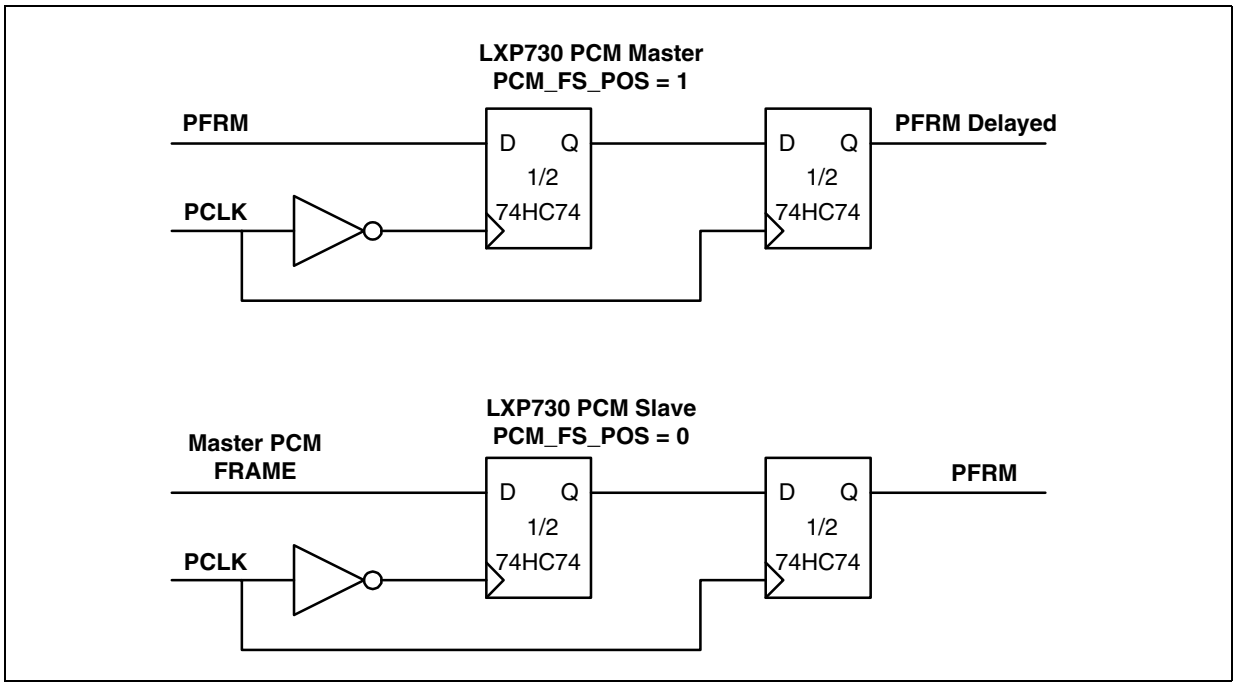


Figure 9. IOM Adaption Circuitry



3.1.2 Handling TIP/RING Reversal in Early Version of SK70725

The early version of the SK70725 data pump device has an error in the Master (CO) mode. The QUAT_CLK is not aligned correctly with the RDATA for the sign and magnitude bits. When there is no TIP/RING reversal, the LXP730 is able to correctly parse the data bits. However, when TIP/RING reversal has occurred the LXP730 detects that the sign bit is inverted by detecting the inverted Frame Sync Word (FSW) pattern. The LXP730 then uses the QUAT_CLK to determine which bit to invert. The sign bit is already inverted and the LXP730 inverts the magnitude bit. This problem does not occur in the Slave (CPE) mode of the SK70725. The SK70725 has the ability to invert the received data pulses inside itself. This is done by setting bit 7 of the register WR2. The following procedure takes advantage of how the LXP730 reacts during the error condition and the ability to invert the data stream from the SK70725. The procedure uses one of the Z-bit bytes after frame sync has been achieved to determine if there is a tip-ring reversal at the LTU. DXZ2 and MXZ2 are good choices and are used only at the start up time. The TIP/RING reversal indicator in the SK70725 does not have any meaning in mode 0, as the transparent mode needed to work with LXP730. This procedure can be left in the code for the future SK70725 revision. The procedure also shows how to handle BELB from the CPE end.

TIP/RING Reversal Procedure:

1. Start.
2. Initialize the LXP730s for required configuration.
3. Activate the SK70725s.
4. Send the test pattern MXZ2 from the NTU side. MXZ2 = AAh.
5. If DXZ2 = AAh is received on LTU TIP/RING lines are straight and system is ready for transmission. Go to step 7.

6. Otherwise if DXZ2 = 55h, set B7 to 1 in register WR2 of SK70725 (Address 02, data 80h). Set bit B0 to 0 in register 24h of LXP730 to stop it and then set this bit back to 1 to re-start. The framer needs to be restarted to recognize the new sync word. TIP/RING lines are reversed and corrected for in the SK70725, and the system is ready for transmission.
7. Normal operation.

For BELB (Back End Loop Back) on the NTU side:

8. Send message to NTU side to set the SK70725 in BELB (set bit B6 to 1 in register WR0 of SK70725 on the NTU side).
9. If the TIP/RING was detected to be straight then set B4 to 1 in register 17h in LTU LXP730 (Address 57h, data 10h) and go to step 11. BELB is completed and the system is ready for transmission.
10. If the TIP/RING reversal was detected and corrected on the LTU side, then set B7 to 0 in register WR2 of LTU SK70725. Set B4 to 1 in register 17 in LXP730 (Address 57h, data 10h). Set bit B0 to 0 in register 24 of LXP730 to stop it and then set this bit back to 1 to re-start. BELB is completed and the system is ready for transmission.
11. When BELB testing is done, reset B4 to 1 in register 17h in LTU LXP730 and send the command to NTU to undo BELB. Before NTU shuts off BELB all received payload and overhead data will be scrambled with the wrong polynomial and the value in DXZ2 will jump. At the LTU wait until there are two consecutive frames where DXZ2 = 55h or AAh.
12. Go to step 4.

3.1.3 DSL System Loopbacks

Data loopbacks in telecom systems are primarily used for system diagnostics. These tests are usually either BER (Bit Error Rate), or to determine which part of the system is malfunctioning.

In DSL systems the loopback points are usually controlled by the CO (Central Office) end. Line cards may have one or more DSL loops, and the processor on the board sets the loopback operation; typically on command from the central control point in the switching system.

The loopback in the linecard demonstrates that the data can successfully be moved from the input at the MX section through the DX section to receive side of the payload. Typically this is done with the data pump Front End Loop Back (FELB). This transmits the data onto the wire pair, but the receive signal from the wire pair is ignored. Instead, the DSL receiver is fed the signal from the transmitter via an internal multiplexer.

The framer also has a loop back that ignores data from the data pump. This is useful in isolating the data pump as the source of a malfunction such as when the line has been hit by lightning.

A back end loopback (BELB) is used to test the wire pair and the remote data pump. Here the RDATA from the data pump is passed to the framer so it can still receive commands from the CO, such as to turn off the BELB.

A payload loopback at the remote line card will check out the framer and give a more complete evaluation of the DSL system.

The CO and the CPE each use a different scrambling polynomial in their transmitted data. Each side expects to receive a different scrambling setting than the one they transmit. When the framer is in loopback it knows to switch its receive scrambler to match the transmitter. When the local

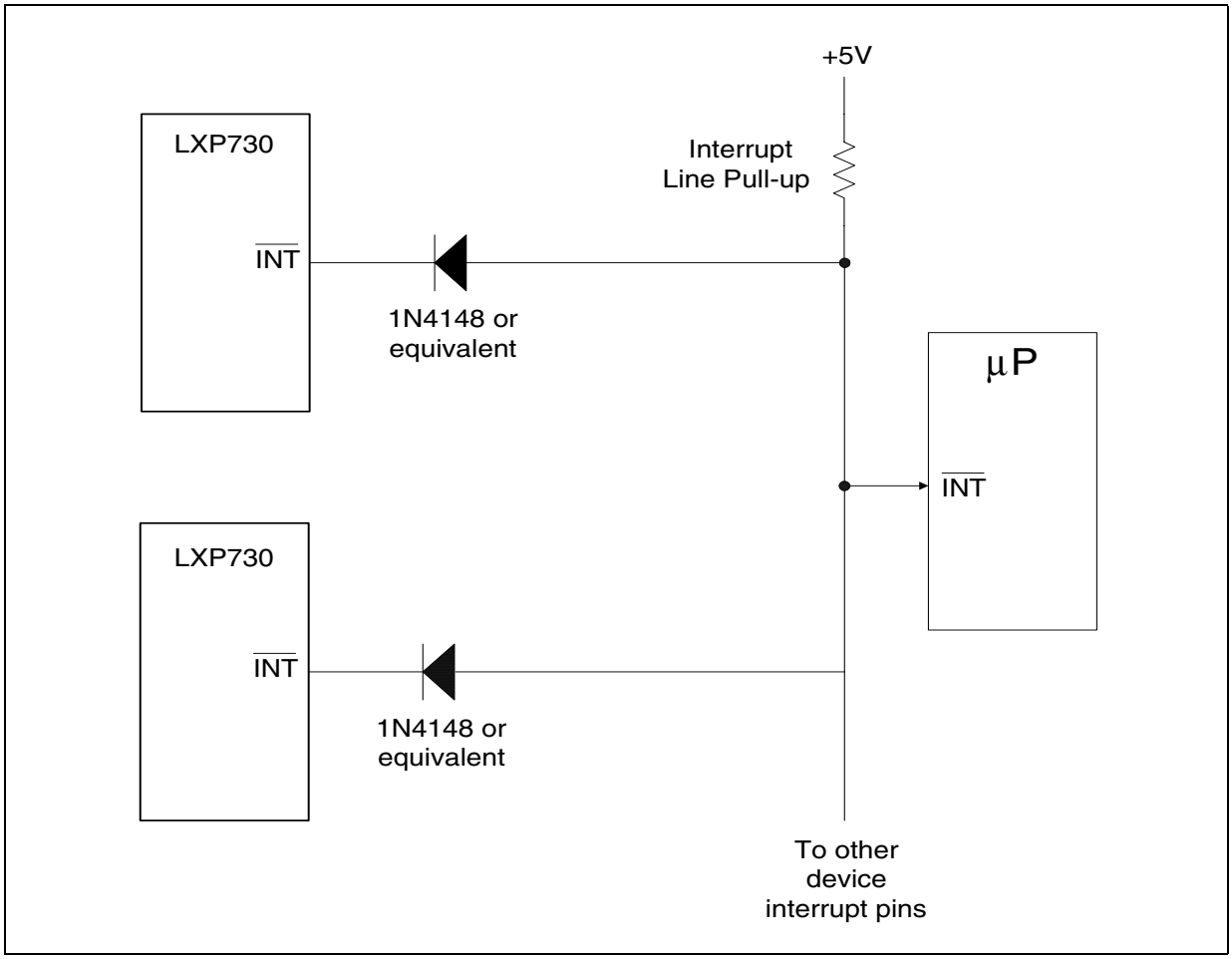
FELB is on, the framer does not know by itself that its receive scrambler has to be switched. Switching is accomplished in the LXP730 by setting the REMOTE_LB bit in register 17h. This also needs to be done when the remote BELB is in operation.

When the remote CPE end switches off the BELB the CO end will not correctly interpret the data until the REMOTE_LB is turned off. However it will still recognize the FSW because it is not scrambled.

3.1.4 Using Multiple Devices on an Interrupt Line

The LXP730 $\overline{\text{INT}}$ pin is an output pin and therefore requires a circuit, as shown in Figure 10, to operate with additional devices that share the same interrupt line to the microprocessor. Each LXP730 that is tied to the shared interrupt line will need its own isolating diode.

Figure 10. Multiple Interrupt Line Circuit



4.0 Test Specifications

Note: Table 8 through Table 23 and Figure 11 through Figure 24 represent the performance specifications of the LXP730 and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 10 through Table 23 are guaranteed over the recommended operating conditions specified in Table 9.

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	-0.3	6	V
Storage temperature	T_{ST}	-65	+150	ºC
Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.				

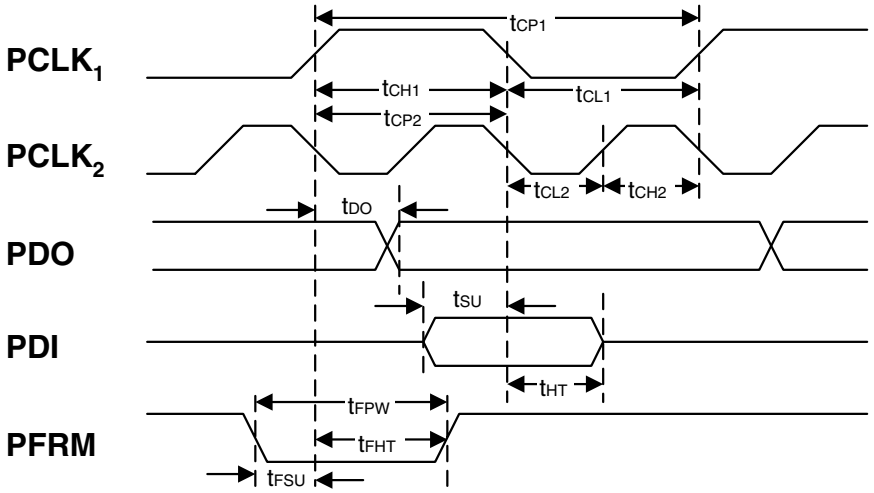
Table 9. Recommended Operating Conditions

Parameter	Sym	Min	Typ[1]	Max	Unit
Recommended supply voltage	V_{CC}	4.5	5.0	5.5	V
Recommended operating temperature	T_{OP}	-40	25	+85	°C
Power dissipation	PD	-	0.3	0.6	W
1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.					

Table 10. I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Input Low voltage	V_{IL}	–	–	0.3xV_{CC}	V	CMOS inputs
Input High voltage	V_{IH}	0.7xV_{CC}	–	–	V	CMOS inputs
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	0.7xV_{CC}	–	–	V	I_{OH} = -4 mA
Input Low current	I_{IL}	-10	–	–	µA	V_{IN} = Gnd, V_{CC} = 5.5V
Input High current	I_{IH}	–	–	10	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V
Output rise/fall time	t_R, t_F	–	5	–	ns	C_{LOAD} = 30 pF
Capacitance, any input pin	C_{IN}	–	12	–	pF	
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 11. Generic PCM Interface Timing



NOTES:

$PCLK_1$ = 1x clock, $PCLK_2$ = 2x clock.
Clock sampling edges and frame pulse polarity are programmable.

Table 11. Generic PCM Bus Interface Timing Specifications (See Figure 11)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
PCLK period	t_{CP1} t_{CP2}	122	–	3906	ns	
PCLK duty cycle input		40	–	60	%	
PCLK duty cycle output (MCLK)			50		%	
PCLK duty cycle output (ADPLL)		See Note 2				
PDO delay time	t_{DO}	–	–	80	ns	
PDI setup time	t_{SU}	20	–	–	ns	
PDI hold time	t_{HT}	10	–	–	ns	
PFRM setup time	t_{FSU}	20	–	–	ns	
PFRM hold time	t_{FHT}	10	–	–	ns	
PFRM pulse width	t_{FPW}		1		tcp	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. UI Jitter = PCLK frequency ÷ MCLK frequency.

Figure 12. PCM Timing, 1X Clock

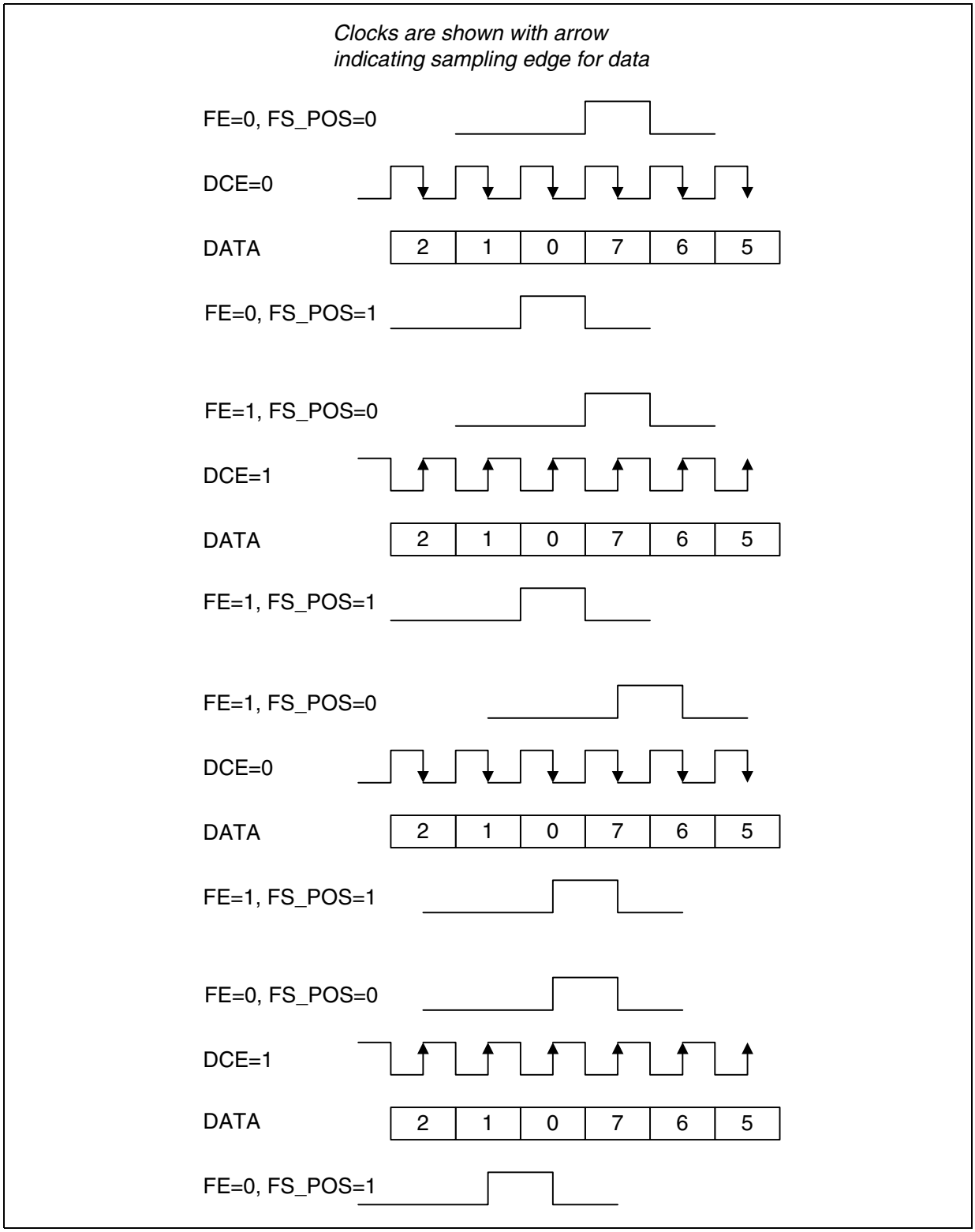


Figure 13. PCM Timing, 2X Clock

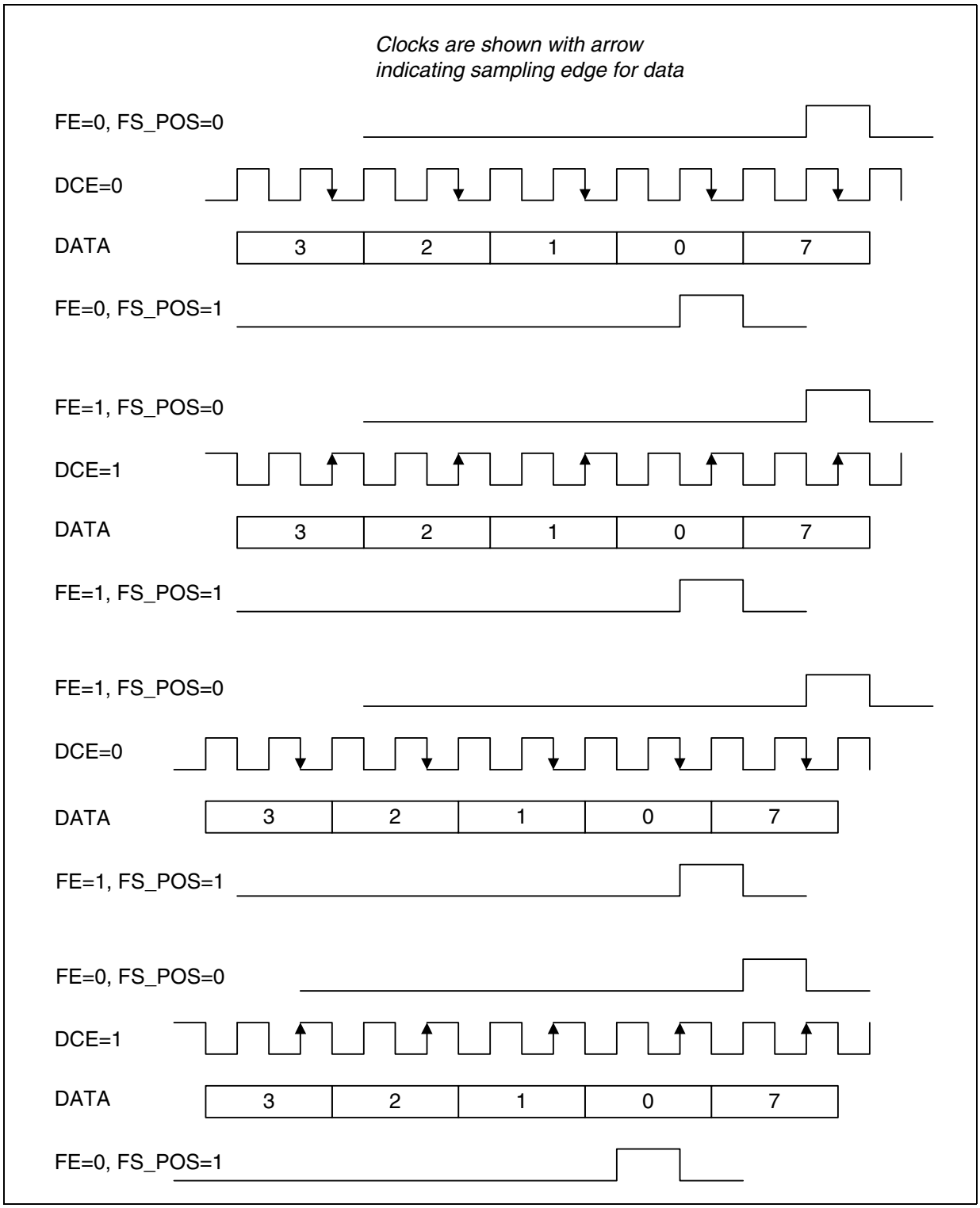


Figure 14. Codec Interface Timing

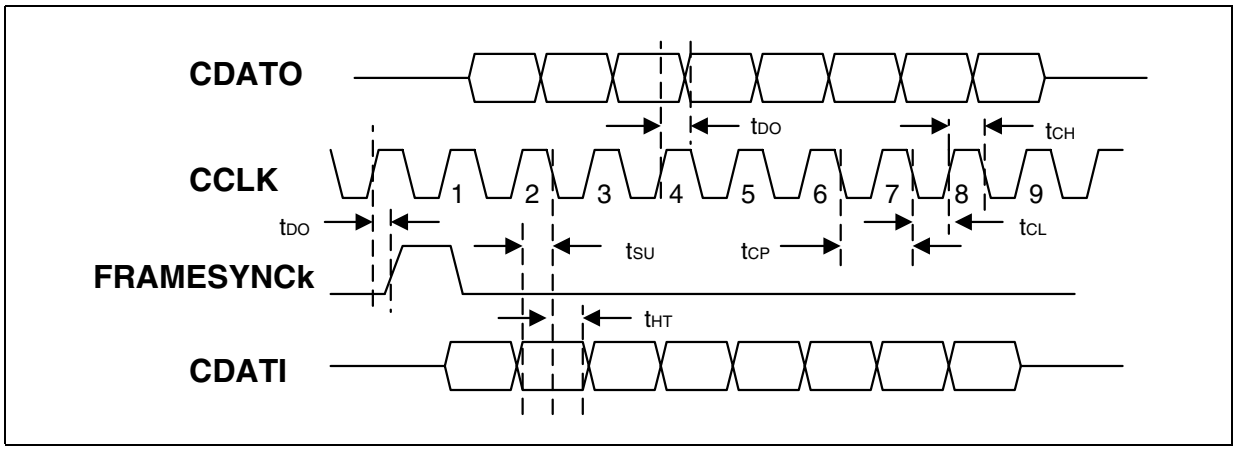


Table 12. Codec Interface Timing Specifications (See Figure 14)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output delay time of CDATO, FRAMESYNCk	t_{DO}	–	–	40	ns	Referenced from rising edge of CCLK
Codec clock period	t_{CP}	122	488	3906	ns	
CCLK duty cycle output (MCLK)			50		%	
CCLK duty cycle output (ADPLL)		See Note 2				
CDATI setup	t_{SU}	20	–	–	ns	Referenced from the falling edge of CCLK
CDATI hold time	t_{HT}	50	–	–	ns	Referenced from the falling edge of CCLK

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. UI Jitter = PCLK frequency ÷ MCLK frequency.

Figure 15. Asynchronous Port Timing

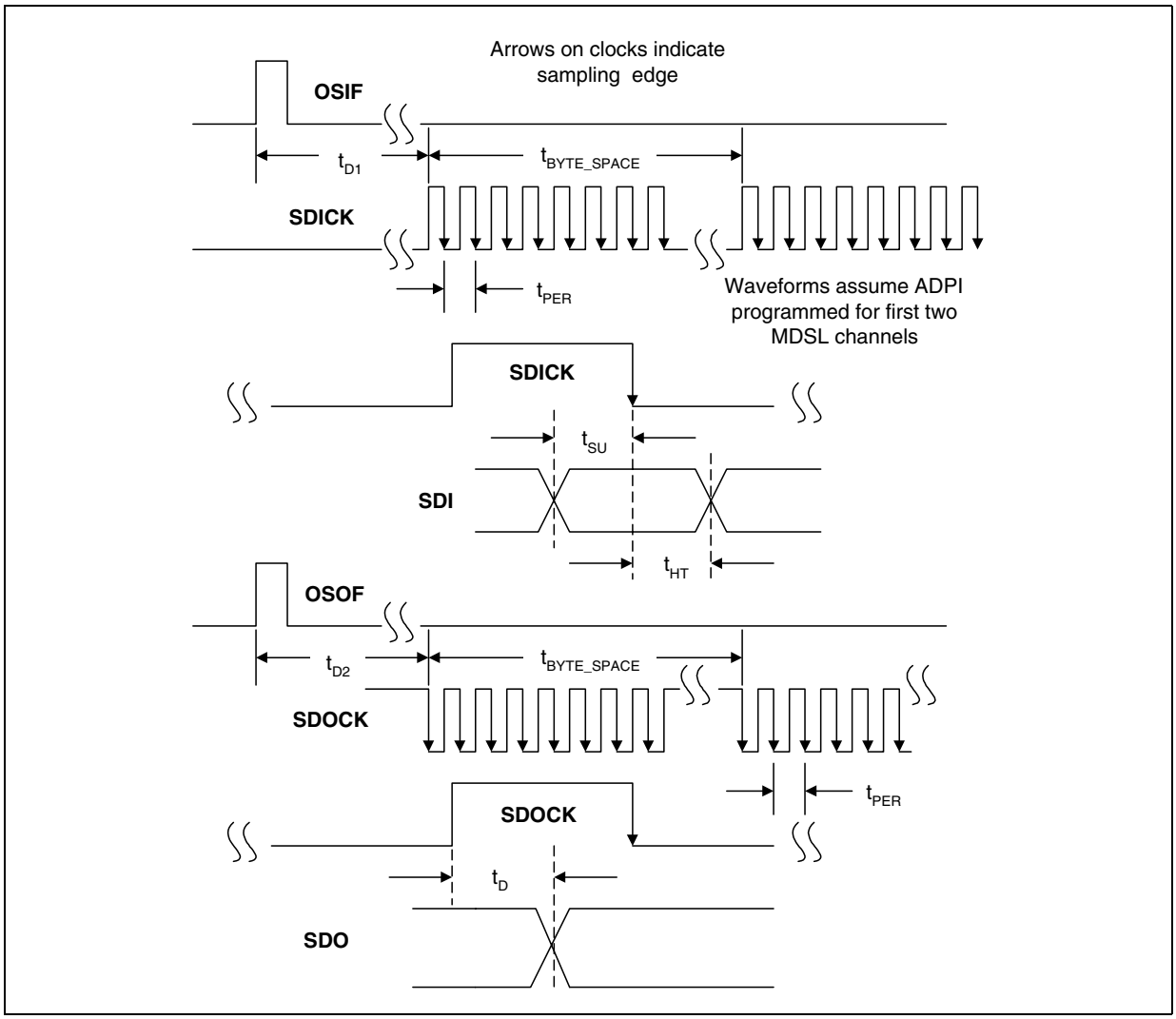
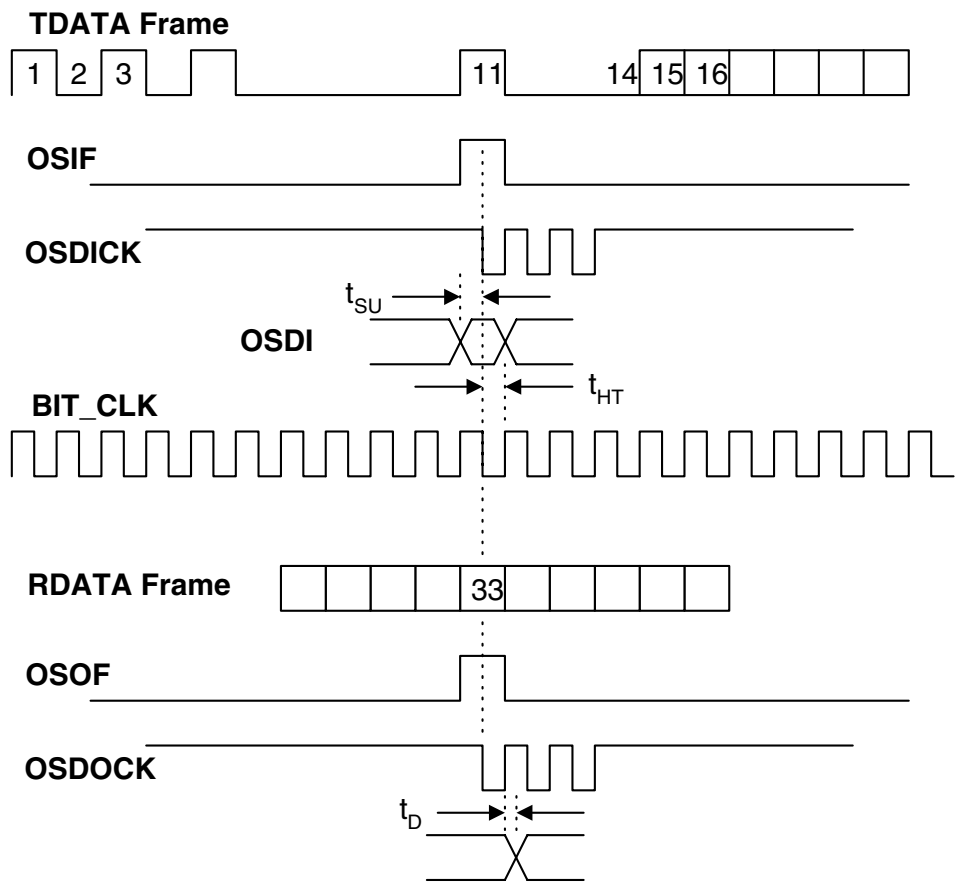


Table 13. Asynchronous Port Timing Specifications (See Figure 15)

Parameter	Sym	Min	Typ[1]	Max	Unit
Time to next adjacent byte	tBYTE_SPACE	-	8 x BIT_CLK^{-1}	-	seconds
Clock period	tPER	-	MCLK^{-1} x SAPCLKDIV	-	seconds
Delay to first transmit byte	tD1	-	140 x BIT_CLK^{-1}	-	seconds
Delay to first receive byte	tD2	-	11 x BIT_CLK^{-1}	-	seconds
Set-up time	tSU	20	-		ns
Hold time	tHT	10	-		ns
Output delay	tD	-	-	40	ns
1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.					

Figure 16. OSIO Timing



NOTE:

1. OSDICK and OSDOCK are shown for OH transparent setting, and both OH and Z bits tr
2. Data waveforms exagerated with respect to clock to show timing details more clearly.

Table 14. OSIO Timing Specifications (See Figure 16)

Parameter	Sym	Min	Typ[1]	Max	Unit
Set-up time	tSU	-	-	20	ns
Hold time	tHT	10	-	-	-
Output delay	tD	-	-	80	ns
1. Typical figures are at 25° C and are for design aid only; not guaranteed and not subject to production testing.					

Figure 17. MDSL Interface Input Timing

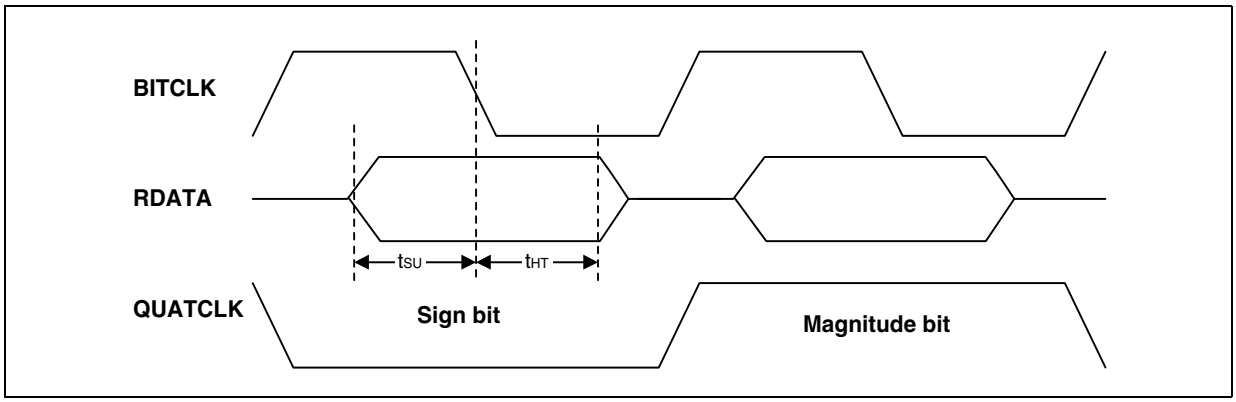


Table 15. MDSL Interface Input Timing Specifications (See Figure 17)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Setup time of RDATA	t_{SU}	30	–	–	ns	Referenced from falling edge of BITCLK
Hold time of RDATA	t_{HT}	10	–	–	ns	Referenced from falling edge of BITCLK
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 18. MDSL Interface Output Timing

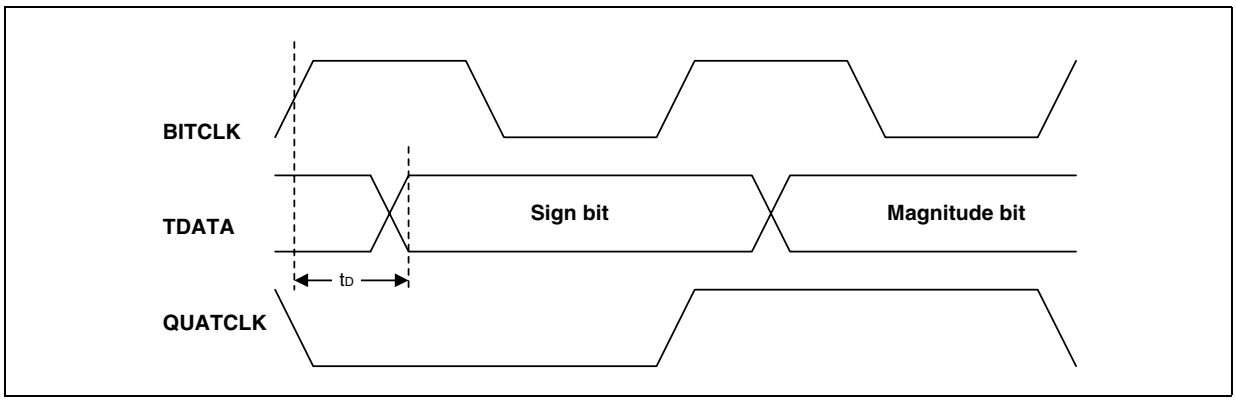


Table 16. MDSL Interface Output Timing Specifications (See Figure 18)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output delay time of TDATA	t_D	–	–	100	ns	Referenced from rising edge of BITCLK
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 19. E1/T1 Input Timing

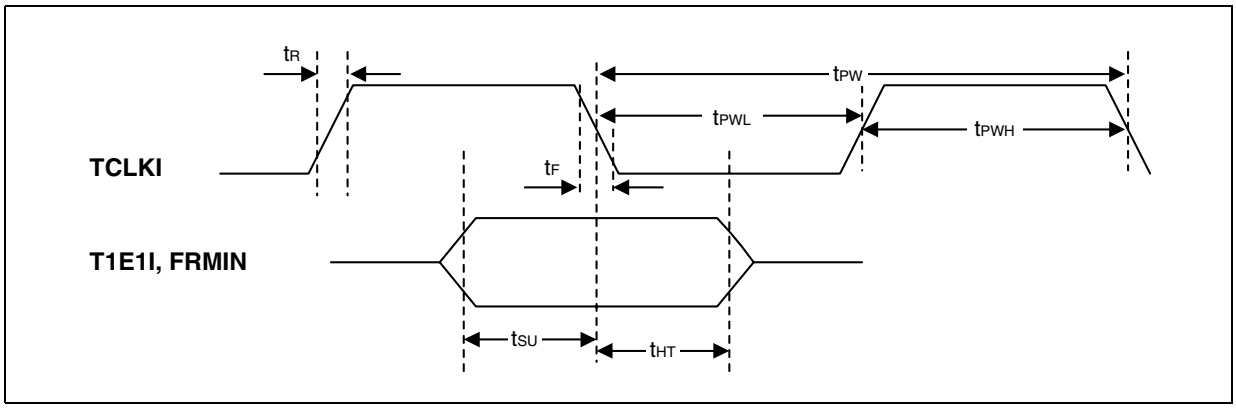


Table 17. E1/T1 Input Timing Specifications (See Figure 19)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Setup time of T1E1I, FRMIN	t_{SU}	30	–	–	ns	Referenced from falling edge of PCLK
Hold time of T1E1I, FRMIN	t_{HT}	10	–	–	ns	Referenced from falling edge of PCLK
E1, T1 clock period	t_{PW}	–	488, 647	–	ns	
TCLKI pulse width low	t_{PWL}	50	–	–	ns	
TCLKI pulse width high	t_{PWH}	50	–	–	ns	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 20. E1/T1 Output Timing

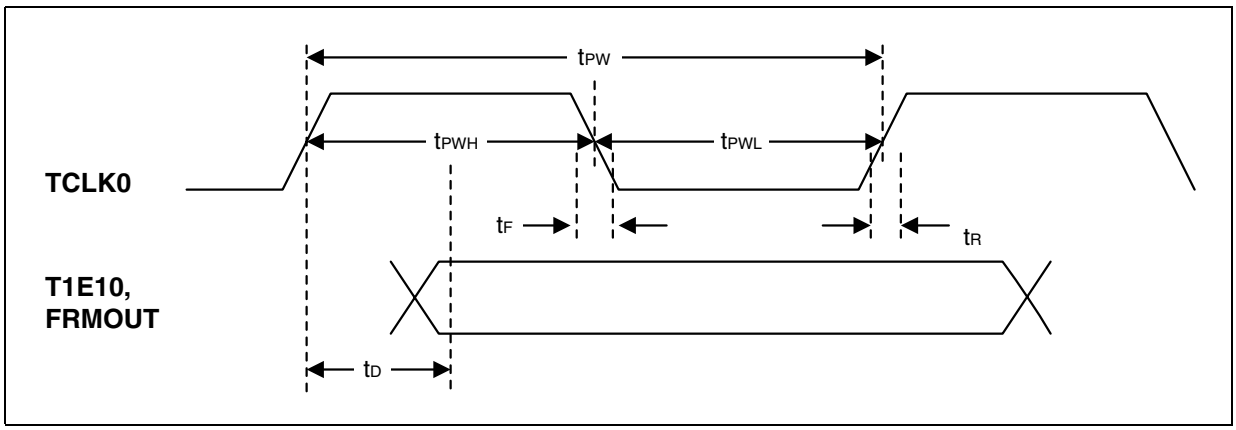


Table 18. E1/T1 Output Timing Specifications (See Figure 20)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Output delay time of T1E10, FRMOUT	t_D	–	–	100	ns	Referenced from rising edge of CCLK
E1, T1 nominal clock period	t_{PW}	–	488, 647	–	ns	
TCLK0 pulse width Low	t_{PWL}	50	–	–	ns	
TCLK0 pulse width High	t_{PWH}	50	–	–	ns	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 21. Microprocessor Write Cycle - Motorola Mode

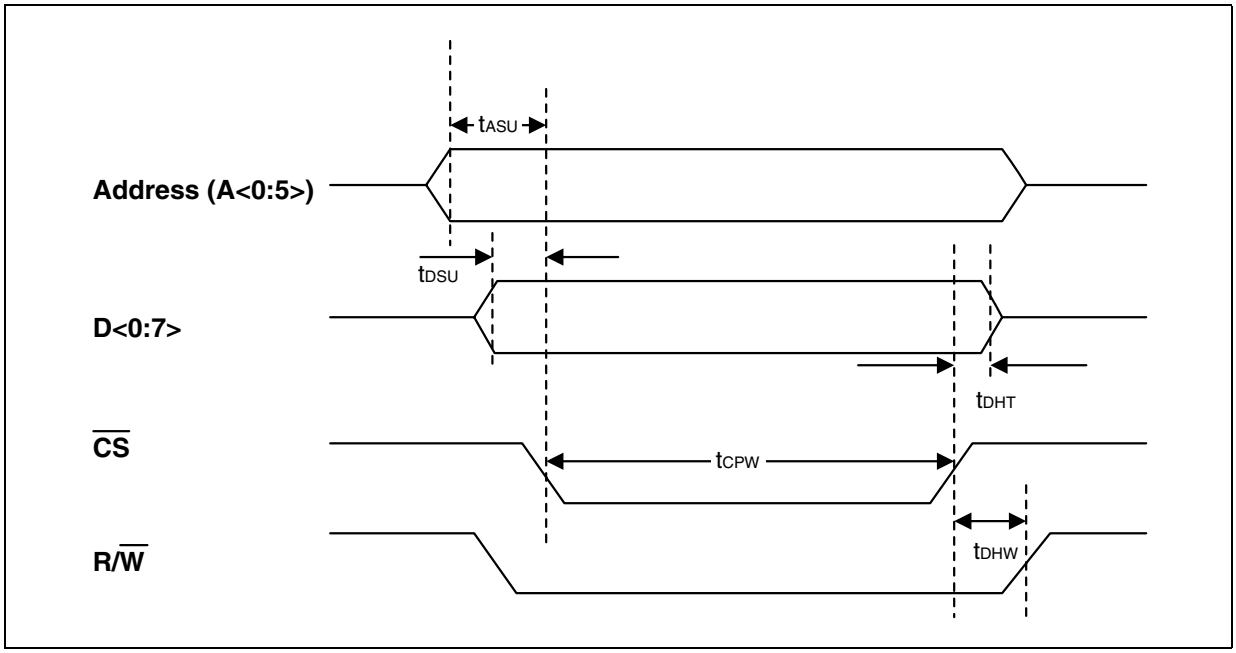


Table 19. Microprocessor Write Cycle Specifications—Motorola Mode (See Figure 21)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time to $\overline{CS}$	t_{ASU}	20	–	–	ns	
D<0:7> setup time to $\overline{CS}$	t_{DSU}	0	–	–	ns	
Data-In hold time from $\overline{CS}$	t_{DHT}	10	–	–	ns	
Allowable $\overline{CS}$ width	t_{CPW}	4/MCLK	–	–	s	
Write hold time	t_{DHW}	20			ns	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 22. Microprocessor Read Cycle - Motorola Mode

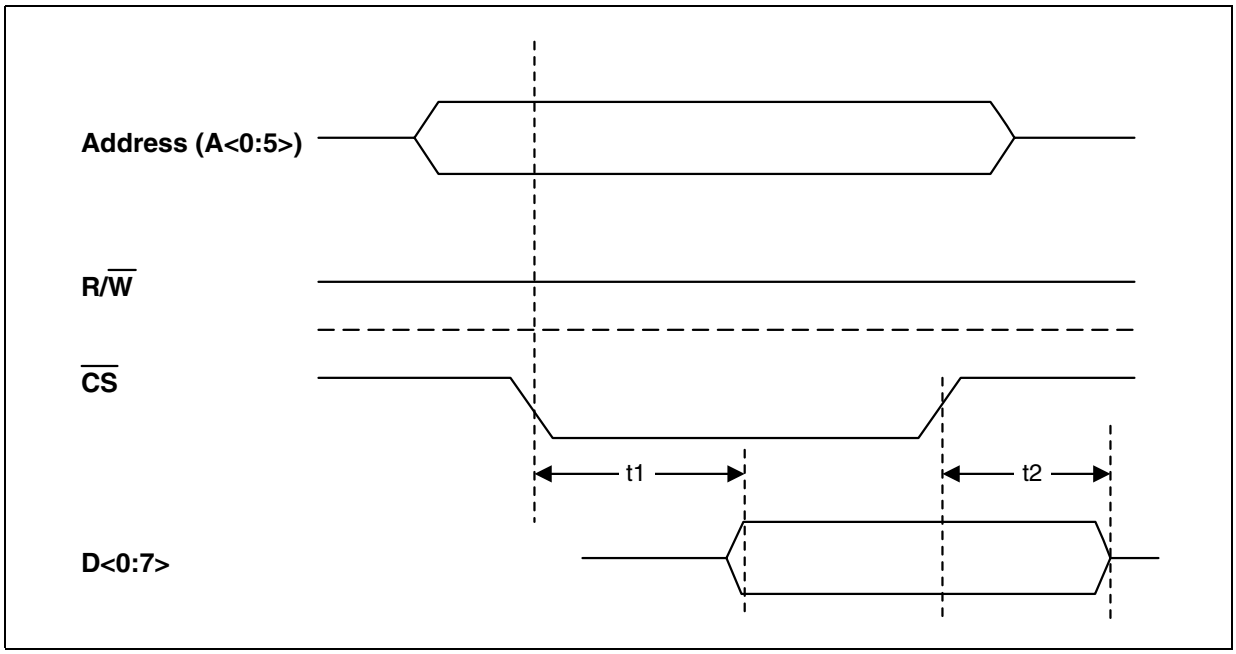


Table 20. Microprocessor Read Cycle Specifications - Motorola Mode (See Figure 22)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
D<0:7> valid after $\overline{CS}$	t1	–	-	4/MCLK	s	
D<0:7> keep valid after $\overline{CS}$ negation	t2	–	–	10	ns	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 23. Microprocessor Write Cycle - Intel Mode

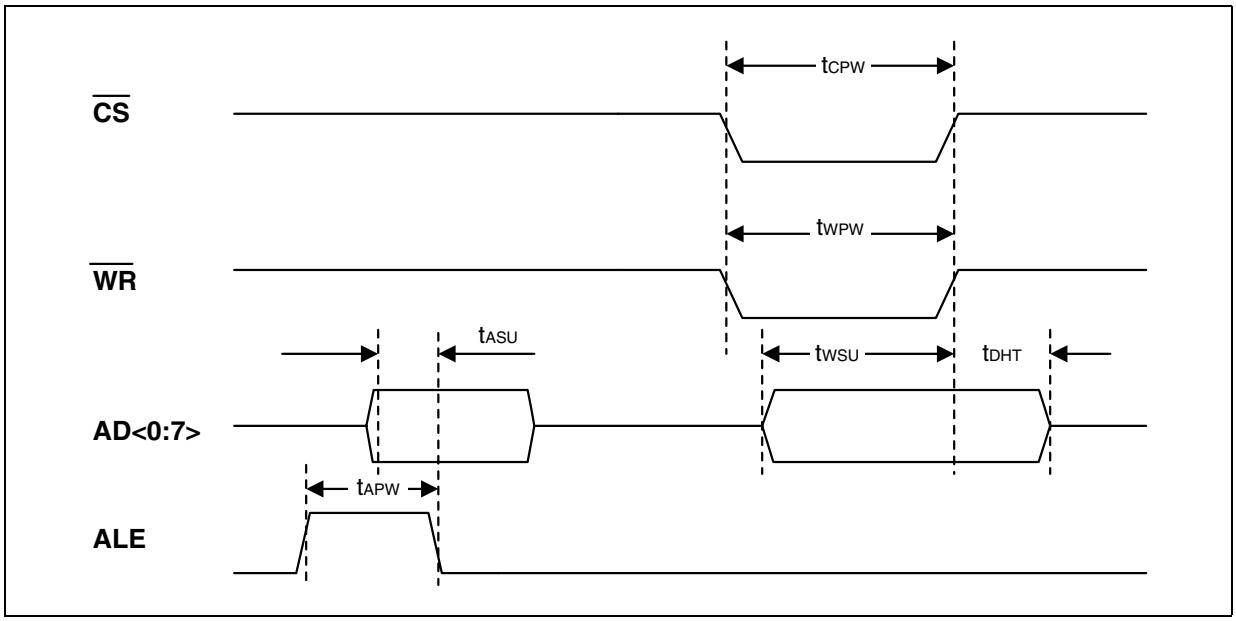


Table 21. Microprocessor Write Cycle Specifications—Intel Mode (See Figure 23)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time	t_{ASU}	30	–	–	ns	Referenced from falling edge of ALE
Address latch enable pulse width	t_{APW}	30			ns	
D<0:7> setup time	t_{WSU}	30	–	–	ns	Referenced from rising edge of $\overline{CS}$ or $\overline{WR}$
D<0:7> hold time	t_{DHT}	10	–	–	ns	Referenced from rising edge of $\overline{CS}$ or $\overline{WR}$
$\overline{CS}$ width	t_{CPW}	4/MCLK	–	–	s	
$\overline{WR}$ width	t_{WPW}	4/MCLK	–	–	s	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 24. Microprocessor Read Cycle - Intel Mode

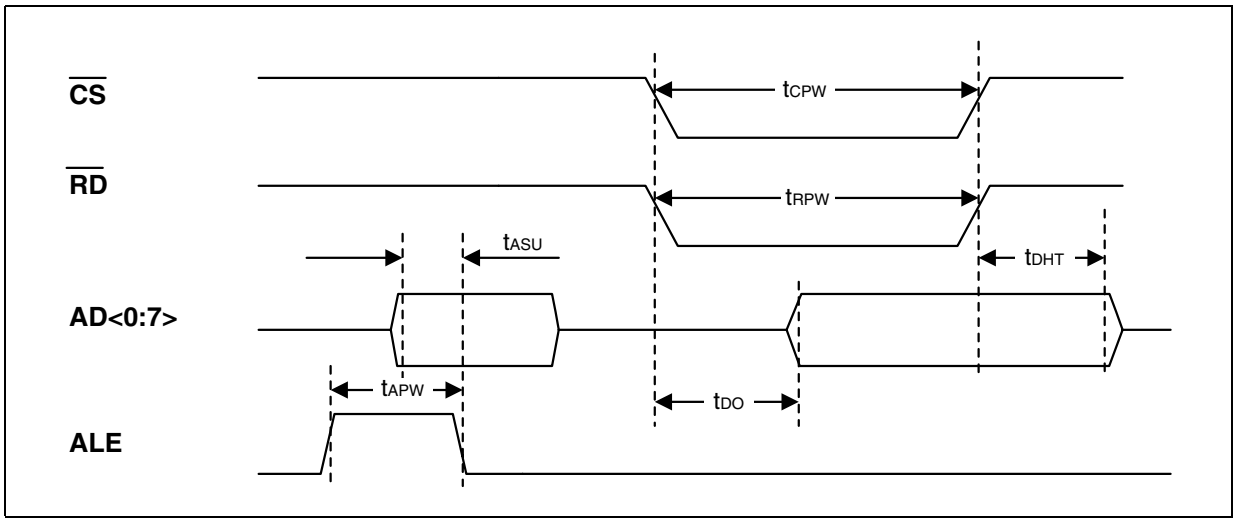


Table 22. Microprocessor Read Cycle Specifications—Intel Mode (See Figure 24)

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Address setup time	t_{ASU}	30	–	–	ns	Referenced from falling edge of ALE
Address latch enable pulse width	t_{APW}	30	–	–	ns	
D<0:7> valid after $\overline{CS}$, $\overline{RD}$ assertion	t_{DO}	–	–	60	ns	Referenced from the falling edge of $\overline{RD}$ and $\overline{CS}$
D<0:7> keep valid after $\overline{CS}$, $\overline{RD}$ negation	t_{DHT}	–	10	20	ns	Referenced from rising edge of $\overline{CS}$ or $\overline{RD}$
Allowed width of $\overline{CS}$	t_{CPW}	4/MCLK	–	–	s	
Allowed width of $\overline{RD}$	t_{RPW}	4/MCLK	–	–	s	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Table 23. MCLK Frequency and Tolerance Specification

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
MCLK frequency	F_{mclk}	–	–	24.832	MHz	
MCLK duty cycle	M_{DC}	40	–	60	%	
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 25. Reset Timing

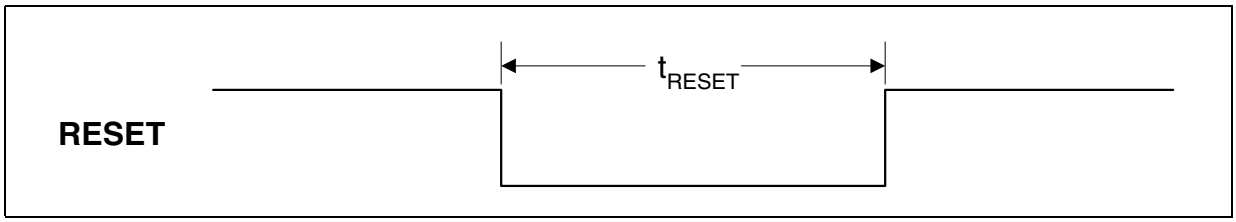


Table 24. Reset Timing Specifications (See Figure 25)

Parameter	Sym	Min	Typ	Max	Unit
Reset Time	tRESET	3	-	-	Clock periods of slowest externally applied clock

5.0 Register Definitions

Table 25. LXP730 Register Summary

Hex Address	Decimal Address	Symbol	Type	Description
00	0	N_MDSL	R/W	Number of nx64 channels
01	1	N1	R/W	MDSL channel 1 configuration
02	2	N2	R/W	MDSL channel 2 configuration
03	3	N3	R/W	MDSL channel 3 configuration
04	4	N4	R/W	MDSL channel 4 configuration
05	5	N5	R/W	MDSL channel 5 configuration
06	6	N6	R/W	MDSL channel 6 configuration
07	7	N7	R/W	MDSL channel 7 configuration
08	8	N8	R/W	MDSL channel 8 configuration
09	9	N9	R/W	MDSL channel 9 configuration
0A	10	N10	R/W	MDSL channel 10 configuration
0B	11	N11	R/W	MDSL channel 11 configuration
0C	12	N12	R/W	MDSL channel 12 configuration
0D	13	N13	R/W	MDSL channel 13 configuration
0E	14	N14	R/W	MDSL channel 14 configuration
0F	15	N15	R/W	MDSL channel 15 configuration
10	16	N16	R/W	MDSL channel 16 configuration
11	17	N17	R/W	MDSL channel 17 configuration
12	18	N18	R/W	MDSL channel 18 configuration
13	19	RSVR1	-	Reserved for future use
14	20	RSVR2	-	Reserved for future use
15	21	RSVR3	-	Reserved for future use
16	22	WANDER	R/W	Wander Reduction Register
17	23	FIFO_MISC	R/W	Fifo/Miscellaneous Control Register
18	24	SLIP_THDL	R/W	Slip Buffer Threshold Low Level
19	25	SLIP_THDH	R/W	Slip Buffer Threshold High Level
1A	26	VERSION	R	Version of the LXP730
1B	27	PLLCTL1	R/W	ADPLL Control 1
1C	28	PLLCTL2	R/W	ADPLL Control 2
1D	29	PLLCTL3	R/W	ADPLL Control 3
1E	30	PROG_DIV	R/W	MCLK Divide for PCM/codec blocks
1F	31	IDLE	R/W	Idle code for blocked PCM and MDSL slots
20	32	PCM1_CFG	R/W	PCM 1 configurations
21	33	PCM2_CFG	R/W	PCM 2 configuration

Table 25. LXP730 Register Summary *(Continued)*

Hex Address	Decimal Address	Symbol	Type	Description
22	34	COD_CFG	R/W	Codec Configuration
23	35	MISC_CTL	R/W	Miscellaneous Control
24	36	OVRHD_CFG	R/W	Overhead mode
25	37	CRC_ERR_CNT	R/W	CRC error counter
26	38	FEBE_ERR_CNT	R/W	FEBE error counter
27	39	CRC_FEBE_ST	R/W	CRC and FEBE status
28	40	MXOH1	R/W	Mux Overhead Bits 1 - 8
29	41	MXOH2	R/W	Mux Overhead Bits 9 - 16
2A	42	MXOH3	R/W	Mux Overhead Bits 17 - 24
2B	43	MXOH4	R/W	Mux Overhead Bits 25 - 32
2C	44	MXZ1	R/W	Mux Z Bits 1 - 8
2D	45	MXZ2	R/W	Mux Z Bits 9 - 16
2E	46	MXZ3	R/W	Mux Z Bits 17 - 24
2F	47	MXZ4	R/W	Mux Z Bits 25 - 32
30	48	MXZ5	R/W	Mux Z Bits 33 - 40
31	49	MXZ6	R/W	Mux Z Bits 41 - 48
32	50	DXOH1	R	Demux Overhead Bits 1 - 8
33	51	DXOH2	R	Demux Overhead Bits 9 - 16
34	52	DXOH3	R	Demux Overhead Bits 17 - 24
35	53	DXOH4	R	Demux Overhead Bits 25 - 32
36	54	DXZ1	R	Demux Z Bits 1 - 8
37	55	DXZ2	R	Demux Z Bits 9 - 16
38	56	DXZ3	R	Demux Z Bits 17 - 24
39	57	DXZ4	R	Demux Z Bits 25 - 32
3A	58	DXZ5	R	Demux Z Bits 33 - 40
3B	59	DXZ6	R	Demux Z Bits 41 - 48
3C	60	RSVR4	-	Reserved for future use
3D	61	RSVR5	-	Reserved for future use
3E	62	INT_EN	R/W	Interrupt enables
3F	63	INT_STATUS	R/W	Interrupt status flags

5.1 Number MDSL Channels Register

Address: 00

Abbreviation: N_MDSL

Read/Write

Table 26. Number MDSL Channels

Bit	Name	Default	Description
<7:5>	Z_NUM	0	Number of Z bits in a group, valid values 0 - 7, Number of Z bits = Z_NUM + 1. For T1/E1, only Z_NUM = 0 is valid
<4:0>	Number<4:0>	3	Number of MDSL channels, valid values: 3 - 17, Number of DSL channels = Number + 1.

5.2 MDSL Channel Configuration Registers (18 bytes)

5.2.1 Channel 1

Address: 01

Abbreviation: N1

Read/Write

Table 27. Timeslot to Channel 1

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.2 Channel 2

Address: 02

Abbreviation: N2

Read/Write

Table 28. Timeslot to Channel 2

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.3 Channel 3

Address: 03

Abbreviation: N3

Read/Write

Table 29. Timeslot to Channel 3

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.4 Channel 4

Address: 04

Abbreviation: N4

Read/Write

Table 30. Timeslot to Channel 4

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.5 Channel 5

Address: 05

Abbreviation: N5

Read/Write

Table 31. Timeslot to Channel 5

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.6 Channel 6

Address: 06

Abbreviation: N6

Read/Write

Table 32. Timeslot to Channel 6

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.7 Channel 7

Address: 07

Abbreviation: N7

Read/Write

Table 33. Timeslot to Channel 7

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.8 Channel 8

Address: 08

Abbreviation: N8

Read/Write

Table 34. Timeslot to Channel 8

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.9 Channel 9

Address: 09

Abbreviation: N9

Read/Write

Table 35. Timeslot to Channel 9

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.10 Channel 10

Address: 0A

Abbreviation: N10

Read/Write

Table 36. Timeslot to Channel 10

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.11 Channel 11

Address: 0B

Abbreviation: N11

Read/Write

Table 37. Timeslot to Channel 11

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.12 Channel 12

Address: 0C

Abbreviation: N12

Read/Write

Table 38. Timeslot to Channel 12

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.13 Channel 13

Address: 0D

Abbreviation: N13

Read/Write

Table 39. Timeslot to Channel 13

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.14 Channel 14

Address: 0E

Abbreviation: N14

Read/Write

Table 40. Timeslot to Channel 14

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.15 Channel 15

Address: 0F

Abbreviation: N15

Read/Write

Table 41. Timeslot to Channel 15

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.16 Channel 16

Address: 10

Abbreviation: N16

Read/Write

Table 42. Timeslot to Channel 16

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.17 Channel 17

Address: 11

Abbreviation: N17

Read/Write

Table 43. Timeslot to Channel 17

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.2.18 Channel 18

Address: 12

Abbreviation: N18

Read/Write

Table 44. Timeslot to Channel 18

Bit	Name	Default	Description
<7,6>	CH_CFG	0	Channel configuration: 00 codec, 01 Idle code, 10 PCM, 11 Async data
<5:0>	TS	0	PCM timeslot, valid values 0 - 63.

5.3 Reserved Registers (3 bytes)

Addresses: 13 - 15

Abbreviation: RSVR1-3

Table 45. Reserved Registers

Bit	Name	Default	Description
<7:0>	RSRV1-3	-	Not valid for read or write.

5.4 Wander Reduction Register

Addresses: 16

Abbreviation: WANDER

Read/Write

Table 46. Wander Reduction Register

Bit	Name	Default	Description
<7:0>	W_ENABLE	0	0 = disable wander reduction circuit; 24h = enable wander reduction circuit.

5.5 FIFO/Miscellaneous Control Register

Addresses: 17

Abbreviation: FIFO_MISC

Read/Write

Table 47. FIFO/Miscellaneous Control Register

Bit	Name	Default	Description
<7:6>	SAPCLKDIV	00b	Async serial port clock select, 0 = MCLK/2, 1 = MCLK/4, 2 = MCLK/8, 3 = MCLK/16.
5	TX8KSSEL	0	Transmit 8 KHz reference sync select control. 0 = TX reference sync selected from PCM interface, 1 = TX reference sync selected from codec interface.
4	REMOTE_LB	0	Remote Loopback select. Controls the scrambling polynomial for remote loopback. 0 = normal operation, 1 = remote loopback.
3	PDOE_SEL	0	PCM data output enable select. Default value of 0 causes pin to be FRMSYNC12 for codec operation. Set to 1 to create the output enable signal PDOE for PCM usage. PDOE goes high for programmed PCM time slots in the Nx registers.
2	DXFIFORXT	0	DX FIFO reset control. The DX elastic store FIFO is reset on a 0 to a 1 transition. The 0 or 1 state must be active for a minimum of 3 BITCLK periods.
1	MXFIFORXT	0	MX FIFO reset control. The MX elastic store FIFO is reset on a 0 to a 1 transition. The 0 or 1 state must be active for a minimum of 3 BITCLK periods.
0	FIX2BSTUF	0	Fixed 2-bit stuffing mode enable; 0 = disable, 1 = enable.

5.6 Slip Buffer Lower Threshold Register

Address: 18

Abbreviation: SLP_THDL

Read/Write

Table 48. Slip Buffer Lower Threshold

Bit	Name	Default	Description
<7>	SLP_L_EN	0	0 = Use default, 1 = Enable and use Bits <6:0> for the Lower Threshold. Must be set when Stopped (Run/Stop = 0).
<6:0>	SLP_LWR	0	MPC Mode: Lower Threshold of PCM Receive Slip Buffer (Default 31-N). HWC Mode: Not Used.

5.7 Slip Buffer Upper Threshold Register

Address: 19

Abbreviation: SLP_THDH

Read/Write

Table 49. Slip Buffer Upper Threshold

Bit	Name	Default	Description
<7>	SLP_U_EN	0	0 = Use default, 1 = Enable and use Bits <6:0> for the Upper Threshold. Must be set when Stopped (Run/Stop = 0).
<6:0>	SLP_UPR	0	MPC Mode: Upper Threshold of PCM Receive Slip Buffer (Default 32+N). HWC Mode: Not Used.

5.8 Version Register

Address: 1A

Abbreviation: VERSION

Read only

Table 50. Version

Bit	Name	Default	Description
<7:0>	VER	0	Version of Device.

5.9 Internal Clock Control Registers (4 bytes)

5.9.1 ADPLL Control 1

Address: 1B

Abbreviation: PLLCTL1

Read/Write

Table 51. ADPLL Control 1

Bit	Name	Default	Description
<7:0>	CFREQ(17:10)	40	Center Frequency of the ADPLL.

5.9.2 ADPLL Control 2

Address: 1C

Abbreviation: PLLCTL2

Read/Write

Table 52. ADPLL Control 2

Bit	Name	Default	Description
<7:0>	CFREQ(9:2)	0	Center Frequency of the DPPL.

5.9.3 ADPLL Control 3

Address: 1D

Abbreviation: PLLCTL3

Read/Write

Bit	Name	Default	Description
<7:6>	CFREQ(1:0)	0	Center Frequency of the DPPL.
<5>	AUTO_RST	0	1 = the ADPLL automatically resets the RX FIFO after lock. 0 = No Reset.
<4:0>	KLOOP(4:0)	9	ADPLL Loop Filter Gain Setting.

5.9.4 MCLK Divide

Address: 1E

Abbreviation: PROG_DIV

Read/Write

Table 53. PROG Divide

Bit	Name	Default	Description
<7:0>	PROG_DIV	07	PROG Divide, pre-scaler for PCM and codec Interfaces, PrescaleOut = MCLK/(MCLK_DIV + 1).

5.10 Programmable Idle Code Byte

Address: 1F

Abbreviation: IDLE

Read/Write

Table 54. Programmable Idle Code Byte

Bit	Name	Default	Description
<7:0>	IDLE <7:0>	FFh	Programmable idle code. This 8 bit code contains the bit used for channel blocking.

5.11 PCM Configuration Registers

5.11.1 PCM1 Configuration

Address: 20

Abbreviation: PCM_CFG1

Read/Write

Table 55. PCM 1 Configuration Bits

Bit	Name	Default	Description
7	PCLKMODE	0	Set to '0' for 1x clock, set to '1' for 2x clock.
<6:5>	PCLKMUX	10b	PCM Clock Mux 00 External Pin, PCLK pin-14 (PCM Slave) 01 Internal ADPLL (PCM Master) 10 MCLK divided by PROG_DIV register 11 ADPLL output divided by PROG_DIV register
4	DCE	0	Data clock edge, 0 = sample input data on falling edge - output data on rising edge, 1 = sample input on rising edge - output data on falling edge.
3	FINV	0	Frame Sync Pulse polarity, 0 = Active low, 1 = Active high.
2	FE	0	Frame Clock Edge, 0 = sample frame sync on falling edge - output on rising edge, 1 = sample frame sync on rising edge - output on falling edge.
1	SBBP	1	Slip buffer ByPass, 0 = Slip buffer active, 1 = Slip buffer bypassed.
0	TFI	0	Tri-state for IDLE code, 0 = pass IDLE to PCM, 1 = Tri-state PCM for IDLE.

5.11.2 PCM2 Configuration

Address: 21

Abbreviation: PCM_CFG2

Read/Write

Table 56. PCM 2 Configuration Bits

Bit	Name	Default	Description
7	T1E1/PCM	0	T1E1 - PCM selection, 0 = PCM mode, 1 = T1E1 mode.
6	T1E1	1	T1/E1 selection, 0 = T1 frame mode, 1 = E1 frame mode.
<5:0>	MAXPCHN	1Fh	Max Number of PCM Channels, values 0 - 63, MAXPCHN + 1 = n PCM channels between PCM sync pulses.

5.12 Codec Configuration Register

Address: 22

Abbreviation: COD_CFG

Read/Write

Table 57. Codec Configuration

Bit	Name	Default	Description
<7:6>	CCLKMUX	10b	Codec Clock Mux 00 External Pin, PCLK pin-14 01 Internal ADPLL 10 MCLK divided by PROG_DIV register 11 ADPLL output divided by PROG_DIV register
<0:5>	MAXCCHN	1Fh	Max Number of codec channels, values 0 - 31, MAXCCHN + 1 = n codec channels between codec sync pulses.

5.13 Overhead Registers (25 bytes)

5.13.1 Miscellaneous Control

Address: 23

Abbreviation: MISC_CTL

Read/Write

Table 58. Miscellaneous Control

Bit	Name	Default	Description
<7:6>	LOS_SEL	00b	LOS Select, for outgoing MX direction 00 set LOS based on PCLK 01 set LOS based on codec clock 10 disable LOS; set ‘1’ to LOSD on TX DSL frame 11 enable LOS, for testing; set ‘0’ to LOSD on TX DSL frame
5	CCLKMODE	0	Set to ‘0’ for 1x clock, set to ‘1’ for 2x clock.

Table 58. Miscellaneous Control (Continued)

Bit	Name	Default	Description
4	GAP_CLK	0	Gapped DSL Clock Out Select, Enable output for gapped receive DSL clock. 0 = output always high, 1 = Gapped clock out.
3	Z_CTL	0	Z bit Mux control, 1 = Z bits to registers (Z_NUM = 0 only), 0 = Z bits to OSIO.
2	ASPSEL	0	ADPI serial port select enable. 0 = disabled, 1 = enabled. Enabling the ADPI disables codec frame syncs 7, 8, 9, and 10.
1	CCLK_OE	0	Codec Clock Output Enable. 0 = disabled, 1 = enabled.
0	PCM_FS_POS	1	PCM Frame Sync Position: 0 = first bit of the frame, 1= last bit of the frame.

5.13.2 Overhead Configuration

Address: 24

Abbreviation: OVRHD_CFG

Read/Write

Table 59. Overhead Configuration

Bit	Name	Default	Description
7	Par/Ser	0	Overhead Data Mode: set to ‘0’ for external pins, ‘1’ for internal register.
6	Trans/PreDef	0	‘1’ for transparent mode, ‘0’ for limited pre-defined mode.
5	CRC_CNT	0	CRC-6 error counter mode: ‘0’ for reset when read, ‘1’ for modulo count.
4	FEBE_CNT	0	FEBE error counter mode: ‘0’ for reset when read, ‘1’ for modulo count.
3	L/R	0	Local/Remote Mode, ‘0’ for Remote, ‘1’ for Local, selects scrambling polynomial.
2	SRC_EN	0	Scrambler Enable, ‘0’ enabled, ‘1’ disabled.
1	DSL_LB	0	DSL Interface Loop Back, ‘0’ disabled, ‘1’ enabled.
0	RUN/STOP	0	0 = Set MDSL framer state machine to Deactivated state, 1 = Set MDSL framer state machine to Activation state.

5.13.3 CRC Error Counter

Address: 25

Abbreviation: CRC_ERR_CNT

Read/Write

Table 60. CRC Error Counter

Bit	Name	Default	Description
<7:0>	CRC_ERR_ CNT <7:0>	0	CRC error counter, mode set by CRC mode bit in OVRHD_CFG register.

5.13.4 FEBE Error Counter

Address: 26

Abbreviation: FEBE_ERR_CNT

Read/Write

Table 61. FEBE Error Counter

Bit	Name	Default	Description
<7:0>	FEBE_ERR_ CNT <7:0>	0	FEBE error counter, mode set by FEBE mode bit in OVRHD_CFG register.

5.13.5 CRC - FEBE - LOS Status

Address: 27

Abbreviation: CRC_FEBE_ST

Read/Write

Table 62. CRC - FEBE Status

Bit	Name	Default	Description
7	CRC_OVR	0	'1' when CRC error counter overflowed in reset mode. Must write '1' to reset.
6	FEBE_OVR	0	'1' when FEBE error counter overflowed in reset mode. Must write '1' to reset.
5	CRCERRINJ	0	CRC Error Injection; when this bit is set to '1' a CRC will be injected, then the LXP730 will clear this bit after 1 DSL frame.
4	MX_LOS	0	'1' when LOS occurs, affected by LOS_SEL in MISC_CTL.
<3:1>	n/a	000b	Reserved.
0	DSLACTIVE	0	DSL link active status -- reports current status.

5.13.6 MX Overhead Bits 1 - 8

Address: 28

Abbreviation: MXOH1

Read/Write

Table 63. MX Overhead Bits 1 - 8

Bit	Name	Default	Description
7	mx8/crc2	0	Transparent mode/ Pre defined mode.
6	mx7/crc1	0	Transparent mode/ Pre defined mode.
<5:2>	mx<6:3>	00b	User definable.
1	mx2/febe	0	Transparent mode/ Pre defined mode.
0	mx1/los	0	Transparent mode/ Pre defined mode.

5.13.7 MX Overhead Bits 9 - 16

Address: 29

Abbreviation: MXOH2

Read/Write

Table 64. MX Overhead Bits 9 - 16

Bit	Name	Default	Description
<7:0>	mx<16:9>	0	User definable.

5.13.8 MX Overhead Bits 17 - 24

Address: 2A

Abbreviation: MXOH3

Read/Write

Table 65. MX Overhead Bits 17 - 24

Bit	Name	Default	Description
<7:2>	mx<24:19>	0	User definable.
1	mx18/crc4	0	Transparent mode/ Pre defined mode.
0	mx17/crc3	0	Transparent mode/ Pre defined mode.

5.13.9 MX Overhead Bits 25 - 32

Address: 2B

Abbreviation: MXOH4

Read/Write

Table 66. MX Overhead Bits 25 - 32

Bit	Name	Default	Description
<7:6>	mx<32,31>	00b	User definable.
5	mx30/indcr	0	Transparent mode/ Pre defined mode.
4	mx29	0	User definable.
3	mx28/crc6	0	Transparent mode/ Pre defined mode.
2	mx27/crc5	0	Transparent mode/ Pre defined mode.
<0:1>	mx<25,26>	00b	User definable.

5.13.10 MX Z Bits 1 - 8

Address: 2C

Abbreviation: MXZ1

Read/Write

Table 67. MX Z Bits 1 - 8

Bit	Name	Default	Description
<7:0>	mxz<8:1>	0	User definable when not in T1 mode.

5.13.11 MX Z Bits 9 - 16

Address: 2D

Abbreviation: MXZ2

Read/Write

Table 68. MX Z Bits 9 - 16

Bit	Name	Default	Description
<7:0>	mxz<16:9>	0	User definable when not in T1 mode.

5.13.12 MX Z Bits 17 - 24

Address: 2E

Abbreviation: MXZ3

Read/Write

Table 69. MX Z Bits 17 - 24

Bit	Name	Default	Description
<7:0>	mxz<17:24>	0	User definable when not in T1 mode.

5.13.13 MX Z Bits 25 - 32

Address: 2F

Abbreviation: MXZ4

Read/Write

Table 70. MX Z Bits 25 - 32

Bit	Name	Default	Description
<7:0>	mxz<32:25>	0	User definable when not in T1 mode.

5.13.14 MX Z Bits 33 - 40

Address: 30

Abbreviation: MXZ5

Read/Write

Table 71. MX Z Bits 33 - 40

Bit	Name	Default	Description
<7:0>	mxz<40:33>	0	User definable when not in T1 mode.

5.13.15 MX Z Bits 41 - 48

Address: 31

Abbreviation: MXZ6

Read/Write

Table 72. MX Z Bits 41 - 48

Bit	Name	Default	Description
<7:0>	mxz<48:41>	0	User definable when not in T1 mode.

5.13.16 DX Overhead Bits 1 - 8

Address: 32

Abbreviation: DXOH1

Read/Write

Table 73. DX Overhead Bits 1 - 8

Bit	Name	Default	Description
7	dx8/crc2	0	Transparent mode/ Pre defined mode.
6	dx7/crc1	0	Transparent mode/ Pre defined mode.
<5:2>	dx<6:3>	0000b	User definable.
1	dx2/febe	0	Transparent mode/ Pre defined mode.
0	dx1/los	0	Transparent mode/ Pre defined mode.

5.13.17 DX Overhead Bits 9 - 16

Address: 33

Abbreviation: DXOH2

Read/Write

Table 74. DX Overhead Bits 9 - 16

Bit	Name	Default	Description
<7:0>	dx<16:9>	0	User definable.

5.13.18 DX Overhead Bits 17 - 24

Address: 34

Abbreviation: DXOH3

Read/Write

Table 75. DX Overhead Bits 17 - 24

Bit	Name	Default	Description
<7:2>	dx<24:19>	0	User definable.
1	dx18/crc4	0	Transparent mode/ Pre defined mode.
0	dx17/crc3	0	Transparent mode/ Pre defined mode.

5.13.19 DX Overhead Bits 25 - 32

Address: 35

Abbreviation: DXOH4

Read/Write

Table 76. DX Overhead Bits 25 - 32

Bit	Name	Default	Description
<7:6>	dx<32,31>	00b	User definable.
5	dx30/indcr	0	Transparent mode/ Pre defined mode.
4	dx29	0	User definable.
3	dx28/crc6	0	Transparent mode/ Pre defined mode.
2	dx27/crc5	0	Transparent mode/ Pre defined mode.
<0:1>	dx<25,26>	00b	User definable.

5.13.20 DX Z Bits 1 - 8

Address: 36

Abbreviation: DXZ1

Read/Write

Table 77. DX Z Bits 1 - 8

Bit	Name	Default	Description
<7:0>	dxz<8:1>	0	User definable when not in T1 mode.

5.13.21 DX Z Bits 9 - 16

Address: 37

Abbreviation: DXZ2

Read/Write

Table 78. DX Z Bits 9 - 16

Bit	Name	Default	Description
<7:0>	dxz<16:9>	0	User definable when not in T1 mode.

5.13.22 DX Z Bits 17 - 24

Address: 38

Abbreviation: DXZ3

Read/Write

Table 79. DX Z Bits 17 - 24

Bit	Name	Default	Description
<7:0>	dxz<17:24>	0	User definable when not in T1 mode.

5.13.23 DX Z Bits 25 - 32

Address: 39

Abbreviation: DXZ4

Read/Write

Table 80. DX Z Bits 25 - 32

Bit	Name	Default	Description
<7:0>	dxz<32:25>	0	User definable when not in T1 mode.

5.13.24 DX Z Bits 33 - 40

Address: 3A

Abbreviation: DXZ5

Read/Write

Table 81. DX Z Bits 33 - 40

Bit	Name	Default	Description
<7:0>	dxz<40:33>	0	User definable when not in T1 mode.

5.13.25 DX Z Bits 41 - 48

Address: 3B

Abbreviation: DXZ6

Read/Write

Table 82. DX Z Bits 41 - 48

Bit	Name	Default	Description
<7:0>	dxz<48:41>	0	User definable when not in T1 mode.

5.14 Reserved Registers (2 bytes)

Addresses: 3C and 3D

Abbreviation: RSVR4 and 5

Table 83. Reserved Registers

Bit	Name	Default	Description
<7:0>	RSRV4,5	-	Not valid for read or write.

5.15 Interrupt Registers (2 bytes)

5.15.1 Interrupt Enables

Address: 3E

Abbreviation: INT_EN

Read/Write

Table 84. Interrupt Enables

Bit	Name	Default	Description
7	LOS_EN	0	Loss of source interrupt enable (set to ‘1’ to enable).
6	CRC_FEBE_EN	0	CRC - FEBE interrupt enable.
5	INDCR_EN	0	indcr interrupt enable.
4	SLIP_DET_ EN	0	Slip detect interrupt enable.
3	OHMX_EN	0	Overhead MX interrupt enable.
2	OHDX_EN	0	Overhead DX interrupt enable.
1	ACTIVE_EN	0	ACTIVE interrupt enable.
0	COFA_EN	0	COFA interrupt enable.

5.15.2 Interrupt Status

Address: 3F

Abbreviation: INT_STAT

Read/Write

Table 85. Interrupt Status

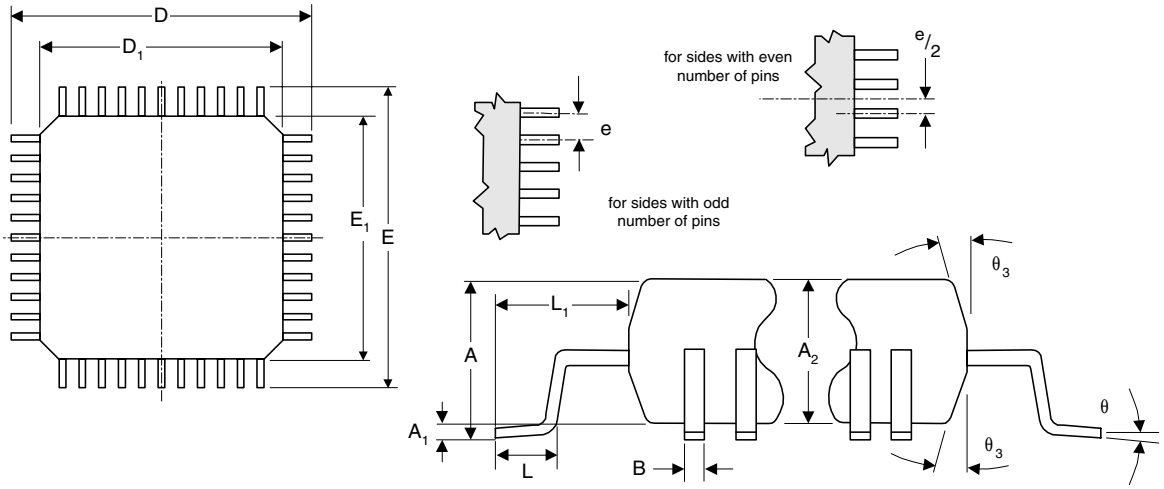
Bit	Name	Default	Description
7	LOS	0	loss of source interrupt, set to ‘1’ when los is received in dx1/los.
6	CRC_FEBE	0	CRC - FEBE interrupt, set to ‘1’ when 1.) CRC error is detected in DX, or 2.) febe is received in dx2/febe.
5	INDCR	0	indcr interrupt, set to ‘1’ when indcr is received in dx30/indcr.
4	SLIP_DET	0	Slip detect interrupt, set to ‘1’ when slip occurs in slip buffer.
3	OHMX	0	Overhead MX interrupt, set to ‘1’ when MX frame has started allowing 6ms to write MX registers before start of next frame.
2	OHDX	0	Overhead DX interrupt, set to ‘1’ when DX frame has ended allowing 6ms to read DX registers before end of next frame.
1	ACTIVE	0	ACTIVE interrupt, set to ‘1’ when MDSL link is up.
0	COFA	0	COFA interrupt, set to ‘1’ when change of frame position occurs.

6.0 Mechanical Specifications

Figure 26. 64 - Pin LQFP Package Specification

Part Number LXP730LE

- 64-pin Low Profile Quad Flat Pack
- Extended Temperature Range (-40 to +85° C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A		.063	–	1.60
A_1	.002	.006	0.05	0.15
A_2	.053	.057	1.35	1.45
b	.007	.011	0.17	0.27
D	0.472 BSC[1]		12.00 BSC[1]	
D_1	0.394 BSC[1]		10.00 BSC[1]	
E	0.472 BSC[1]		12.00 BSC[1]	
E_1	0.394 BSC[1]		10.00 BSC[1]	
e	0.020 BSC[1]		0.50 BSC[1]	
L	0.018	0.030	0.45	0.75
L_1	0.039 REF		1.00 REF	
q_3	11°	13°	11°	13°
q	0°	7°	0°	7°