PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH52CV256HT-10LL

256K SRAM

(Model No.: LH52C5V1)

Spec No.: MS-J080X04

Issue Date: October 18, 1996

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● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

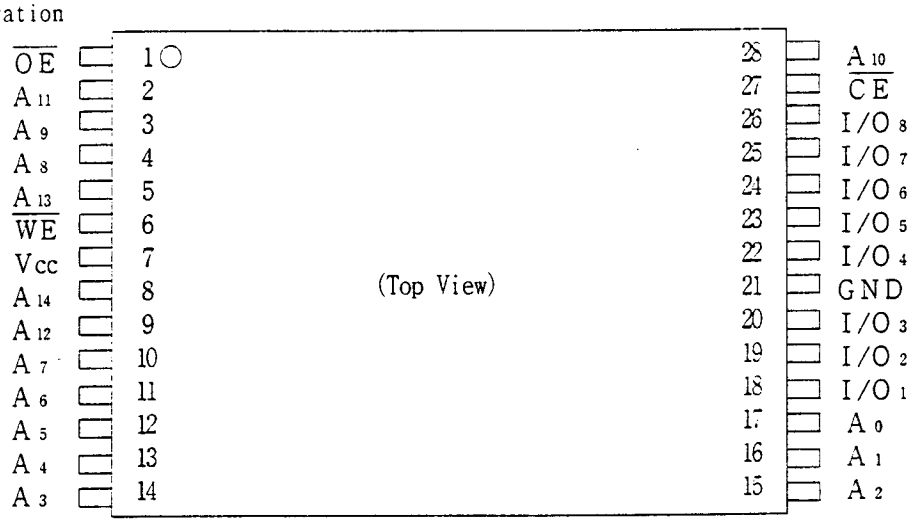
1. Description

The LH52CV256HT-10LL is a static RAM organized as 32,768×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

- ○Access Time ···· 100 ns (Max.)
- ○Operating current ···· 15 mA (Max.)
  ···· 5 mA (Max. t_{RC}, t_{WC} = 1 μs)
- ○Standby current ···· 25 μA (Max.)
- ○Data retention current ···· 1.0 μA (Max. V_{CCDR} = 3.0V, Ta = 25℃)
- ○Single power supply ···· 2.7V to 3.6V
- ○Operating temperature ···· −40℃ to +85℃
- ○Fully static operation
- ○Three-state output
- ○Not designed or rated as radiation hardened
- ○28 pin TSOP (TSOP28-P-0813) plastic package
- ○N-type bulk silicon

2. Pin Configuration



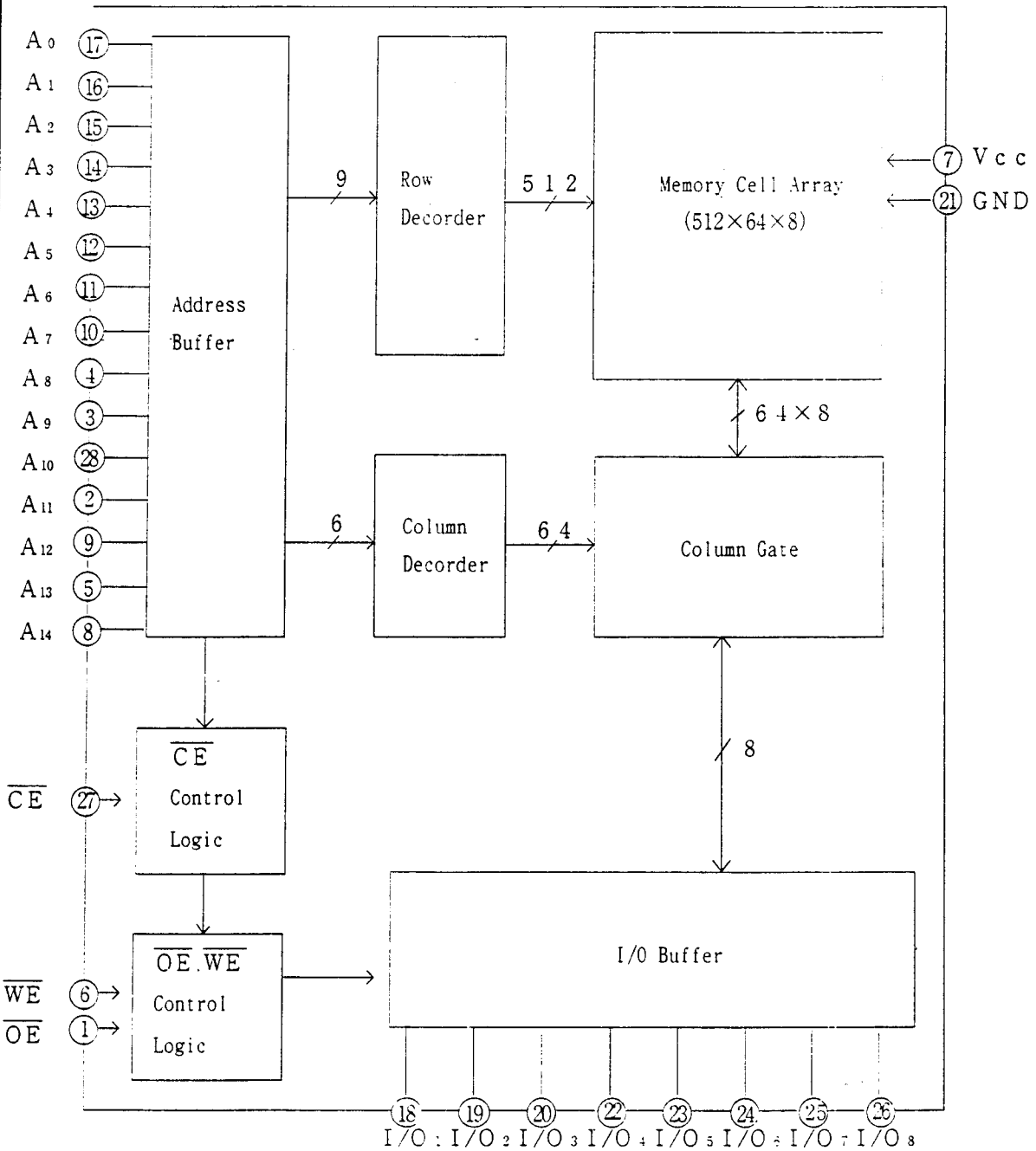
Pin Name	Function
A_0 to A_{14}	Address inputs
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
Vcc	Power supply
GND	Ground

3. Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1 to I/O8	Supply current
H	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	Read	Data output	Active (I_{CC})
L	H	H	Output disable	High impedance	Active (I_{CC})
L	L	*	Write	Data Input	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram



5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.5 to +7.0	V
Input voltage (*1)	V_{IN}	−0.5 (*2) to V_{CC}+0.3	V
Operating temperature	T_{opr}	−40 to +85	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pluse bellow 50ns.

6. Recommended DC Operating Conditions

(T_a= −40℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.2		V_{CC}+0.3	V
	V_{IL}	−0.3 (*3)		0.4	V

Note) *3. Undershoot of −3.0V is allowed width of pluse below 50ns.

7. DC Electrical Characteristics

(T_a= −40℃ to +85℃, V_{CC}= 2.7V to 3.6V)

Parameter	Symbol	Conditions	Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN} =0V to V_{CC}	−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$ =V_{IH} or $\overline{OE}$ =V_{IH} $V_{I/O}$ =0V to V_{CC}	−1.0		1.0	μA
Operating supply current	I_{CC}	Minimum cycle V_{IN} =V_{IL} or V_{IH}, $I_{I/O}$ =0mA, $\overline{CE}$ =V_{IL}		10	15	mA
		t_{RC}, t_{WC} =1μs V_{IN} =V_{IL} or V_{IH}, $I_{I/O}$ =0mA, $\overline{CE}$ =V_{IL}			5	mA
Standby current	I_{SB}	$\overline{CE}$ ≧V_{CC}−0.2V		0.3	25	μA
	I_{SB1}	$\overline{CE}$ =V_{IH}			2	mA
Output voltage	V_{OL}	I_{OL} = 0.5mA			0.4	V
	V_{OH}	I_{OH} =−0.5mA	2.4			V

Note) *4. Typical values at V_{CC}=3.0V, T_a=25℃.

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.4V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5V
Output load	C_L (100pF) (*5)

Note) *5. Including scope and jig capacitance.

Read cycle

(Ta= −40℃ to +85℃, Vcc= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
$\overline{CE}$ access time	t_{ACE}		100	ns	
Output enable to output valid	t_{OE}		60	ns	
Output hold from address change	t_{OH}	15		ns	
$\overline{CE}$ Low to output active	t_{LZ}	15		ns	*6
$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*6
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	35	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	35	ns	*6

Write cycle

(Ta= −40℃ to +85℃, Vcc= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	100		ns	
$\overline{CE}$ Low to end of write	t_{CW}	80		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pluse width	t_{WP}	75		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	40		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output active	t_{OW}	5		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	35	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	35	ns	*6

Note) *6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

9. Data Retention Characteristics

(Ta= −40℃ to +85℃)

Paramenter	Symbol	Conditions		Min.	Typ. (*7)	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geqq V_{CCDR}-0.2V$		2.0		3.6	V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=3V$	Ta=25℃		0.3	1.0	μA
			Ta=70℃			15	μA
		$\overline{CE} \geqq V_{CCDR}-0.2V$				20	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			5			ms

Note) *7. Typical values at Ta=25℃

10. Pin Capacitance

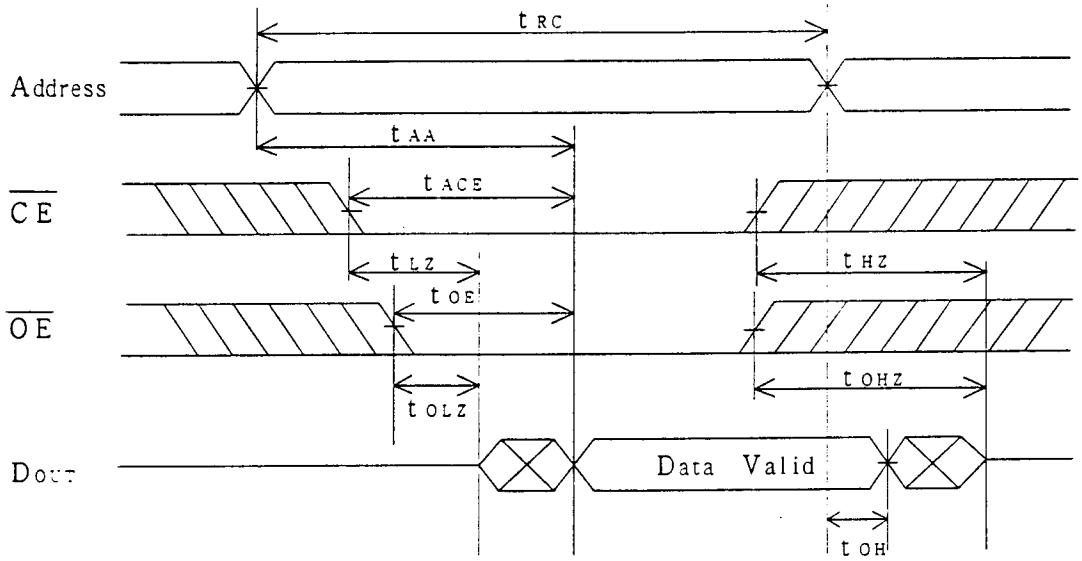
(Ta=25℃, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN}=0V$			8	pF	*8
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$			10	pF	*8

Note) *8. This parameter is sampled and not production tested.

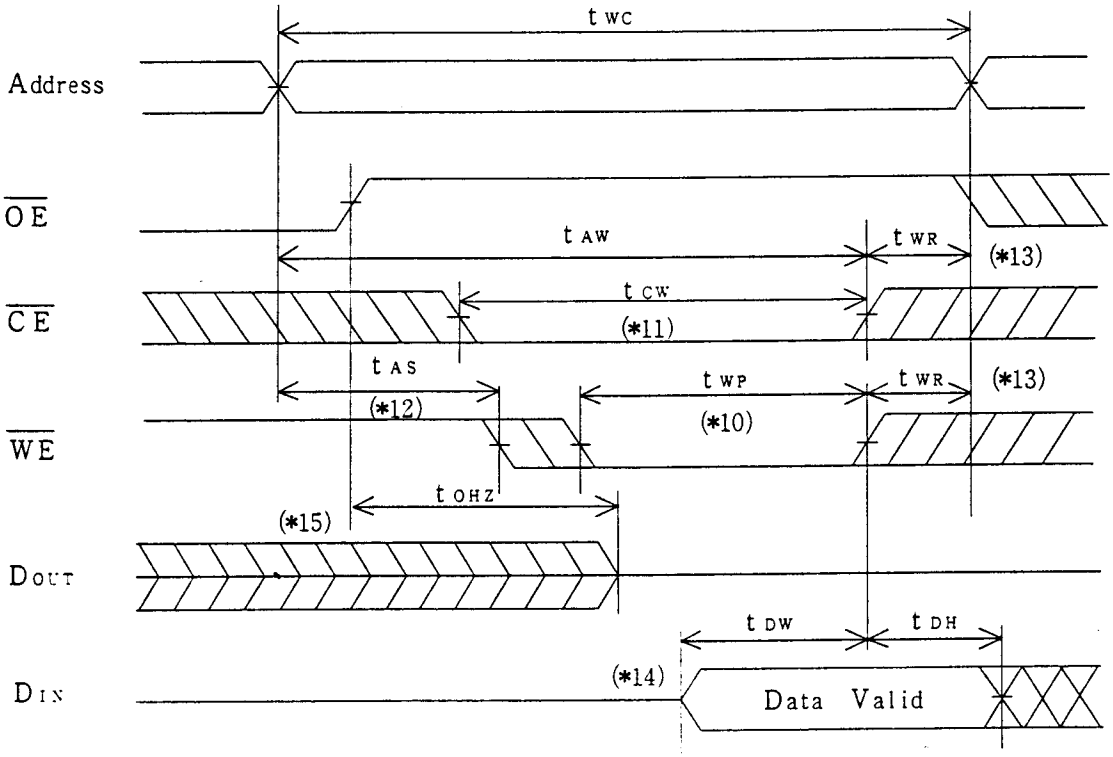
11. Timing Chart

Read cycle timing chart— (＊9)

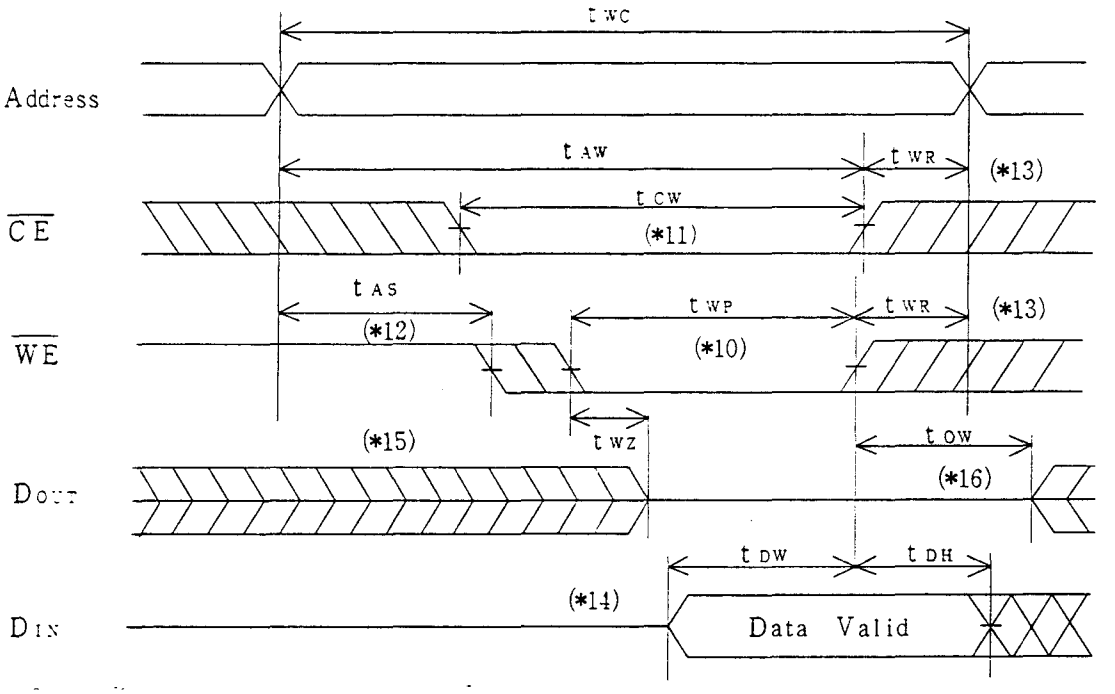


Note) ＊9. $\overline{WE}$ is high for Read cycle.

Write cycle timing chart— ($\overline{OE}$ Controlled)



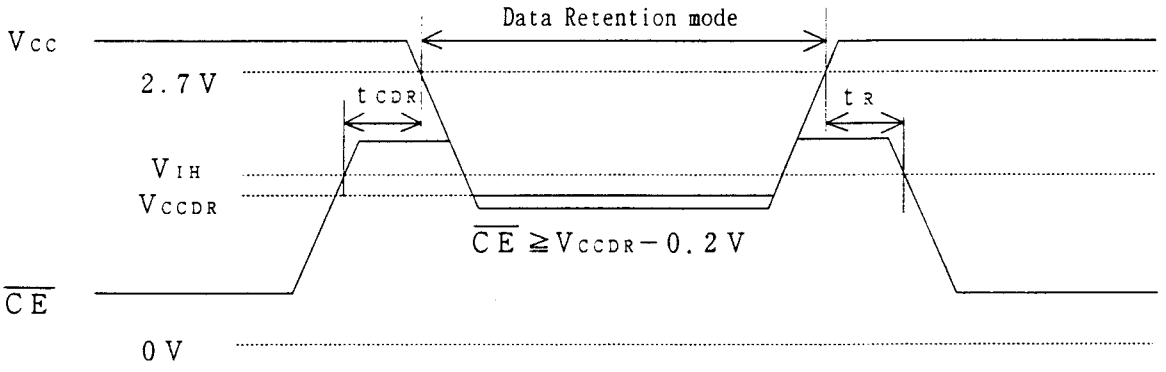
Write cycle timing chart — ($\overline{OE}$ Low fixed)



Note) * 10. A write occurs during the overlap of a low $\overline{CE}$, and a low $\overline{WE}$.
A write begins at the latest transition among $\overline{CE}$ going low, and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE}$ going high, and $\overline{WE}$ going high.
t_{WP} is measured from the beginning of write to the end of write.

* 11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.
* 12. t_{AS} is measured from the address valid to the beginning of write.
* 13. t_{WR} is measured from the end of write to the address change.
* 14. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
* 15. If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
* 16. If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart— $\overline{CE}$ Controlled)



STATIC SRAM RAM Random Access Memory 3V TSOP Industrial Temp LowVoltage Low Power LH52CV256HT10LL 256K