LH51V2008
2M SRAM

FEATURES

- Access time 85 ns (MAX.)
- Operating current
  - 40 mA (MAX.)
  - 5 mA (MAX. t_{RC}, t_{WC} = 1 µs)
- Standby current 45 µA (MAX.)
- Data retention current 1.0 µA (TYP. V_{CCDR} = 3 V, T_A = 25°C)
- Single power supply 2.7 V to 3.6 V
- Operating temperature
  - Wide -25°C to +85°C
  - Industrial -40°C to +85°C
- Fully static operation
- Three-state output
- Not designed or rated as radiation hardened
- Packaging
  - 32-pin TSOP (TSOP32-P-0813) plastic package
  - 32-pin CSP (CSP32-P-0610) plastic package
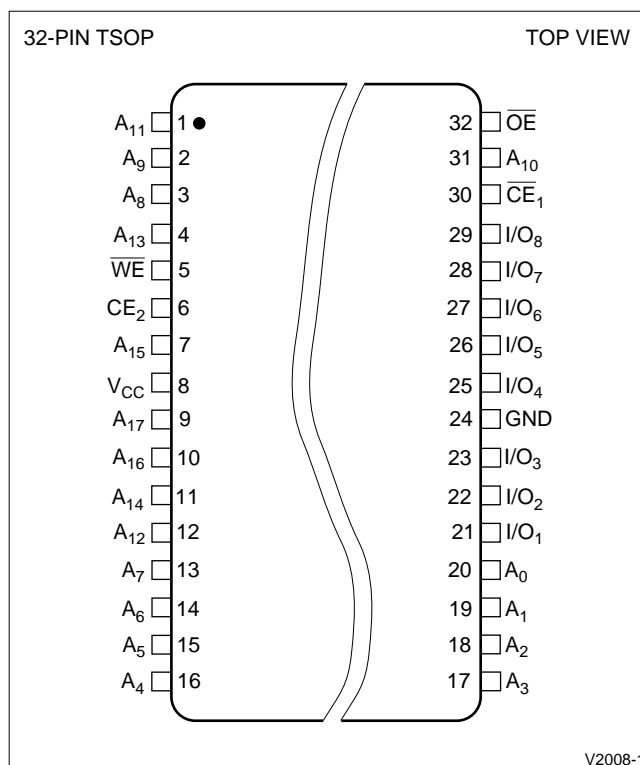- P-type bulk silicon

DESCRIPTION

The LH51V2008 is a static RAM organized as 262,144 × 8-bit which provides low-power standby mode.

It is fabricated using silicon-gate CMOS process technology.

PIN DESCRIPTION

PIN	DESCRIPTION
A_0 to A_{17}	Address Inputs
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1 - I/O_8	Data Inputs/Outputs
V_{CC}	Power Supply
GND	Ground
NC	Non Connection

32-PIN TSOP PINOUT

32-PIN TSOP — TOP VIEW

Pin	Signal		Pin	Signal
1	A_{11}		32	$\overline{OE}$
2	A_9		31	A_{10}
3	A_8		30	$\overline{CE}_1$
4	A_{13}		29	I/O_8
5	$\overline{WE}$		28	I/O_7
6	CE_2		27	I/O_6
7	A_{15}		26	I/O_5
8	V_{CC}		25	I/O_4
9	A_{17}		24	GND
10	A_{16}		23	I/O_3
11	A_{14}		22	I/O_2
12	A_{12}		21	I/O_1
13	A_7		20	A_0
14	A_6		19	A_1
15	A_5		18	A_2
16	A_4		17	A_3

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32-PIN CSP PINOUT

TOP VIEW

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