PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LRS1314

Stacked Chip

8M (×16) Flash Memory and 1M (×16) SRAM

(Model No.: LRS1314)

Spec No.: MFM2-J10307
Issue Date: March 18, 1998

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● Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

Part 1 Product Overview

Part 2 Flash Memory Specifications

Part 3 SRAM Specifications

The contents described in Part 1 take first priority over Part 2 and Part 3.

Part 1 Overview

1.Description

The LRS1314 is a combination memory organized as 524,288×16 bit flash memory and 65,536×16 bit static RAM in one package.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time

Flash memory access time	· · · ·	150 ns Max.	
SRAM access time	· · · ·	85 ns Max.	

○Operating current

Flash memory	Read	· · · ·	25 mA Max.	(t_{CYCLE}=200ns)
	Word write	· · · ·	57 mA Max.	(F-Vcc≧3.0V)
	Block erase	· · · ·	42 mA Max.	(F-Vcc≧3.0V)
SRAM	Operating	· · · ·	25 mA Max.	(t_{CYCLE}=200ns)

○Standby current

Flash memory	· · · ·	20 μA Max.	(F-$\overline{CE}$≧F-V_{CC}-0.2V, F-$\overline{RP}$≦0.2V, F-V_{PP}≦0.2V)
SRAM	· · · ·	25 μA Max.	(S-$\overline{CE}$≧S-V_{CC}-0.2V)
		0.3 μA Typ.	(Ta=25℃, S-V_{CC}=3V, S-$\overline{CE}$≧S-Vcc-0.2V)

(Total standby current is the summation of Flash memory's standby current and SRAM's one.)

○Power supply	· · · ·	2.7V to 3.6V	(Read, SRAM write)
	· · · ·	3.0V to 3.6V	(Flash erase/write)

(Block erase and word write operations with V_{CC}<3.0V in Flash memory are not supported.)

○Operating temperature	· · · ·	-25℃ to +85℃

○Fully static operation

○Three-state output

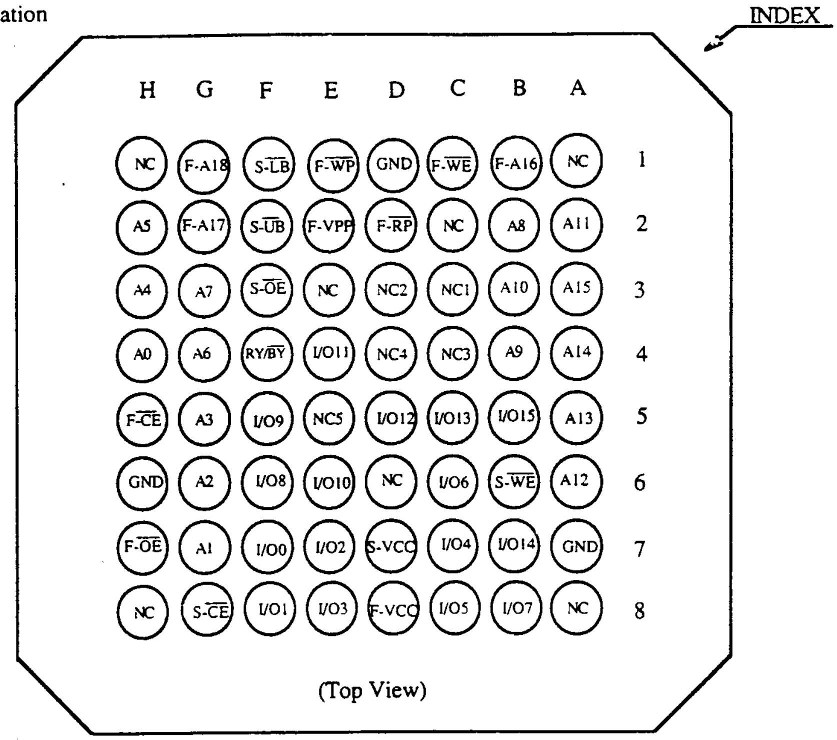
○Not designed or rated as radiation hardened

○ 64pin CSP (LCSP064-P-0808) plastic package

○Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

The contents described in Part 1 take first priority over Part 2 and Part 3.

2.Pin Configuration



	H	G	F	E	D	C	B	A
1	NC	F-A18	S-$\overline{\text{LB}}$	F-$\overline{\text{WP}}$	GND	F-$\overline{\text{WE}}$	F-A16	NC
2	A5	F-A17	S-$\overline{\text{UB}}$	F-VPP	F-$\overline{\text{RP}}$	NC	A8	A11
3	A4	A7	S-$\overline{\text{OE}}$	NC	NC2	NC1	A10	A15
4	A0	A6	RY/$\overline{\text{BY}}$	I/O11	NC4	NC3	A9	A14
5	F-$\overline{\text{CE}}$	A3	I/O9	NC5	I/O12	I/O13	I/O15	A13
6	GND	A2	I/O8	I/O10	NC	I/O6	S-$\overline{\text{WE}}$	A12
7	F-$\overline{\text{OE}}$	A1	I/O0	I/O2	S-VCC	I/O4	I/O14	GND
8	NC	S-$\overline{\text{CE}}$	I/O1	I/O3	F-VCC	I/O5	I/O7	NC

(Top View)

Note: From NC_1 to NC_5 are needed to be open.

PIN	DESCRIPTION
A_0 to A_{15}	Common Address Input Pins
F-A_{16} to F-A_{18}	Address Input Pins for Flash Memory
F-$\overline{\text{CE}}$	Chip Enable Input Pin for Flash Memory
S-$\overline{\text{CE}}$	Chip Enable Input Pin for SRAM
F-$\overline{\text{WE}}$	Write Enable Input Pin for Flash Memory
S-$\overline{\text{WE}}$	Write Enable Input Pin for SRAM
F-$\overline{\text{OE}}$	Output Enable Input Pin for Flash Memory
S-$\overline{\text{OE}}$	Output Enable Input Pin for SRAM
I/O_0 to I/O_{15}	Common Data Input/Output Pins
F-$\overline{\text{RP}}$	Reset/Deep Power Down Input Pin for Flash Memory
F-$\overline{\text{WP}}$	Write Protect Pin for Flash Memrory's Boot Block
F-V_{CC}	Power Supply Pin for Flash Memory
F-V_{PP}	Power Supply Pin for Flash Memory Write/Erase
S-V_{CC}	Power Supply Pin for SRAM
GND	Common GND
RY/$\overline{\text{BY}}$	Ready/Busy Output Pin for Flash Memory
S-$\overline{\text{LB}}$	Write Enable Input (I/O_0 to I/O_7)
S-$\overline{\text{UB}}$	Write Enable Input (I/O_8 to I/O_{15})
NC	Non Conect
NC_1 to NC_5	Non Conect (Should be open)

The contents described in Part 1 take first priority over Part 2 and Part 3.

3. Notes

This product is a stacked CSP package that a 8M(x16) bit Flash Memory and a 1M(x16) bit SRAM are assembled into.

POWER SUPPLY AND CHIP ENABLE OF FLASH MEMORY AND SRAM

It is forbidden that both F-$\overline{\text{CE}}$ and S-$\overline{\text{CE}}$ should be LOW simultaneously. If the two memories are active together, possibly they may not operate normally by interference noises or data collision on I/O bus. Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time.

SRAM DATA RETENTION

SRAM data retention is capable in three ways as below. SRAM power switching between a system battery and a backup battery needs careful device decoupling from Flash Memory to prevent SRAM supply voltage from falling lower than 2.0V by a Flash Memory peak current caused by transition of Flash Memory supply voltage or of control signals (F-$\overline{\text{CE}}$, F-$\overline{\text{OE}}$ and $\overline{\text{RP}}$).

CASE 1: FLASH MEMORY IS IN STANDBY MODE. (F-V_{CC}=2.7V to 3.6V)

- SRAM inputs and input/outputs except S-$\overline{\text{CE}}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).
- Flash Memory inputs and input/outputs except F-$\overline{\text{CE}}$ and $\overline{\text{RP}}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).

CASE 2: FLASH MEMORY IS IN DEEP POWER DOWN MODE. (F-V_{CC}=2.7V to 3.6V)

- SRAM inputs and input/outputs except S-$\overline{\text{CE}}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open.
- Flash Memory inputs and input/outputs except $\overline{\text{RP}}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z). $\overline{\text{RP}}$ is needed to be at the same level as F-V_{CC} or to be open.

CASE 3: FLASH MEMORY POWER SUPPLY IS TURNED OFF. (F-V_{CC}=0V)

- Fix $\overline{\text{RP}}$ LOW level before turning off Flash memory power supply.
- SRAM inputs and input/outputs except S-$\overline{\text{CE}}$ are needed to be applied with voltages in the range of -0.3V to S-V_{CC}+0.3V or to be open(High-Z).
- Flash Memory inputs and input/outputs except $\overline{\text{RP}}$ are needed to be at GND or to be open(High-Z).

POWER UP SEQUENCE

When turning on Flash memory power supply, keep $\overline{\text{RP}}$ LOW. After F-V_{CC} reaches over 2.7V, keep $\overline{\text{RP}}$ LOW for more than 100nsec.

DEVICE DECOUPLING

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals(F-$\overline{\text{CE}}$, S-$\overline{\text{CE}}$).

4.Truth table(*1,3)

F-$\overline{\text{CE}}$	F-$\overline{\text{OE}}$	F-$\overline{\text{WE}}$	F-$\overline{\text{RP}}$	S-$\overline{\text{CE}}$	S-$\overline{\text{OE}}$	S-$\overline{\text{WE}}$	Address	Mode	I/O_0 toI/O_{15}	Current	Note
L	L	H	H	H	X	X	X	Flash read	Output	I_{CC}	*2,7,8
L	H	H	H	H	X	X	X	Flash read	High-Z	I_{CC}	*8
L	H	L	H	H	X	X	X	Flash write	Input	I_{CC}	*5,6,7,8
H	X	X	X	L	L	H	X	SRAM read	Output	I_{CC}	
H	X	X	X	L	H	H	X	SRAM read	High-Z	I_{CC}	
H	X	X	X	L	X	L	X	SRAM write	Input	I_{CC}	
H	X	X	H	H	X	X	X	Standby	High-Z	I_{SB}	*8
H	X	X	L	H	X	X	X	Deep power down	High-Z	I_{SB}	*4

(X=Don't Care, L=Low, H=High)

Notes:

∗1. Do not make F-$\overline{\text{CE}}$ and S-$\overline{\text{CE}}$ "LOW" level at the same time.

∗2. Refer to DC Characteristics. When F-$V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.

∗3. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for F-V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH} voltages.

∗4. F-$\overline{\text{RP}}$ at GND ± 0.2V ensures the lowest deep power-down current.

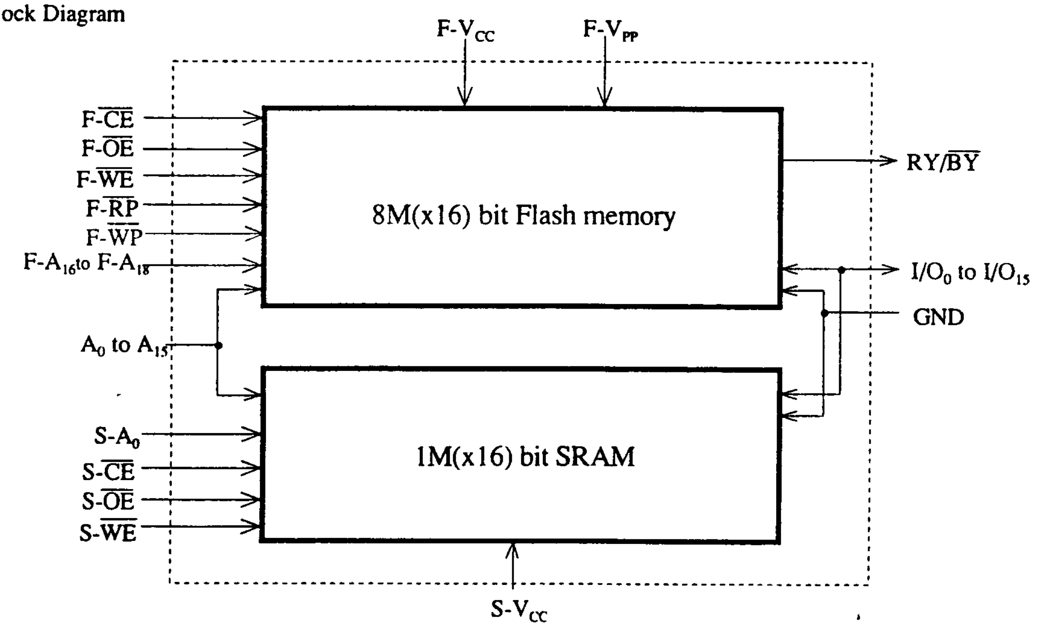
∗5. Command writes involving block erase, write, or lock-bit configuration are reliably executed when F-V_{PP}=V_{PPH} and F-V_{CC}=V_{CC2}. Block erase, byte write, or lock-bit configuration with F-V_{CC}<3.0V or V_{IH}<F-$\overline{\text{RP}}$<V_{HH} produce spurious results and should not be attempted.

∗6. Refer to Part 2 Section 3 Table 4 for valid DIN during a write operation.

∗7. Do not use in a timing that both F-$\overline{\text{OE}}$ and F-$\overline{\text{WE}}$ is "LOW" level.

∗8. RY/$\overline{\text{BY}}$ is V_{OL} when the WSM is executing internal block erase byte write, or lock-bit configuration algorityhms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode(with byte write inactive), byte write suspend mode, or deep power-down mode.

5. Block Diagram



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6.Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*9,10)	V_{CC}	-0.3 to +4.6	V
Input voltage(*9,11)	V_{IN}	-0.3 (*12) to V_{CC}+0.3	V
Operating temperature	T_{opr}	-25 to +85	℃
Storage temperature	T_{stg}	-65 to +125	℃
V_{PP} voltage(*9)	V_{PP}	-0.2 to +12.6 (*13)	V
Input voltage(*9)	$\overline{RP}$	-0.5 (*12) to +12.6 (*13)	V

Notes) ∗9.The maximum applicable voltage on any pin with respect to GND.

∗10. Except V_{PP}.

∗11. Except $\overline{RP}$.

∗12. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

∗13. +14.0V overshoot is allowed when the pulse width is less than 20nsec.

7.Recommended DC Operating Conditions

(T_a= -25℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		V_{CC}+0.3 (*16)	V
	V_{IL}	-0.3 (*14)		0.8	V
	V_{HH}(*15)	11.4		12.6	V

Notes) ∗14. -2.0V undershoot is allowed when the pulse width is less than 20nsec.

∗15. This voltage is applicable to F-$\overline{RP}$ Pin only.

∗16. V_{CC} is the lower one of S-V_{CC} and F-V_{CC}.

8.Pin Capacitance

(T_a=25℃, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN}=0V			20	pF	*17
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V			22	pF	*17

Note) ∗17. Sampled but not 100% tested

9.DC Electrical Characteristics

(T_a= -25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

Parameter		Note	Conditions		Min.	Typ.(*18)	Max.	Unit
Input leakage current(I_{LI})			V_{IN}=0V to V_{CC}		-1.5		1.5	µA
Output leakage current (I_{LO})			F-$\overline{CE}$, S-$\overline{CE}$=V_{IH} or F-$\overline{OE}$, S-$\overline{OE}$=V_{IH} or F-$\overline{WE}$, S-$\overline{WE}$=V_{IH}, $V_{I/O}$=0V to V_{CC}		-1.5		1.5	µA
Operating supply current (I_{CC})	FLASH	*19	Read current, F-V_{PP}≦F-V_{CC} F-$\overline{CE}$≦0.2V, VIN≧V_{CC}-0.2V or V_{IN}≦0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			25	mA
		*20 *21	Summation of V_{CC} Byte Write or set lock-bit current, and V_{PP} Byte Write or set lock-bit current. F-V_{CC}≧3.0V				57	mA
		*20 *22	Summation of V_{CC} Block Erase or Clear Block lock-bits current, and V_{PP} Block Erase or Clear Block lock-bits current. F-V_{CC}≧3.0V				42	mA
	SRAM	*23	S-$\overline{CE}$=0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			25	mA
Standby current (I_{SB})	FLASH	*24	F-$\overline{CE}$=V_{IH}, $\overline{RP}$=V_{IH}				2.0	mA
		*25	F-$\overline{CE}$≧V_{CC}-0.2V, F-V_{PP}≦0.2V, $\overline{RP}$≦0.2V				20	µA
	SRAM	*26	S-$\overline{CE}$=V_{IH}				3.0	mA
		*27	S-$\overline{CE}$≧V_{CC}-0.2V			0.3	25	µA
Output voltage (V_{OL}, V_{OH})			I_{OL}=2.0mA				0.4	V
			I_{OH}=-1.0mA		2.4			V

Note) ∗18. T_a=25℃, V_{CC}=3.0V
∗19. This value is read current (I_{CCR}+I_{PPR}) of the flash memory.
∗20. Sampled but not 100% tested.
∗21. This value is operation current (I_{CCW}+I_{PPW}) of flash memory.
∗22. This value is operation current (I_{CCE}+I_{PPE}) of flash memory.
∗23. This value is operation current (I_{CC1}) of SRAM.
∗24. This value is stand-by current (I_{CCS}+I_{PPS}) of flash memory.
∗25. This value is deep power down cuurent (I_{CCD}+I_{PPD}) of flash memory.
∗26. This value is stand-by current (I_{SB1}) of SRAM.
∗27. This value is stand-by current (I_{SB}) of SRAM.

PART2 Flash memory
CONTENTS

1 INTRODUCTION

This datasheet contains LRS1314 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 New Features

The LRS1314 Flash memory maintains backwards-compatibility with SHARP's LH28F800BG-L. Key enhancements over the LH28F800BG-L include:

- Enhanced Suspend Capabilities
- Boot Block Architecture
- V_{PPLK} has been lowered from 6.5V to 1.5V to support 3.3V block erase and word write operations. Designs that switch V_{PP} off during read operations should make sure that the V_{PP} voltage transitions to GND.
- Allow V_{PP} connection to 3.3V.

1.2 Product Overview

The LRS1314 is a high-performance 8-Mbit Smart Voltage Flash memory organized as 512 Kword of 16 bits. The 512 Kword of data is arranged in two 4K-word boot blocks, six 4K-word parameter blocks and fifteen 32K-word main blocks which are individually erasable in-system. The memory map is shown in Figure 2.

SmartVoltage technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations

V_{CC} Voltage	V_{PP} Voltage
2.7V to 3.6V(*1)	3.0V to 3.6V

NOTE :
*1. Block Erase and Word Write operations with V_{CC} <3.0V are not supported.

Internal V_{CC} and V_{PP} detection circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase and word write operations.

A block erase operation erases one of the device's 32K-word blocks typically within 1.14sec., 4K-word blocks typically within 0.38sec. independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word increments of the device's 32K-word blocks typically within 44.6µs, 4K-word blocks typically within 45.9µs. Word write suspend mode enables the system to read data or execute code from any other flash memory array location.

The boot block can be locked for the $\overline{WP}$ pin. Block erase or word write for boot block must not be caried out by $\overline{WP}$ to Low and $\overline{RP}$ to V_{IH}.

The status register indicates when the WSM's block erase or word write operation is finished.

The RY/$\overline{BY}$ output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/$\overline{BY}$ minimizes both CPU overhead and system power consumption. When low, RY/$\overline{BY}$ indicates that the WSM is performing a block erase, byte write, or lock-bit configuration. RY/$\overline{BY}$-high indicates that the WSM is ready for a new command, block erase is suspended (and word write is inactive), word write is suspended, or the device is in deep power-down mode.

The access time is 150ns (t_{AVQV}) over the commercial temperature range (-25°C to +85°C) and V_{CC} supply voltage range of 2.7V-3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 1 mA at 3.3V V_{CC}.

When $\overline{CE}$ and $\overline{RP}$ pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the $\overline{RP}$ pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from $\overline{RP}$ switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from $\overline{RP}$-high until writes to the CUI are recognized. With $\overline{RP}$ at GND, the WSM is reset and the status register is cleared.

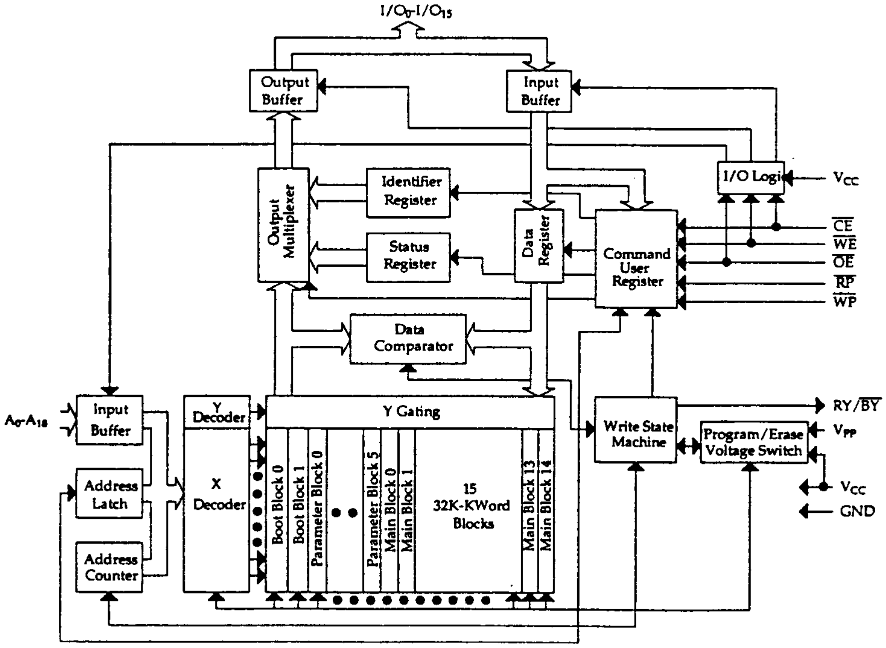


Figure 1. Block Diagram

Table 2. Pin Descriptions

Sym	Type	Name and Function
A_0-A_{18}(*1)	INPUT	ADDRESS INPUTS: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle.
I/O_0-I/O_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI write cycles; outputs data during memory array, status register, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$(*2)	INPUT	CHIP ENABLE: Activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$-high deselects the device and reduces power consumption to standby levels.
$\overline{RP}$	INPUT	RESET/DEEP POWER-DOWN: Puts the device in deep power-down mode and resets internal automation. $\overline{RP}$-high enables normal operation. When driven low, $\overline{RP}$ inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode. Block erase or word write with $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.
$\overline{OE}$(*3)	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
$\overline{WE}$(*4)	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
RY/$\overline{BY}$	OUTPUT	READY/$\overline{BUSY}$: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase or word write). RY/$\overline{BY}$-high indicates that the WSM is ready for new commands, block erase is suspended, and word write is inactive, word write is suspended, or the device is in deep power-down mode. RY/$\overline{BY}$ is always active and does not float when the chip is deselected or data outputs are disabled.
$\overline{WP}$	INPUT	WRITE PROTECT: Master controll for boot blocks locking. When V_{IL}, locked boot blocks cannot be erased and programmed.
V_{PP}(*5)	SUPPLY	BLOCK ERASE and WORD WRITE POWER SUPPLY: For erasing array blocks or writing words. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase and word write with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}(*6)	SUPPLY	DEVICE POWER SUPPLY: Do not float any power pins. With $V_{CC} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	GROUND: Do not float any ground pins.

NOTES:

*1. A_{16}, A_{17}, A_{18} mean F-A_{16}, F-A_{17} and F-A_{18} in the Part 1.
*2. $\overline{CE}$ means F-$\overline{CE}$ in the Part 1.
*3. $\overline{OE}$ means F-$\overline{OE}$ in the Part 1.
*4. $\overline{WE}$ means F-$\overline{WE}$ in the Part 1.
*5. V_{PP} means F-V_{PP} in the Part 1.
*6. V_{CC} means F-V_{CC} in the Part 1.

2 PRINCIPLES OF OPERATION

The LRS1314 Flash memory includes an on-chip WSM to manage block erase and word write functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, byte write, and lock-bit configuration, and minimal processor overhead with RAM-Like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erasure and word writing. All functions associated with altering memory contents–block erase, byte write, Lock-bit configuration, status, and identifier codes–are accessed via the CUI and verified through the status register.

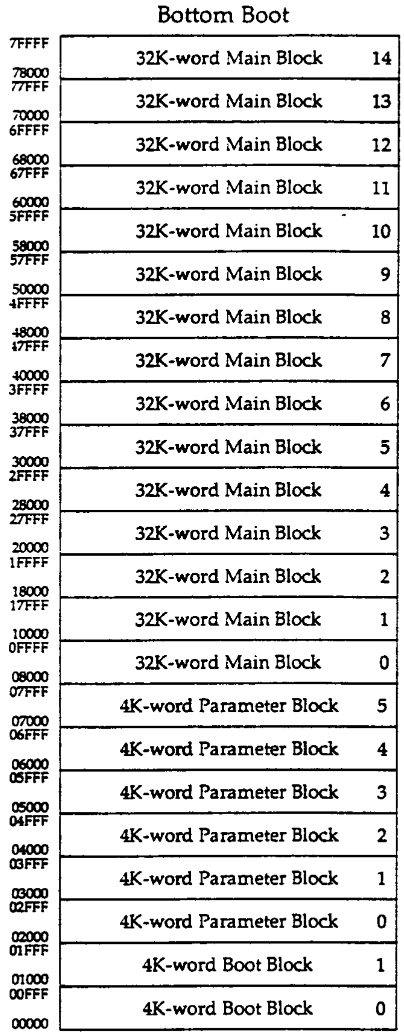
Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase and word write. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, or outputs status register data.

Interface software that initiates and polls progress of block erase and word write can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Word write suspend allows system software to suspend a word write to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when memory block erases or word writes are required) or hardwired to V_{PPH}. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase or word write command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when $\overline{RP}$ is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and word write operations.



Bottom Boot

7FFFF	78000	32K-word Main Block	14
77FFF	70000	32K-word Main Block	13
6FFFF	68000	32K-word Main Block	12
67FFF	60000	32K-word Main Block	11
5FFFF	58000	32K-word Main Block	10
57FFF	50000	32K-word Main Block	9
4FFFF	48000	32K-word Main Block	8
47FFF	40000	32K-word Main Block	7
3FFFF	38000	32K-word Main Block	6
37FFF	30000	32K-word Main Block	5
2FFFF	28000	32K-word Main Block	4
27FFF	20000	32K-word Main Block	3
1FFFF	18000	32K-word Main Block	2
17FFF	10000	32K-word Main Block	1
0FFFF	08000	32K-word Main Block	0
07FFF	07000	4K-word Parameter Block	5
06FFF	06000	4K-word Parameter Block	4
05FFF	05000	4K-word Parameter Block	3
04FFF	04000	4K-word Parameter Block	2
03FFF	03000	4K-word Parameter Block	1
02FFF	02000	4K-word Parameter Block	0
01FFF	01000	4K-word Boot Block	1
00FFF	00000	4K-word Boot Block	0

Figure 2. Memory Map

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, or status register independent of the V_{PP} voltage. $\overline{\text{RP}}$ can be at either V_{IH} or V_{HH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$, $\overline{\text{RP}}$ and $\overline{\text{WP}}$. $\overline{\text{CE}}$ and $\overline{\text{OE}}$ must be driven active to obtain data at the outputs. $\overline{\text{CE}}$ is the device selection control, and when active enables the selected memory device. $\overline{\text{OE}}$ is the data output (I/O_0-I/O_{15}) control and when active drives the selected memory data onto the I/O bus. $\overline{\text{WE}}$ must be at V_{IH} and $\overline{\text{RP}}$ must be at V_{IH} or V_{HH}. Figure 10 illustrates a read cycle.

3.2 Output Disable

With $\overline{\text{OE}}$ at a logic-high level (V_{IH}), the device outputs are disabled. Output pins I/O_0-I/O_{15} are placed in a high-impedance state.

3.3 Standby

$\overline{\text{CE}}$ at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. I/O_0-I/O_{15} outputs are placed in a high-impedance state independent of $\overline{\text{OE}}$ If deselected during block erase or word write, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

$\overline{\text{RP}}$ at V_{IL} initiates the deep power-down mode.

In read modes, $\overline{\text{RP}}$-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. $\overline{\text{RP}}$ must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or word write modes, $\overline{\text{RP}}$-low will abort the operation. RY/$\overline{\text{BY}}$ remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after $\overline{\text{RP}}$ goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert $\overline{\text{RP}}$ during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase or word write modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the $\overline{\text{RP}}$ input. In this application, $\overline{\text{RP}}$ is controlled by the same $\overline{\text{RESET}}$ signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code (see Figure 3). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

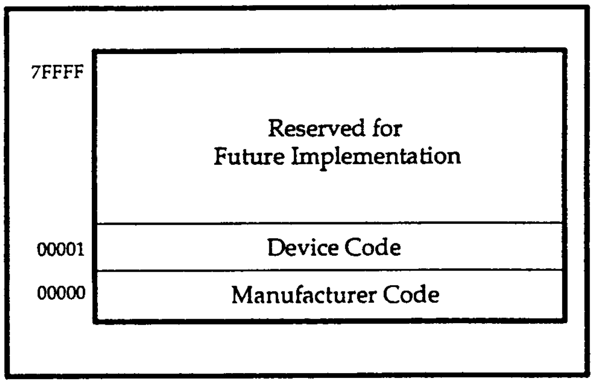


Figure 3. Device Identifier Code Memory Map

3.6 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written.

The CUI does not occupy an addressable memory location. It is written when $\overline{WE}$ and $\overline{CE}$ are active. The address and data needed to execute a command are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first). Standard microprocessor write timings are used. Figures 11 and 12 illustrate $\overline{WE}$ and $\overline{CE}$-controlled write operations.

4 COMMAND DEFINITIONS

When the $V_{PP} \leq V_{PPLK}$, Read operations from the status register, identifier codes, or blocks are enabled. Placing V_{PPH} on V_{PP} enables successful block erase and word write operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3. Bus Operations

Mode	Notes	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Address	V_{PP}	I/O_{0-7}	RY/$\overline{BY}$
Read	*1,2,3,8	V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	*3	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	*3	V_{IH} or V_{HH}	V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	*4	V_{IL}	X	X	X	X	X	High Z	V_{OH}
Read Identifier Codes		V_{IH} or V_{HH}	V_{IL}	V_{IL}	V_{IH}	See Figure 3	X	* 5	V_{OH}
Write	*3,6,3,8	V_{IH} or V_{HH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

*1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.

*2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or V_{PPH} for V_{PP}. See DC Characteristics for V_{PPLK} and V_{PPH} voltages.

*3. RY/$\overline{BY}$ is V_{OL} when the WSM is executing internal block erase or word write algorithms. It is V_{OH} during when the WSM is not busy, in block erase suspend mode (with word write inactive), word write suspend mode, or deep power-down mode.

*4. $\overline{RP}$ at GND±0.2V ensures the lowest deep power-down current.

*5. See Section 4.2 for read identifier code data.

*6. $V_{IH} < \overline{RP} < V_{HH}$ produce spurious results and should not be attempted.

*7. Refer to Table 4 for valid D_{IN} during a write operation.

*8. Don't use the timing both $\overline{OE}$ and $\overline{WE}$ are V_{IL}.

Table 4. Command Definitions(*7)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(*1)	Addr(*2)	Data(*3)	Oper(*1)	Addr(*2)	Data(*3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	*4	Write	X	90H	Read	IA	ID
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	*5	Write	BA	20H	Write	BA	D0H
Word Write	2	*5,6	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	*5	Write	X	B0H			
Block Erase and Word Write Resume	1	*5	Write	X	D0H			

NOTES:

*1. BUS operations are defined in Table 3.

*2. X=Any valid address within the device.
IA=Identifier Code Address: see Figure 3.
BA=Address within the block being erased or locked.
WA=Address of memory location to be written.

*3. SRD=Data read from status register. See Table 7 for a description of the status register bits.
WD=Data to be written at location WA. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ (whichever goes high first).
ID=Data read from identifier codes.

*4. Following the Read Identifier Codes command, read operations access manufacturer, device codes. See Section 4.2 for read identifier code data.

*5. If the block is boot block, $\overline{WP}$ must be at V_{IH} or $\overline{RP}$ must be at V_{HH} to enable block erase or word write operations. Attempts to issue a block erase or word write to a boot block while $\overline{WP}$ is V_{IH} or $\overline{RP}$ is V_{IH}.

*6. Either 40H or 10H are recognized by the WSM as the word write setup.

*7. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and $\overline{RP}$ can be V_{IH} or V_{HH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 3 retrieve the manufacturer and codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and $\overline{RP}$ can be V_{IH} or V_{HH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address	Data
Manufacture Code	00000H	00B0H
Device Code (Top boot)	00001H	0060H
Device Code (Bottom boot)	00001H	0062H

4.3 Read Status Register Command

The status register may be read to determine when a block erase or word write is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs. $\overline{OE}$ or $\overline{CE}$ must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. $\overline{RP}$ can be V_{IH} or V_{HH}.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 7). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurre during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. $\overline{RP}$ can be V_{IH} or V_{HH}. This command is not functional during block erase or word write suspend modes.

4.5 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 4). The CPU can detect block erase completion by analyzing the output data of the RY/$\overline{BY}$ pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that the corresponding, if set, that $\overline{WP}=V_{IH}$ or $\overline{RP}=V_{HH}$. If block erase is attempted when the corresponding $\overline{WP}=V_{IL}$ or $\overline{RP}=V_{IH}$, SR.1 and SR.5 will be set to "1". Block erase operations with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

4.6 Word Write Command

Word write is executed by a two-cycle command sequence. Word write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of $\overline{WE}$). The WSM then takes over, controlling the word write and write verify algorithms internally. After the word write sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect the completion of the word write event by analyzing the RY/$\overline{BY}$ pin or status register bit SR.7.

When word write is complete, status register bit SR.4 should be checked. If word write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word writes can only occur when $V_{CC}=V_{CC2}$ and $V_{PP}=V_{PPH}$. In the absence of this high voltage, memory contents are protected against word writes. If word write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word write for boot blocks requires that the corresponding , if set, that $\overline{WP}=V_{IH}$ or $\overline{RP}=V_{HH}$. If word write is attempted to boot block when the corresponding $\overline{WP}=V_{IL}$ or $\overline{RP}=V_{IH}$, SR.1 and SR.4 will be set to "1". Word write operations with $V_{IH}<\overline{RP}<V_{HH}$ produce spurious results and should not be attempted.

4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/$\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A Word Write command sequence can also be issued during erase suspend to program data in other blocks. Using the Word Write Suspend command (see Section 4.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/$\overline{BY}$ output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/$\overline{BY}$ will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 6). V_{PP} must remain at V_{PPH} (the same V_{PP} level used for block erase) while block erase is suspended. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for block erase). Block erase cannot resume until word write operations initiated during block erase suspend have completed.

4.8 Word Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word write operation has been suspended (both will be set to "1"). RY/$\overline{BY}$ will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After Word Write Resume command is written to the flash memory, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and RY/$\overline{BY}$ will return to V_{OL}. After the Word Write Resume command is written, the device automatically outputs status register data when read (see Figure 7). V_{PP} must remain at V_{PPH} (the same V_{PP} level used for word write) while in word write suspend mode. $\overline{RP}$ must also remain at V_{IH} or V_{HH} (the same $\overline{RP}$ level used for word write). $\overline{WP}$ must also remain V_{IL} or V_{IH} (the same $\overline{WP}$ level used for word write).

Table 6. Write Protection Alternatives

Operation	V_{PP}	$\overline{RP}$	$\overline{WP}$	Effect
Word Write or Block Erase	V_{IL}	X	X	All Blocks Locked.
	>V_{PPLK}	V_{IL}	X	All Blocks Locked.
		V_{HH}	X	All Blocks Unlocked.
		V_{IH}	V_{IL}	2 Boot Blocks Locked.
			V_{IH}	All Blocks Unlocked.

Table 7. Status Register Definition

WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE
1 = Error in Block Erasure
0 = Successful Block Erase

SR.4 = WORD WRITE
1 = Error in Word Write
0 = Successful Word Write

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = WORD WRITE SUSPEND STATUS
1 = Word Write Suspended
0 = Word Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = $\overline{WP}$ and/or $\overline{RP}$ Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

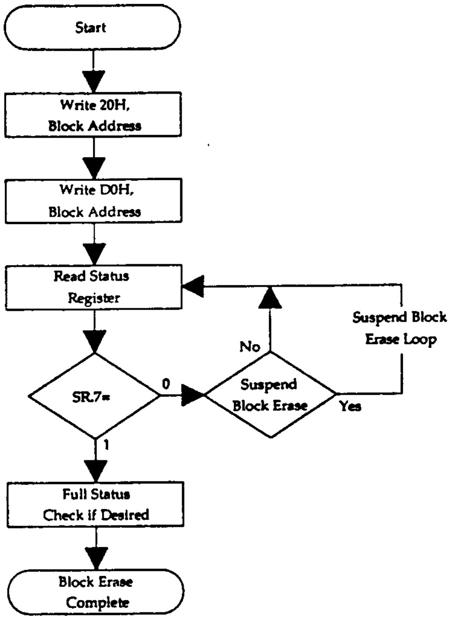
NOTES:

Check RY/$\overline{BY}$ or SR.7 to determine block erase or word write completion.
SR.6-0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase or Word Write command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP}=V_{PPH}$.

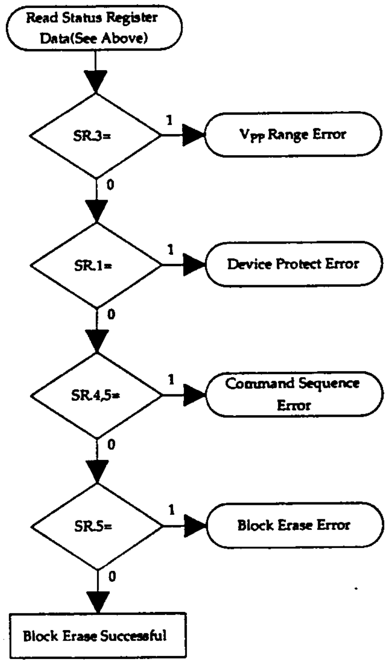
SR.0 is reserved for future use and should be masked out when polling the status register.



Bus Operation	Command	Comments
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

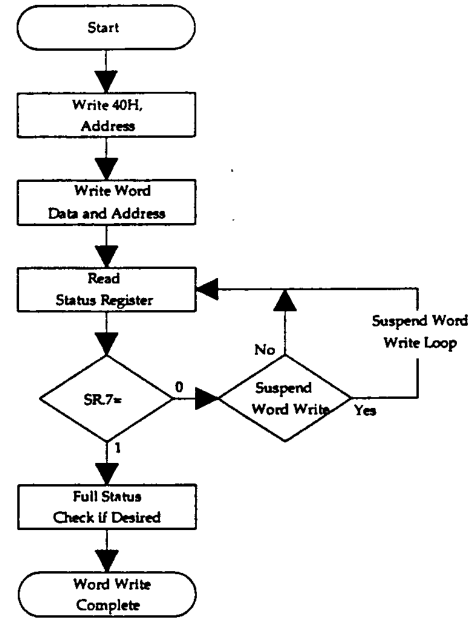
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

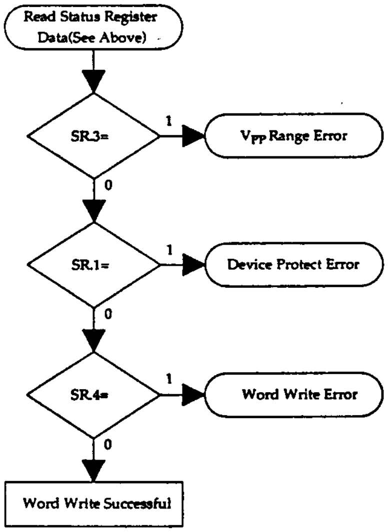
Figure 4. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Setup Word Write	Data=40H Addr=Location to Be Written
Write	Word Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent byte writes..
SR full status check can be done after each byte write, or after a sequence of byte writes.
Write FFH after the last byte write operation to place device in read array mode.

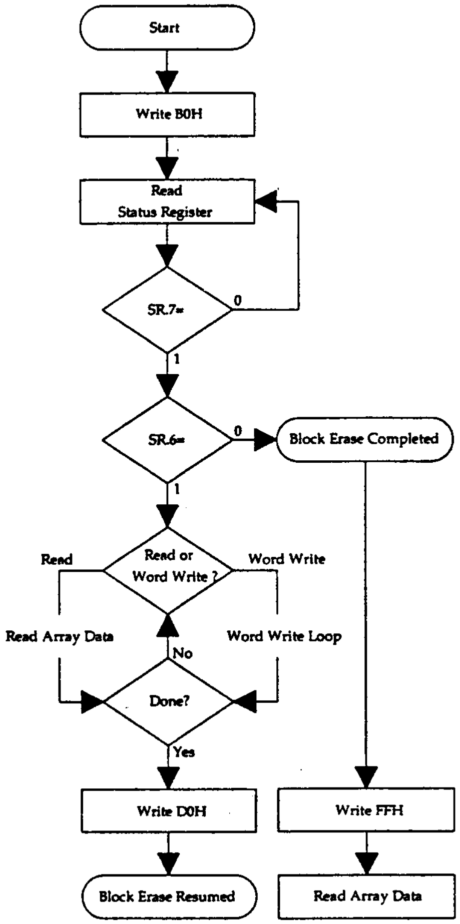
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=Data Write Error

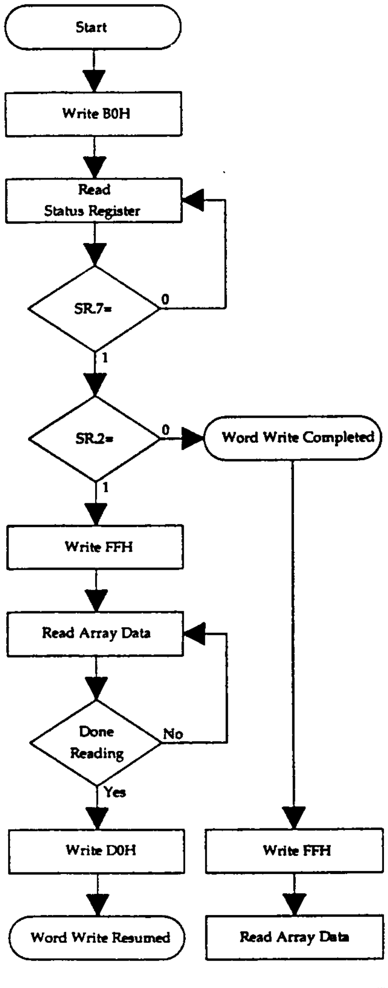
SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 5. Automated Word Write Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 6. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Word Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Word Write Suspended 0=Word Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	Word Write Resume	Data=D0H Addr=X

Figure 7. Word Write Suspend/Resume Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable $\overline{CE}$ while $\overline{OE}$ should be connected to all memory devices and the system's $\overline{READ}$ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. $\overline{RP}$ should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 RY/$\overline{BY}$ and Block Erase and Word Write Polling

RY/$\overline{BY}$ is a full CMOS output that provides a hardware method of detecting block erase and word write completion. It transitions low after block erase or word write commands and returns to V_{OH} when the WSM has finished executing the internal algorithm.

RY/$\overline{BY}$ can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/$\overline{BY}$ is also V_{OH} when the device is in block erase suspend (with word write inactive), word write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of $\overline{CE}$ and $\overline{OE}$. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for word writing and block erasing. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, $\overline{RP}$ Transitions

Block erase and word write are not guaranteed if V_{PP} falls outside of a valid V_{PPH} range, V_{CC} falls outside of a valid V_{CC2} range, or $\overline{RP} \neq V_{IH}$ or V_{HH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If $\overline{RP}$transitions to V_{IL} during block erase or word write, RY/$\overline{BY}$ will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or $\overline{RP}$ transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or $\overline{CE}$ transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase or word write, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure or word writing during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both $\overline{WE}$ and $\overline{CE}$ must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

The device is disabled while $\overline{RP}=V_{IL}$ regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering $\overline{RP}$ to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after $\overline{RP}$ is first raised to V_{IH}. See AC Characteristics–Read Only and Write Operations and Figures 12, 13 and 14 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

<Operating Temprature>
Commercial Products
During Read, Block Erase and
Word Write .... -25°C to +85°C(*1)

<Storage Temperature>....................... -65°C to +125°C

<Voltage On Any Pin>
except V_{CC}, V_{PP}, and $\overline{RP}$ ....-2.0V to +7.0V(*2)
V_{CC} Supply Voltage......................-2.0V to +7.0V(*2)
V_{PP} Update Voltage during
Block Erase and
Word Write .... -2.0V to +14.0V(*2,3)
$\overline{RP}$ Voltage................................ -2.0V to +14.0V(*2,3)

<Output Short Circuit Current> ....100mA(*4)

*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:

*1. Operating temperature is for commercial product defined by this specification.

*2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.

*3. Maximum DC voltage on V_{PP} and $\overline{RP}$ may overshoot to +14.0V for periods <20ns.

*4. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

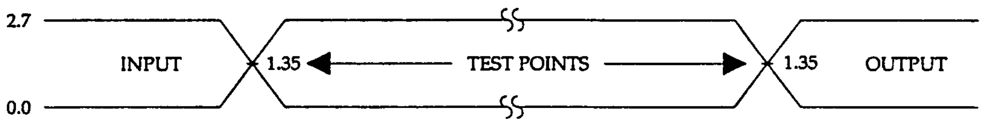
Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		-25	+85	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V-3.6V)	*1	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.0V-3.6V)		3.0	3.6	V	

NOTES:

*1. Block erase and word write operations with V_{CC}<3.0V are not supported.

6.2.1 AC INPUT/OUTPUT TEST CONDITIONS



AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0." Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 ns.

Figure 8. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

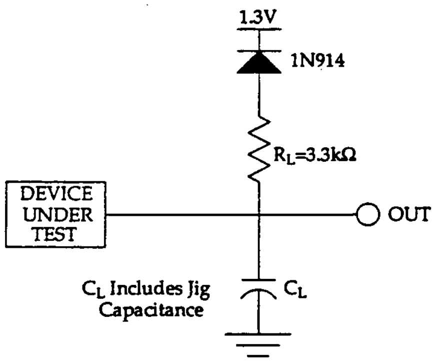


Figure 9. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC}=2.7V to 3.6V	50

6.2.2 DC CHARACTERISTICS

DC Characteristics

Sym	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Typ	Max		
I_{IL}	Input Load Current	*1		±0.5	µA	$V_{CC}=V_{CC}$Max $V_{IN}=V_{CC}$ or GND
I_{OL}	Output Leakage Current	*1		±0.5	µA	$V_{CC}=V_{CC}$Max $V_{OUT}=V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	*1,3, *6	25	50	µA	CMOS Inputs $V_{CC}=V_{CC}$Max $\overline{CE}=\overline{RP}=V_{CC}\pm0.2V$
			0.2	2	mA	TTL Inputs $V_{CC}=V_{CC}$Max $\overline{CE}=\overline{RP}=V_{IH}$
I_{CCD}	V_{CC} Deep Power-Down Current	*1	4	20	µA	$\overline{RP}$=GND±0.2V $I_{OUT}(RY/\overline{BY})$=0mA
I_{CCR}	V_{CC} Read Current	*1, 5 *6	15	25	mA	CMOS Inputs $V_{CC}=V_{CC}$Max, $\overline{CE}$=GND f=5MHz, I_{OUT}=0mA
				30	mA	TTL Inputs $V_{CC}=V_{CC}$Max, $\overline{CE}$=GND f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Word Write Current	*1,7	5	17	mA	$V_{PP}=V_{PPH}$
I_{CCE}	V_{CC} Block Erase Current	*1,7	4	17	mA	$V_{PP}=V_{PPH}$
I_{CCWS} I_{CCES}	V_{CC} Word Write Current	*1,2	1	6	mA	$\overline{CE}=V_{IH}$
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	*1	±2	±15	µA	$V_{PP}\leq V_{CC}$
			10	200	µA	$V_{PP}>V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	*1	0.1	5	µA	$\overline{RP}$=GND±0.2V
I_{PPW}	V_{PP} Word Write Current	*1,7	12	40	mA	$V_{PP}=V_{PPH}$
I_{PPE}	V_{PP} Block Erase Current	*1,7	8	25	mA	$V_{PP}=V_{PPH}$
I_{PPWS} I_{PPES}	V_{PP} Word Write Current	*1	10	200	µA	$V_{PP}=V_{PPH}$

DC Characteristics (Continued)

Sym	Parameter	Notes	V_{CC}=2.7V-3.6V		Unit	Test Conditions
			Min	Max		
V_{IL}	Input Low Voltage	*7	-0.5	0.8	V	
V_{IH}	Input High Voltage	*7	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	*3,7		0.4	V	$V_{CC}=V_{CC}$Min, I_{OL}=2.0mA
V_{OH1}	Output High Voltage (TTL)	*3,7	2.4		V	$V_{CC}=V_{CC}$Min, I_{OH}=-2.0mA
V_{OH2}	Output High Voltage (CMOS)	*3,7	0.85 V_{CC}		V	$V_{CC}=V_{CC}$Min I_{OH}=-2.5mA
			V_{CC} -0.4		V	$V_{CC}=V_{CC}$Min I_{OH}=-100μA
V_{PPLK}	V_{PP} Lockout during Normal Operations	*4,7		1.5	V	
V_{PPH}	V_{PP} during Word Write or Block Erase Operations		3.0	3.6	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		V	
V_{HH}	$\overline{RP}$ Unlock Voltage	*8,9	11.4	12.6	V	Block Erase and Word Write for Boot Blocks

NOTES:

*1. All currents are in RMS unless otherwise noted. Typical values at V_{CC}=3.3V and T_a=+25℃.

*2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.

*3. Includes RY/$\overline{BY}$.

*4. Block erases and word writes are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max) and V_{PPH}(min).

*5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA at 3.3V V_{CC} in static operation.

*6. CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.

*7. Sampled, not 100% tested.

*8. Block erases and word writes are inhibited when the corresponding $\overline{RP}=V_{IH}$. Block erase and word write operations are not guaranteed with V_{CC}<3.0V or $V_{IH}<\overline{RP}<V_{HH}$ and should not be attempted.

*9. $\overline{RP}$ connection to a V_{HH} supply is allowed for a maximum cumulative period of 80 hours.

6.2.3 AC CHARACTERISTICS - READ-ONLY OPERATIONS(*1)

V_{CC}=2.7V-3.6V, T_a=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Read Cycle Time		150		ns
t_{AVQV}	Address to Output Delay			150	ns
t_{ELQV}	$\overline{CE}$ to Output Delay	*2		150	ns
t_{PHQV}	$\overline{RP}$ High to Output Delay			600	ns
t_{GLQV}	$\overline{OE}$ to Output Delay	*2		55	ns
t_{ELQX}	$\overline{CE}$ to Output in Low Z	*3	0		ns
t_{EHQZ}	$\overline{CE}$ High to Output in High Z	*3		55	ns
t_{GLQX}	$\overline{OE}$ to Output in Low Z	*3	0		ns
t_{GHQZ}	$\overline{OE}$ High to Output in High Z	*3		25	ns
t_{OH}	Output Hold from Address, $\overline{CE}$or $\overline{OE}$ Change, Whichever Occurs First	*3	0		ns

NOTES:

*1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.

*2. $\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{CE}$ without impact on t_{ELQV}.

*3. Sampled, not 100% tested.

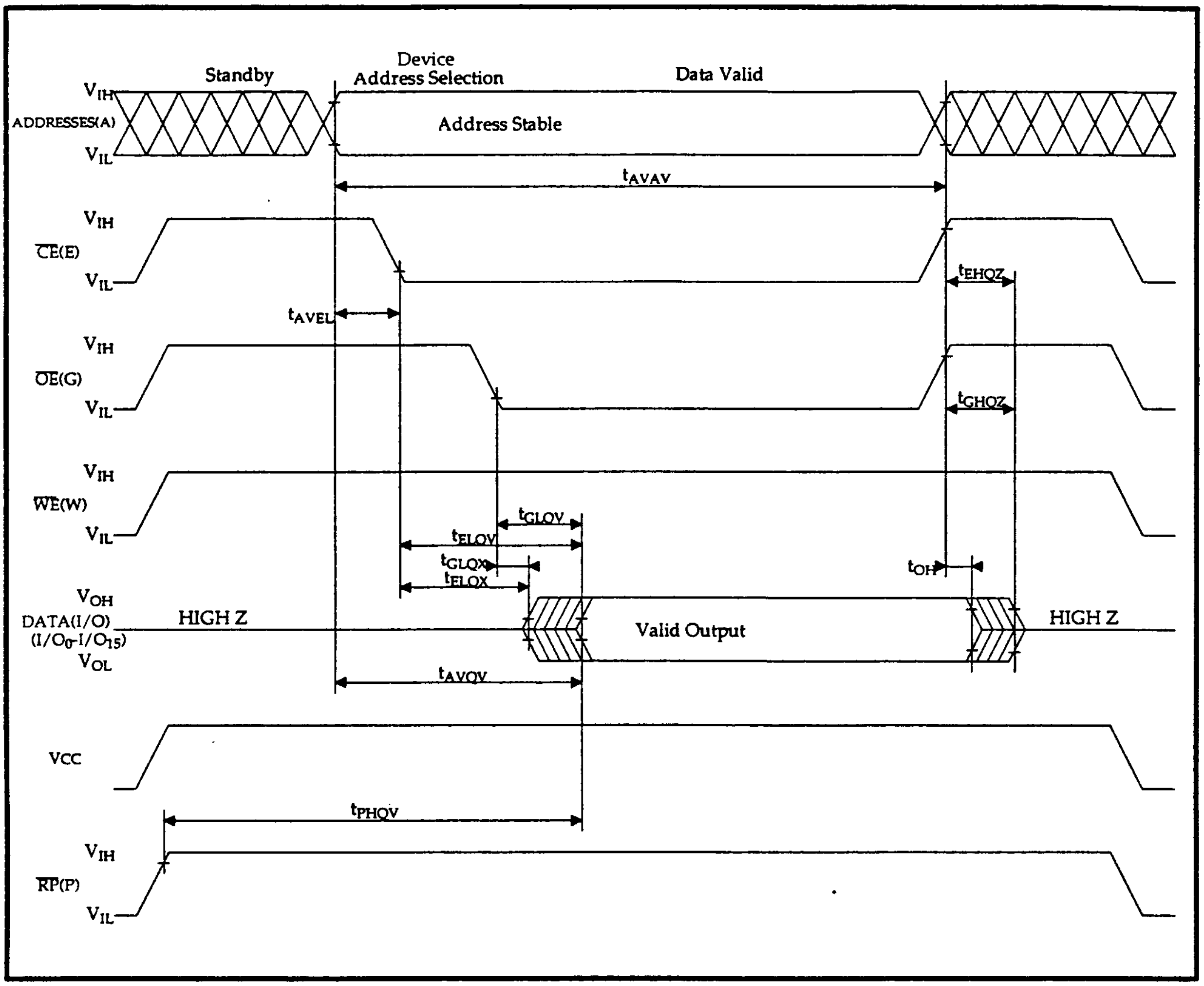


Figure 10. AC Waveform for Read Operations

6.2.4 AC CHARACTERISTICS - WRITE OPERATION(*1)

V_{CC}=2.7V-3.6V, T_a=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		150		ns
t_{PHWL}	$\overline{RP}$ High Recovery to$\overline{WE}$ Going Low	*2	1		µs
t_{ELWL}	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		10		ns
t_{WLWH}	$\overline{WE}$ Pulse Width		50		ns
t_{PHHWH}	$\overline{RP}$ V_{HH} to $\overline{CE}$ Going High	*2	100		ns
t_{SHWH}	$\overline{WP}$ V_{IH} Setup to $\overline{WE}$ Going High	*2	100		ns
t_{VPWH}	V_{PP} Setup to $\overline{WE}$ Going High	*2	100		ns
t_{AVWH}	Address Setup to $\overline{WE}$ Going High	*3	50		ns
t_{DVWH}	Data Setup to $\overline{WE}$ Going High	*3	50		ns
t_{WHDX}	Data Hold from $\overline{WE}$ High		5		ns
t_{WHAX}	Address Hold from $\overline{WE}$ High		5		ns
t_{WHEH}	$\overline{CE}$ Hold from $\overline{WE}$ High		10		ns
t_{WHWL}	$\overline{WE}$ Pulse Width High		30		ns
t_{WHRL}	$\overline{WE}$ High to RY/$\overline{BY}$ Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High	*2,4	0		ns
t_{QVPH}	$\overline{RP}$ V_{HH} Hold from Valid SRD, RY/$\overline{BY}$ High	*2,4	0		ns
t_{QVSL}	$\overline{WP}$ V_{IH} Hold from Valid SRD, RY/$\overline{BY}$ High	*2,4	0		ns

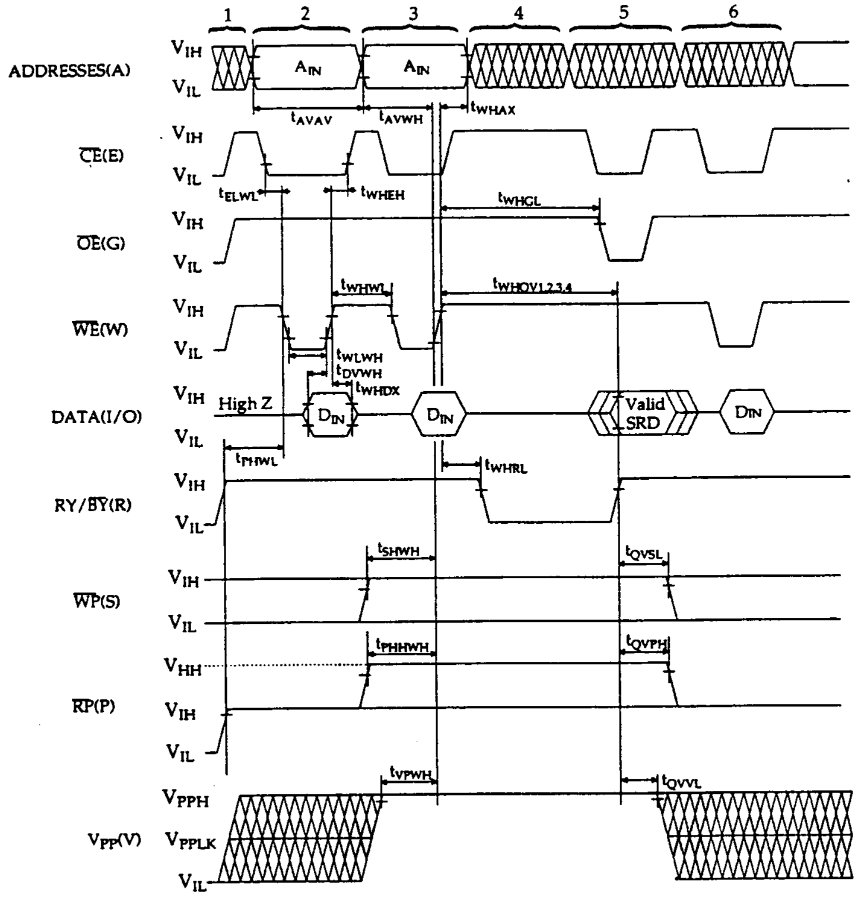
NOTES:

*1. Read timing characteristics during block erase and word write operations are the same as during read-onry operations. Refer to AC Characteristics for read-only operations.

*2. Sampled, not 100% tested.

*3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word write.

*4. V_{PP} should be held at V_{PPH} (and if necessary $\overline{RP}$ should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5=0).



NOTES:

1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 11. AC Waveform for $\overline{\text{WE}}$-Controlled Write Operations

6.2.5 AC CHARACTERISTICS for $\overline{\text{CE}}$-CONTROLLED WRITES OPERATION(*1)

V_{CC}=2.7V-3.6V, T_a=-25°C to +85°C

Sym	Parameter	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		150		ns
t_{PHEL}	$\overline{\text{RP}}$ High Recovery to $\overline{\text{CE}}$ Going Low	*2	1		µs
t_{WLEL}	$\overline{\text{WE}}$ Setup to $\overline{\text{CE}}$ Going Low		0		ns
t_{ELEH}	$\overline{\text{CE}}$ Pulse Width		70		ns
t_{PHHEH}	$\overline{\text{RP}}$ V_{HH} Setup to $\overline{\text{CE}}$ Going High	*2	100		ns
t_{SHEH}	$\overline{\text{WP}}$ V_{IH} Setup to $\overline{\text{CE}}$ Going High	*2	100		ns
t_{VPEH}	V_{PP} Setup to $\overline{\text{CE}}$ Going High	*2	100		ns
t_{AVEH}	Address Setup to $\overline{\text{CE}}$ Going High	*3	50		ns
t_{DVEH}	Data Setup to $\overline{\text{CE}}$ Going High	*3	50		ns
t_{EHDX}	Data Hold from $\overline{\text{CE}}$ High		5		ns
t_{EHAX}	Address Hold from $\overline{\text{CE}}$ High		5		ns
t_{EHWH}	$\overline{\text{WE}}$ Hold from $\overline{\text{CE}}$ High		0		ns
t_{EHEL}	$\overline{\text{CE}}$ Pulse Width High		25		ns
t_{EHRL}	$\overline{\text{CE}}$ High to RY/$\overline{\text{BY}}$ Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{\text{BY}}$ High	*2,4	0		ns
t_{QVPH}	$\overline{\text{RP}}$ V_{HH} Hold from Valid SRD, RY/$\overline{\text{BY}}$ High	*2,4	0		ns
t_{QVSL}	$\overline{\text{WP}}$ V_{IH} Hold from Valid SRD, RY/$\overline{\text{BY}}$ High	*2,4	0		ns

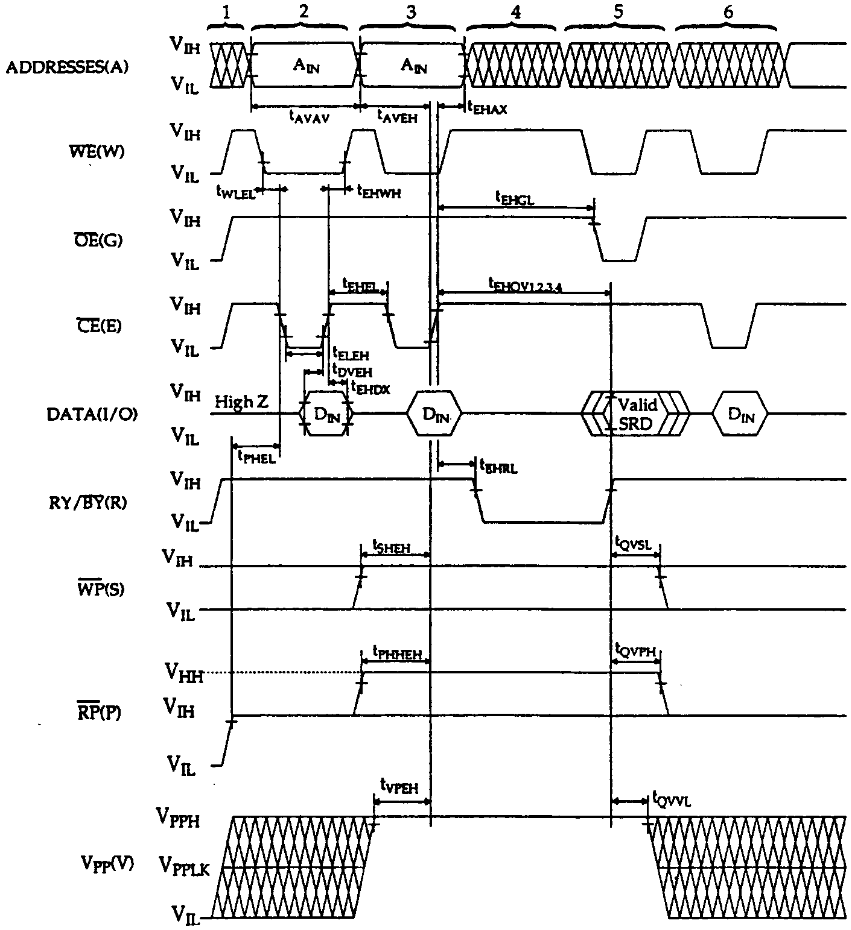
NOTES:

*1. In systems where $\overline{\text{CE}}$ defines the write pulse width (within a longer $\overline{\text{WE}}$ timing waveform), all setup, hold, and inactive $\overline{\text{WE}}$ times should be measured relative to the $\overline{\text{CE}}$ waveform.

*2. Sampled, not 100% tested.

*3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase or word write.

*4. V_{PP} should be held at V_{PPH} (and if necessary $\overline{\text{RP}}$ should be held at V_{HH}) until determination of block erase or word write success (SR.1/3/4/5=0).

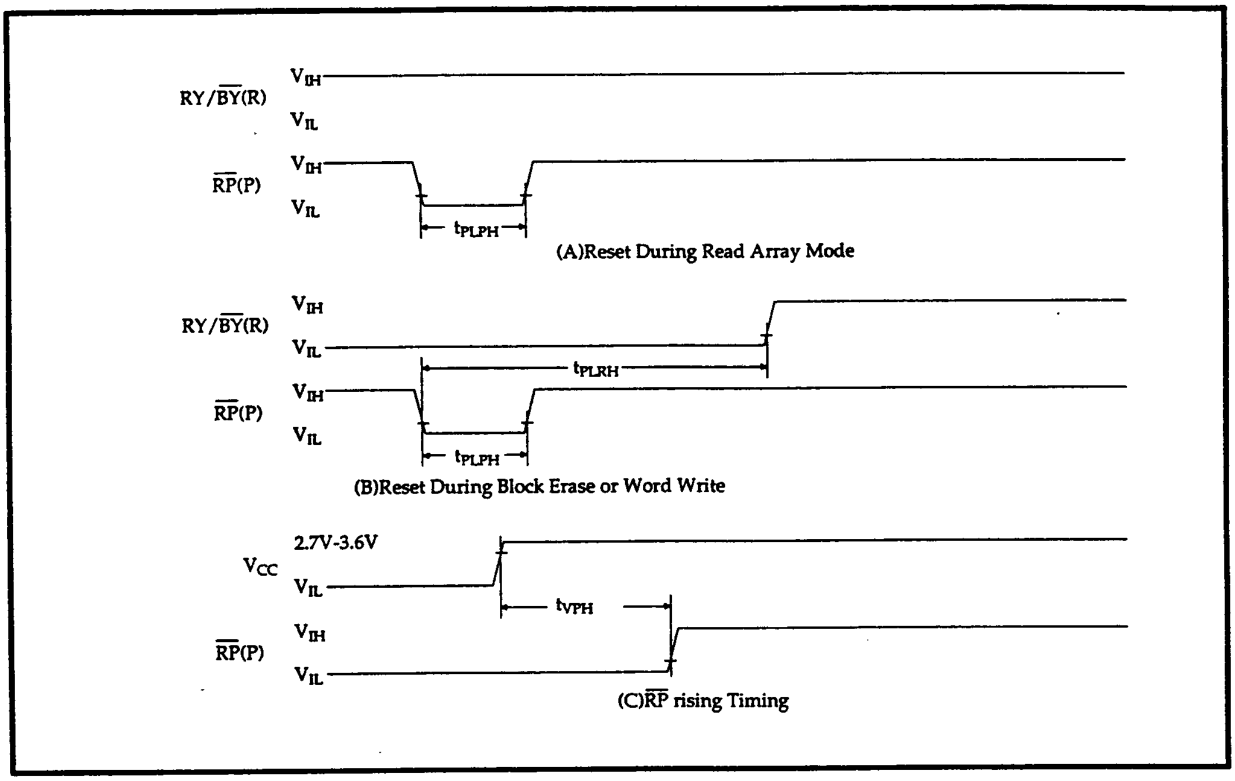


NOTES:

1. V_{CC} power-up and standby.
2. Write block erase or word write setup.
3. Write block erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Figure 12. AC Waveform for $\overline{\text{CE}}$-Controlled Write Operations

6.2.6 RESET OPERATIONS



(A)Reset During Read Array Mode

(B)Reset During Block Erase or Word Write

(C)$\overline{RP}$ rising Timing

Figure 13. AC Waveform for Reset Operation

Reset AC Specifications

Sym	Parameter	Notes	V_{CC}=2.7V		Unit
			Min	Max	
t_{PLPH}	$\overline{RP}$ Pulse Low Time (If $\overline{RP}$ is tied to V_{CC}, this specification is not applicable)		100		ns
t_{PLRH}	$\overline{RP}$ Low to Reset during Block Erase or Word Write	*1,2		22	µs
t_{VPH}	V_{CC} 2.7V to $\overline{RP}$ High	*3	100		ns

NOTES:

*1. If $\overline{RP}$ is asserted while a block erase or word write operation is not executing, the reset will complete within 100ns.

*2. A reset time, t_{PHQV}, is required from the latter of RY/$\overline{BY}$ or $\overline{RP}$ going high until outputs are valid.

*3. When the device power-up, holding $\overline{RP}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.7 BLOCK ERASE AND WORD WRITE PERFORMANCE(*3)

V_{CC}=3.0V-3.6V, T_a=-25°C to +85°C

Sym	Parameter		Notes	V_{PP}=3.0V-3.6V			Unit
				Min	Typ (*1)	Max	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word block	*2		44.6		μs
		4K word block	*2		45.9		
	Word Write Time	32K word block	*2		1.46		sec
		4Kword block	*2		0.19		
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word block	*2		1.14		sec
		4K word block	*2		0.38		
t_{WHRH1} t_{EHRH1}	Word Write Suspend Latency Time to Read				7	8	μs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read				18	22	μs

NOTES:

*1. Typical values measured at T_a=+25°C and nominal voltages. Subject to change based on device characterization.

*2. Excludes system-level overhead.

*3. Sampled but not 100% tested.

Part 3 SRAM
CONTENTS

1.Description

The LRS1314 is a 2M bit static RAM organized as 65,536×16 bit which provides low-power standby mode.

It is fabricated using silicon-gate CMOS process technology.

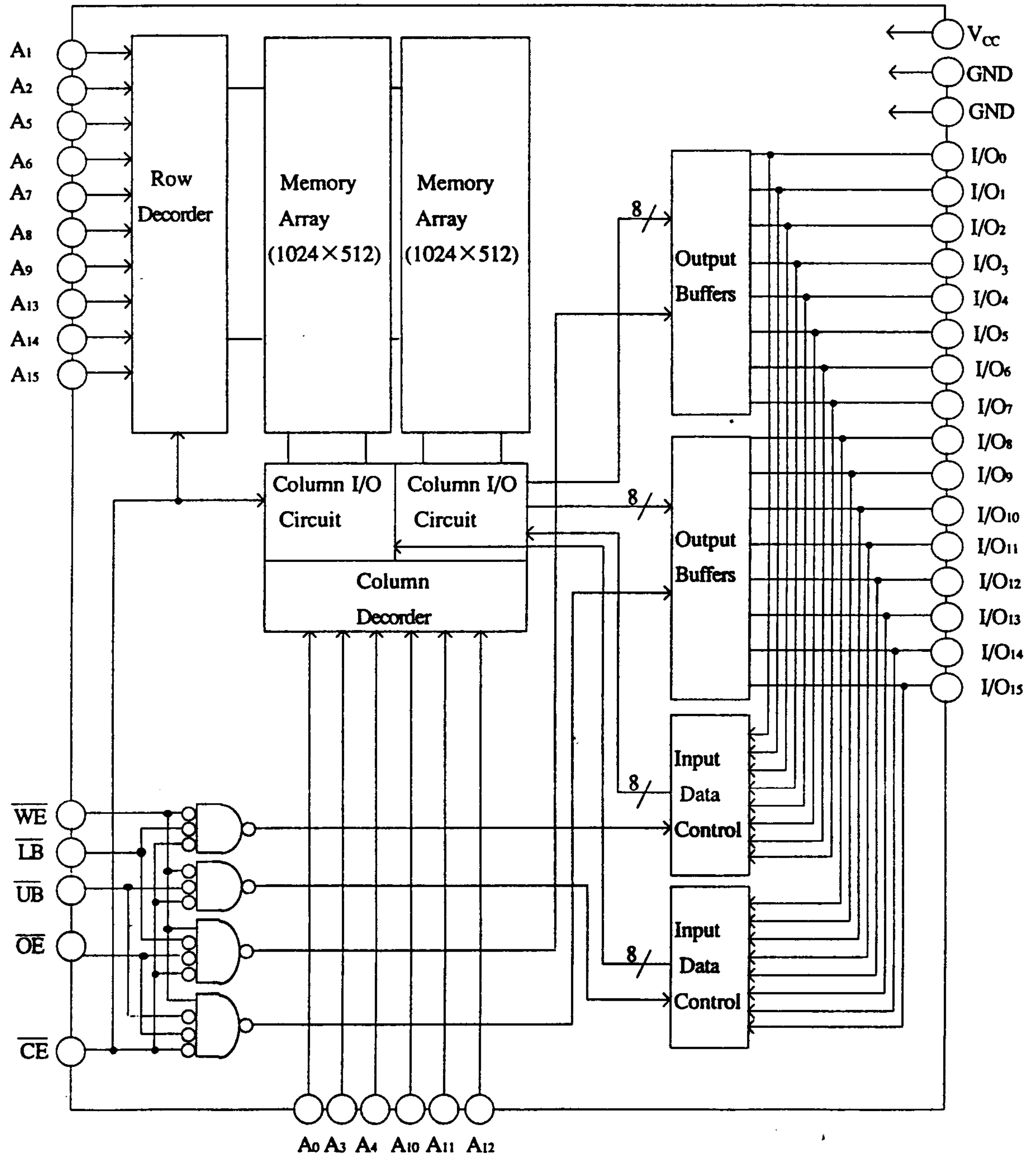
Features

Access Time	85 ns(Max.)
Operating current	45 mA(Max.)
	25 mA(Max. t_{CYCLE}=200ns)
Standby current	25 µA(Max.)
	0.3 µA(Typ. V_{CCDR}=3V, T_a=25℃)
Single power supply	2.7V to 3.6V
Operating temperature	-25℃ to +85℃
Fully static operation	
Three-state output	
Not designed or rated as radiation hardened	
P-type bulk silicon	

3.Truth Table (∗=H or L)

S-$\overline{CE}$	S-$\overline{OE}$	S-$\overline{WE}$	S-$\overline{LB}$	S-$\overline{UB}$	Mode	I/O_0 to I/O_7	I/O_8 to I/O_{15}	Supply current
H	∗	∗	∗	∗	Standby	High impedance	High impedance	Standby(I_{SB})
L	L	H	L	L	Read	Data output	Data output	Active (I_{CC})
			L	H	Read	Data output	High impedance	Active (I_{CC})
			H	L	Read	High impedance	Data output	Active (I_{CC})
L	∗	L	L	L	Write	Data Input	Data Input	Active (I_{CC})
			L	L	Write	Data Input	High impedance	Active (I_{CC})
			H	L	Write	High impedance	Data output	Active (I_{CC})
L	H	H	∗	∗	Output Disable	High impedance	High impedance	Active (I_{CC})
L	∗	∗	H	H	Output Disable	High impedance	High impedance	Active (I_{CC})

4.Block Diagram(V_{CC} means S-V_{CC} .)



4.Absolutc Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage(*1)	V_{CC}	-0.3 to +4.6	V
Input voltage(*1)	V_{IN}	-0.3 (*2) to V_{CC}+0.3	V
Operating temperature	T_{opr}	-25 to +85	℃
Storage temperature	T_{stg}	-65 to +125	℃

Notes

*1. The maximum applicable voltage on any pin with respect to GND.

*2. -3.0V undershoot is allowed to the pulse width less than 50ns.

5.Recommended DC Operating Conditions

(T_a= -25℃ to +85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		V_{CC}+0.3	V
	V_{IL}	-0.3 (*3)		0.8	V

Note

*3. -3.0V undershoot is allowed to the pulse width less than 50ns.

6.DC Electrical Characteristics

(T_a =-25℃ to +85℃, V_{CC}=2.7V to 3.6V)

Parameter	Symbol	Conditions		Min.	Typ. (*4)	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}		-1.0		1.0	µA
Output leakage current	I_{LO}	$\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} $V_{I/O}$=0V to V_{CC}		-1.0		1.0	µA
Operating supply current	I_{CC1}	$\overline{CE}$=V_{IL},V_{IN}=V_{IL} or V_{IH}	t_{CYCLE}=Min $I_{I/O}$=0mA		20	45	mA
	I_{CC2}	$\overline{CE}$≦0.2V V_{IN}=0.2V or V_{CC}−0.2V	t_{CYCLE}=200ns $I_{I/O}$=0mA			25	mA
Standby current	I_{SB}	$\overline{CE}$≧V_{CC}-0.2V			0.3	25	µA
	I_{SB1}	$\overline{CE}$=V_{IH}				3.0	mA
Output voltage	V_{OL}	I_{OL} =2.0mA				0.4	V
	V_{OH}	I_{OH}=-1.0mA		2.4			V

Note

*4. T_a=25℃, V_{CC}=3.0V

7. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.6V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.4V
Output load	1TTL+C_L(30pF) (*5)

Note

＊5.Including scope and jig capacitance.

Read cycle (T$_a$= -25℃ to +85℃ , V$_{CC}$= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Read cycle time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
$\overline{CE}$ access time	t_{ACE}		85	ns	
Output enable to output valid	t_{OE}		45	ns	
Output hold from address change	t_{OH}	10		ns	
$\overline{CE}$ Low to output active	t_{LZ}	10		ns	
$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*6
$\overline{LB}$ or $\overline{UB}$ Low to output active	t_{BLZ}	5		ns	*6
$\overline{CE}$ High to output in High impedance	t_{HZ}	0	40	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	35	ns	*6
$\overline{LB}$ or $\overline{UB}$ High to output active	t_{BHZ}	0	35	ns	*6

Write cycle (T$_a$= -25℃ to +85℃ , V$_{CC}$= 2.7V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
Chip enable to end of write	t_{CW}	70		ns	
Address valid to end of write	t_{AW}	70		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	65		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output active	t_{OW}	5		ns	*6
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	40	ns	*6
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	35	ns	*6

Note

＊6. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

8.Data Retention Characteristics

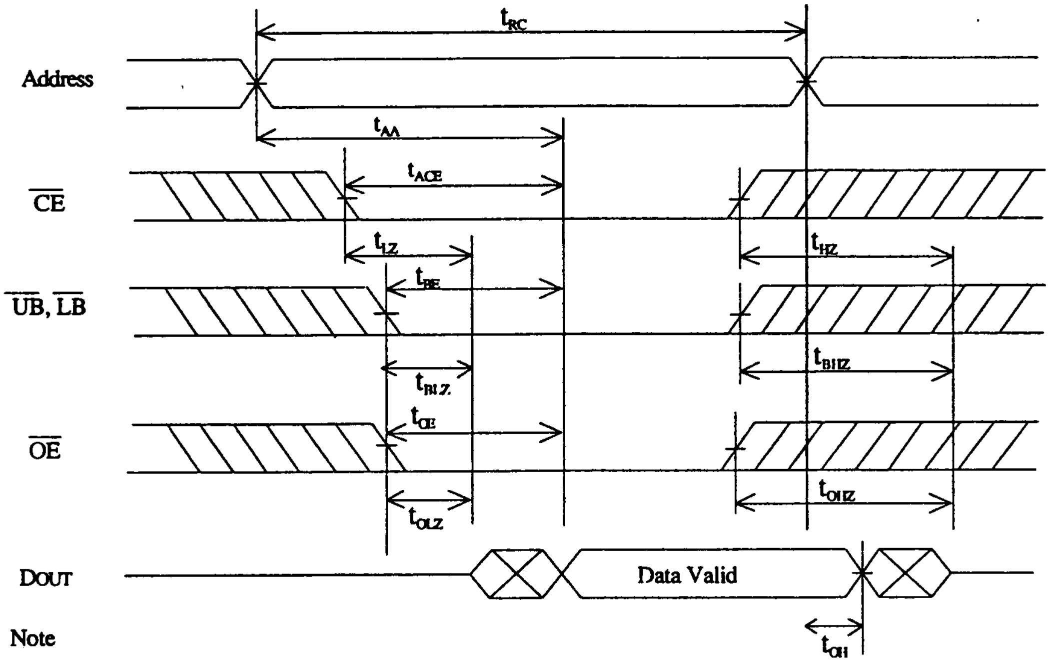
(T_a= -25℃ to +85℃)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$\overline{CE} \geqq V_{CCDR}$-0.2V		2.0		3.6	V
Data Retention supply current	I_{CCDR}	V_{CCDR}=3V $\overline{CE} \geqq V_{CCDR}$-0.2V	T_a=25℃		0.3	1.0	μA
						20	μA
Chip enable setup time	t_{CDR}			0			ms
Chip enable hold time	t_R			(*7) t_{RC}			ms

*7 Read cycle time.

9.Timing Chart

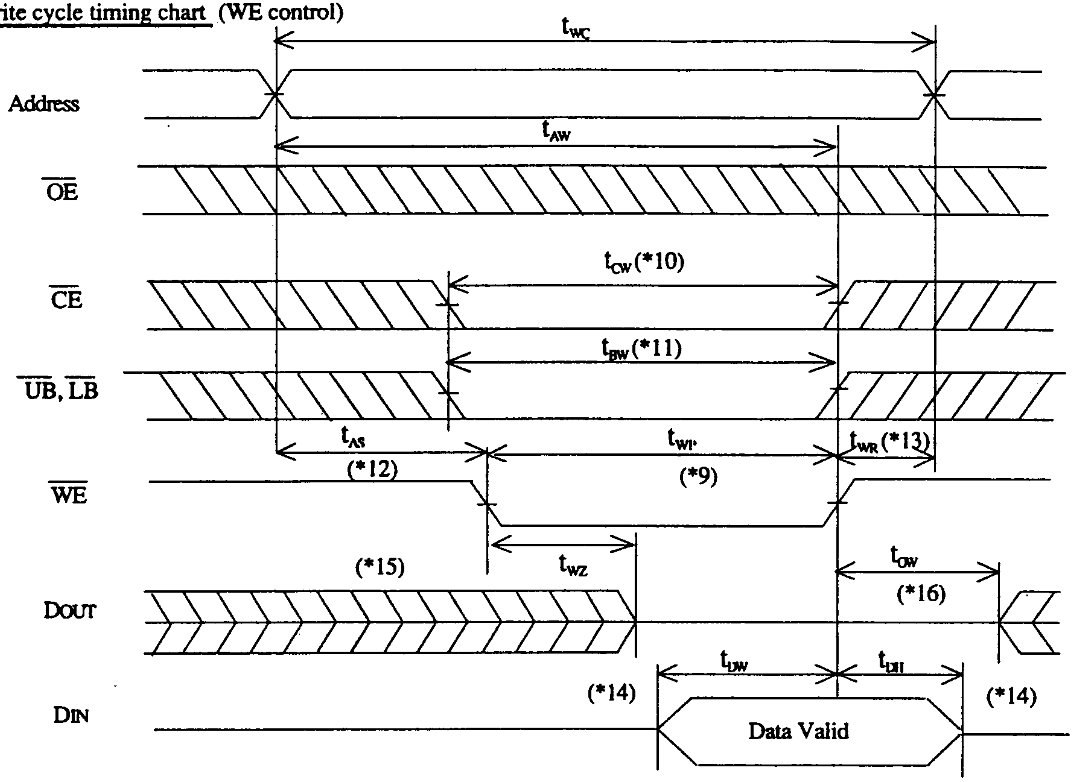
Read cycle timing chart (*8)



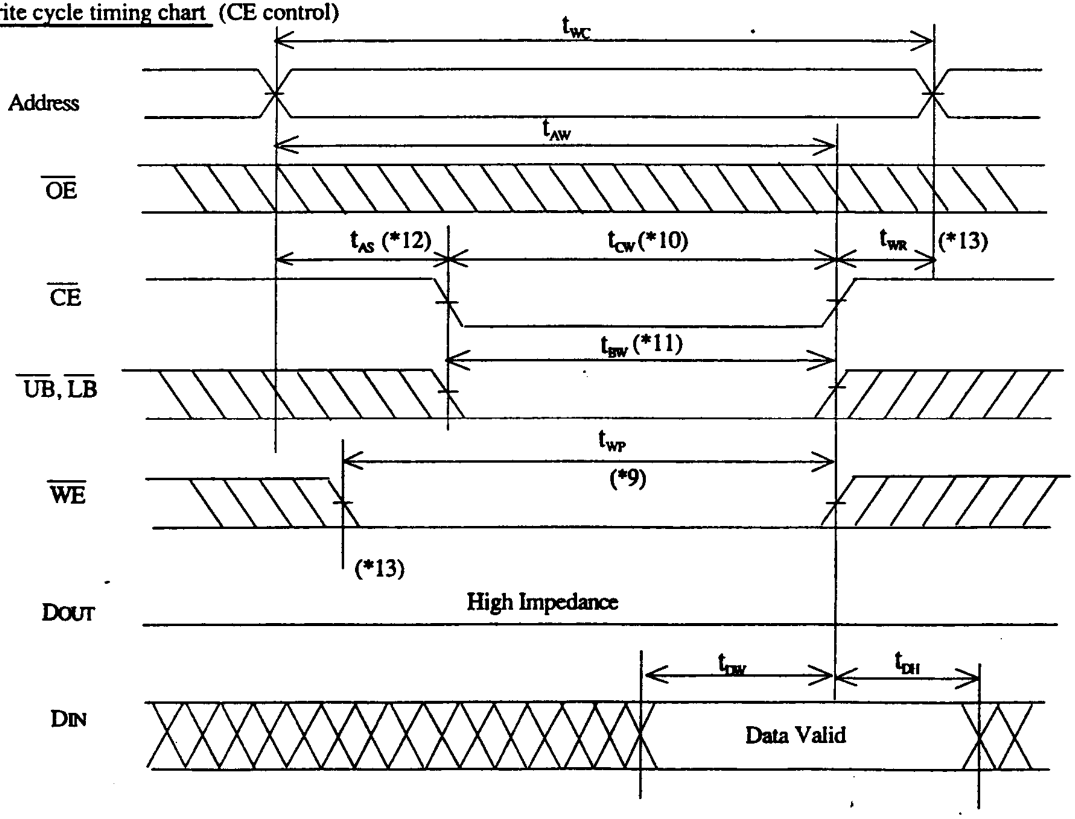
Note

∗ 8. $\overline{WE}$ is high for Read cycle.

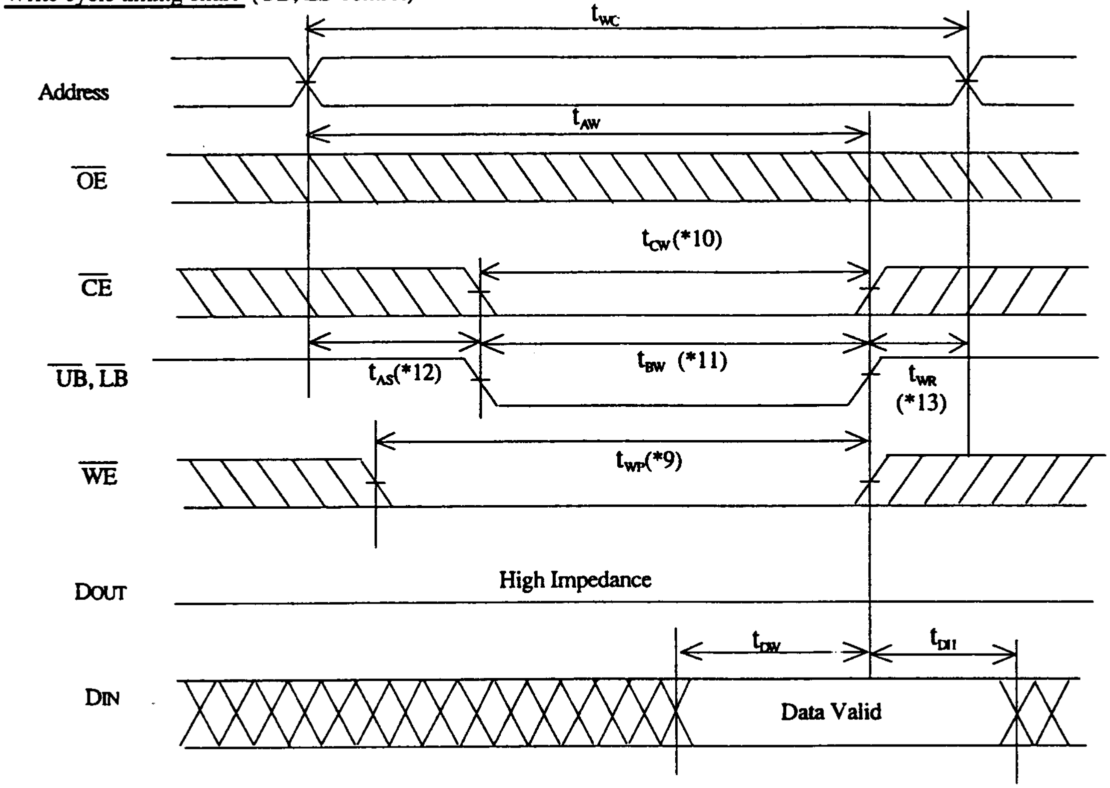
Write cycle timing chart ($\overline{WE}$ control)



Write cycle timing chart ($\overline{CE}$ control)



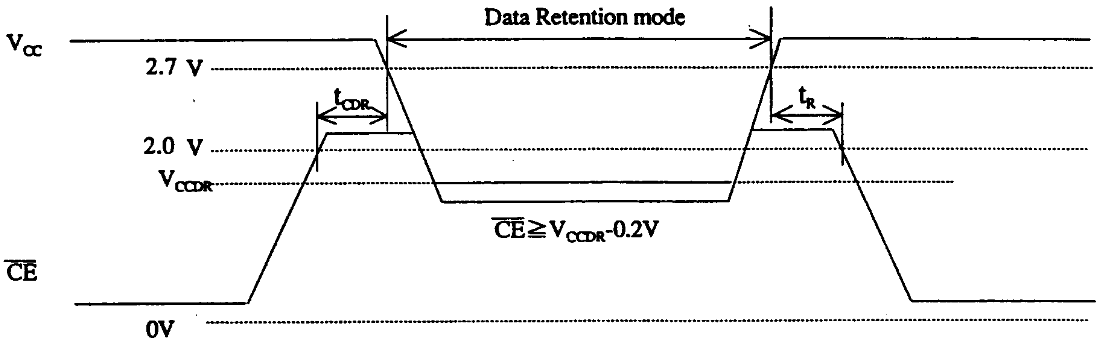
Write cycle timing chart ($\overline{\text{UB}}$, $\overline{\text{LB}}$ control)



Notes

- *9. A write occurs during the overlap of a low $\overline{\text{CE}}$, low $\overline{\text{WE}}$ and low $\overline{\text{UB}}$ or low $\overline{\text{LB}}$.
- *10. t_{CW} is measured from the later of going low $\overline{\text{CE}}$ to the end of write.
- *11. t_{BW} is measured from the later of going low $\overline{\text{UB}}$ or low $\overline{\text{LB}}$ to the end of write.
- *12. t_{AS} is measured from the address valid to the beginning of write.
- *13. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
- *14. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- *15. If $\overline{\text{CE}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
- *16. If $\overline{\text{CE}}$ goes high simultaneously with $\overline{\text{WE}}$ going high or before $\overline{\text{WE}}$ going high, the outputs remain in high impedance state.

Data Retention timing chart



LRS1314, Flash Memory Flash Non-Volatile Memory Flash E2ROM Flash ROM Read Only Memory ETOX Static, SRAM, RAM, Random Access Memory Stacked Chip Combo Chips Combination Chip Stack Chip