L8C211/221/231/241
512/1K/2K/4K x 9-bit Synchronous FIFO

LOGIC DEVICES INCORPORATED

FEATURES

- First-In/First-Out (FIFO) using Dual-Port Memory
- Write and Read Clocks can be synchronous or asynchronous
- Advanced CMOS Technology
- High Speed — to 15 ns Cycle Time
- Empty and Full Warning Flags
- Programmable Almost-Empty and Almost-Full Warning Flags
- Plug Compatible with IDT722x1
- Package Styles Available:
  - 32-pin Plastic LCC, J-Lead

DESCRIPTION

The **L8C211, L8C221, L8C231,** and **L8C241** are synchronous dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

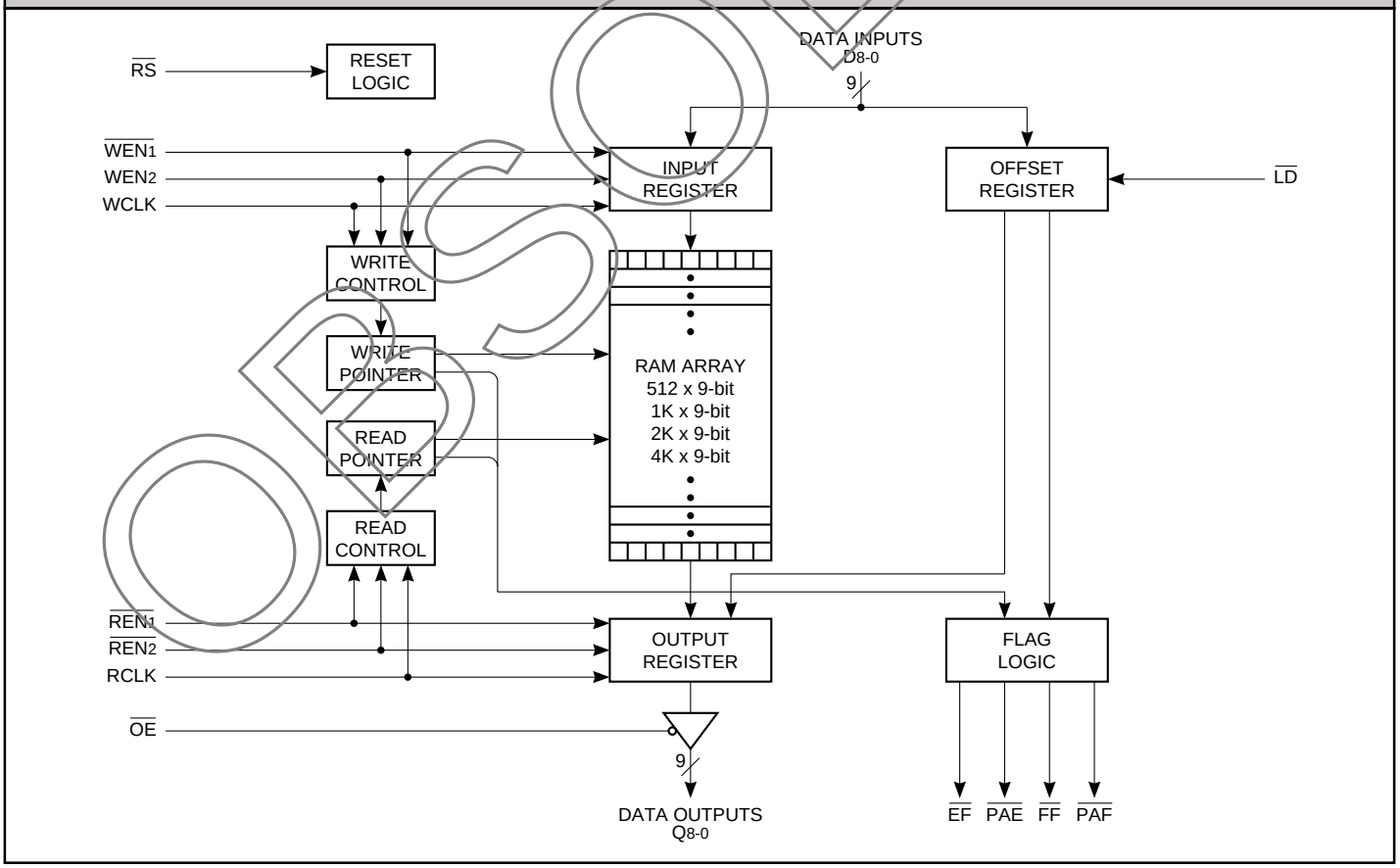
L8C211 — 512 x 9-bit
L8C221 — 1024 x 9-bit
L8C231 — 2048 x 9-bit
L8C241 — 4096 x 9-bit

Each device utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty Flags are provided to prevent data overflow and underflow. Programmable Almost Full and Almost Empty Flags are provided and may be programmed to trigger at any position in the memory array.

The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. Data present at the input port is written to the FIFO if the Write Clock is pulsed when the device is enabled for writing. Data is read from the FIFO if the Read Clock is pulsed when the device is enabled for reading. Multiple FIFOs can be connected together to expand the word width and depth.

These FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

L8C211/221/231/241 BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clocks

WCLK — Write Clock

Data present on D8-0 is written into the FIFO on the rising edge of WCLK when the FIFO is configured for writing. The Full Flag ($\overline{FF}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized to the rising edge of WCLK.

RCLK — Read Clock

Data is read from the FIFO and presented on the output port (Q8-0) after t_D has elapsed from the rising edge of RCLK if the FIFO is configured for reading and if the output port is enabled. The Empty Flag ($\overline{EF}$) and the Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized to the rising edge of RCLK. The Write and Read Clocks can be tied together and driven by the same external clock or they may be controlled by seperate external clocks.

Inputs

$\overline{RS}$ — Reset

A reset occurs when $\overline{RS}$ is set LOW. A reset is required after power-up before a write operation can take place. During reset, the internal read and write pointers are set to the first physical location, the output register is initialized to zero, the offset registers are initialized to their default values (0007H), the Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are set LOW, the Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are set HIGH, and the WEN2/$\overline{LD}$ signal is configured.

$\overline{WEN1}$ — Write Enable 1

If the FIFO is configured to allow loading of the offset registers, $\overline{WEN1}$ is the only write enable. If $\overline{WEN1}$ is LOW, data on D8-0 is written to the FIFO on the rising edge of WCLK. If $\overline{WEN1}$ and $\overline{LD}$ are LOW, data on D8-0 is written to the programmable offset registers as defined in the WEN2/$\overline{LD}$ section. If the FIFO is configured to have two write enables, data on D8-0 is written to the FIFO on the rising edge of WCLK if $\overline{WEN1}$ is LOW and WEN2 is HIGH. When the FIFO is full, $\overline{WEN1}$ is ignored except when loading the offset registers.

WEN2/$\overline{LD}$ — Write Enable 2/Load

The function of this signal is defined during reset. If during reset WEN2/$\overline{LD}$ is HIGH, this signal functions as a second write enable (WEN2). WEN2 is used when depth expansion is needed (see Depth Expansion Mode Section). If during reset WEN2/$\overline{LD}$ is LOW, this signal functions as an offset register load/read control. When WEN2/$\overline{LD}$ is configured to be a write enable, data on D8-0 is written to the FIFO on the rising edge of WCLK if $\overline{WEN1}$ is LOW and WEN2 is HIGH. When the FIFO is full, WEN2 is ignored.

FIGURE 1. OFFSET REGISTERS

L8C211 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	X	X	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	X	X	F8

L8C221 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	X	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	X	F9	F8

L8C231 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	X	E10	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	X	F10	F9	F8

L8C241 OFFSET REGISTERS									
	8	7	6	5	4	3	2	1	0
PAE LSB	X	E7	E6	E5	E4	E3	E2	E1	E0
PAE MSB	X	X	X	X	X	E11	E10	E9	E8
PAF LSB	X	F7	F6	F5	F4	F3	F2	F1	F0
PAF MSB	X	X	X	X	X	F11	F10	F9	F8

E0/FO are the least significant bits.
X = Don't Care.

When WEN2/$\overline{LD}$ is configured to be an offset register load/read control, it is possible to write to or read from the offset registers. The values stored in the offset registers determine how the Programmable Almost-Empty ($\overline{PAE}$) and Programmable Almost-Full ($\overline{PAF}$) Flags operate (see $\overline{PAE}$ and $\overline{PAF}$ sections). There are four 9-bit offset registers. Two are used to control the Programmable Almost-Empty Flag and two are used to control the Programmable Almost-Full Flag (see Figure 1). Data on D8-0 is written to an offset register on the rising edge of WCLK if $\overline{LD}$ and $\overline{WEN1}$ are LOW. After reset, data is written to the offset registers in the following order: PAE LSB, PAE MSB, PAF LSB, PAF MSB. After the PAF MSB register has been loaded, the sequence repeats starting with the PAE LSB register. If register loading is stopped, the next register in sequence will be loaded when the next register write occurs. If $\overline{LD}$, $\overline{REN1}$, and $\overline{REN2}$ are LOW, data is read from an offset register and presented on Q8-0 (if the output port is enabled) after t_D has elapsed from the rising edge of RCLK. The offset registers are read in the same order they are written to. It is not possible to read from and write to the offset registers at the same time.

$\overline{REN1}$, $\overline{REN2}$ — Read Enables 1 and 2

Data is read from the FIFO and presented on Q8-0 after t_D has elapsed from the rising edge of RCLK if $\overline{REN1}$ and $\overline{REN2}$ are LOW and if the output port is enabled. If either Read Enable goes HIGH, the last value loaded in the output register will remain unchanged. The Read Enable signals are ignored when the FIFO is empty.

D8-0 — Data Input

D8-0 is the 9-bit registered data input port.

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, the output port (Q8-0) is enabled for output. When $\overline{OE}$ is HIGH, Q8-0 is placed in a high-impedance state. The flag outputs are not affected by $\overline{OE}$.

Outputs

Q8-0 — Data Output

Q8-0 is the 9-bit registered data output port.

$\overline{FF}$ — Full Flag

The Full Flag goes LOW when the FIFO is full of data. When $\overline{FF}$ is LOW, the FIFO can not be written to. The Full Flag is synchronized to the rising edge of WCLK.

$\overline{EF}$ — Empty Flag

The Empty Flag goes LOW when the read pointer is equal to the write pointer, indicating that the FIFO is empty. When $\overline{EF}$ is LOW, read operations can not be performed. The Empty Flag is synchronized to the rising edge of RCLK.

$\overline{PAF}$ — Programmable Almost-Full Flag

$\overline{PAF}$ goes LOW when the write pointer is (Full – N) locations ahead of the read pointer. N is the value stored in the $\overline{PAF}$ offset register and has a default value of 7. $\overline{PAF}$ is synchronized to the rising edge of WCLK.

$\overline{PAE}$ — Programmable Almost-Empty Flag

$\overline{PAE}$ goes HIGH when the write pointer is (N + 1) locations ahead of the read pointer. N is the value stored in the $\overline{PAE}$ offset register and has a default value of 7. $\overline{PAE}$ is synchronized to the rising edge of RCLK.

OPERATING MODES

Single Device Mode

A single FIFO may be used when the application requirements are for the number of words in a single device.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Any word width can be attained by adding the appropriate number of FIFOs. Status flags can be monitored from any one of the devices.

Depth Expansion Mode

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. If the FIFOs are configured to use WEN2 and external logic is used to direct the flow of data into the cascaded FIFOs, depth expansion can be accomplished.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature ..... –55°C to +125°C
Operating ambient temperature ..... 0°C to +70°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to +7.0 V
Signal applied to high impedance output ..... –0.5 V to +7.0 V
Output current into low outputs ..... 50 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	**Temperature Range** (Ambient)	**Supply Voltage**
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ **V**CC ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ **V**CC ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

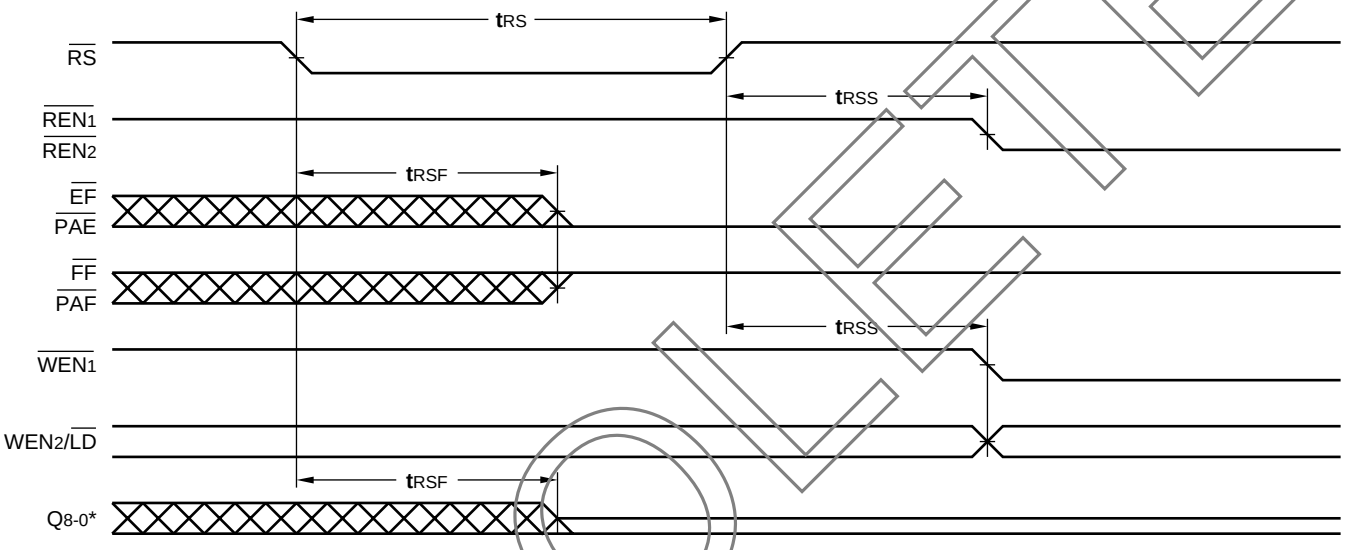
			L8C211/221/231/241			
Symbol	**Parameter**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
VOH	Output High Voltage	**V**CC = 4.5 V, **I**OH = –2.0 mA	2.4			V
VOL	Output Low Voltage	**V**CC = 4.5 V, **I**OL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.0			V
VIL	Input Low Voltage				0.8	V
IIX	Input Leakage Current	Ground ≤ **V**IN ≤ **V**CC	–1		+1	µA
IOZ	Output Leakage Current	Ground ≤ **V**OUT ≤ **V**CC	–10		+10	µA
ICC1	**V**CC Current, Active				90	mA
CIN	Input Capacitance	Ambient Temp = 25°C, **V**CC = 4.5 V			10	pF
COUT	Output Capacitance	Test Frequency = 1 MHz			10	pF

SWITCHING CHARACTERISTICS *Over Operating Range*

RESET TIMING *Notes 3, 4, 5 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{RS}	Reset Pulse Width	50		25		20		15	
t_{RSS}	Reset Setup Time	50		25		20		15	
t_{RSF}	Reset to Flag and Output Valid		50		25		20		15

RESET TIMING



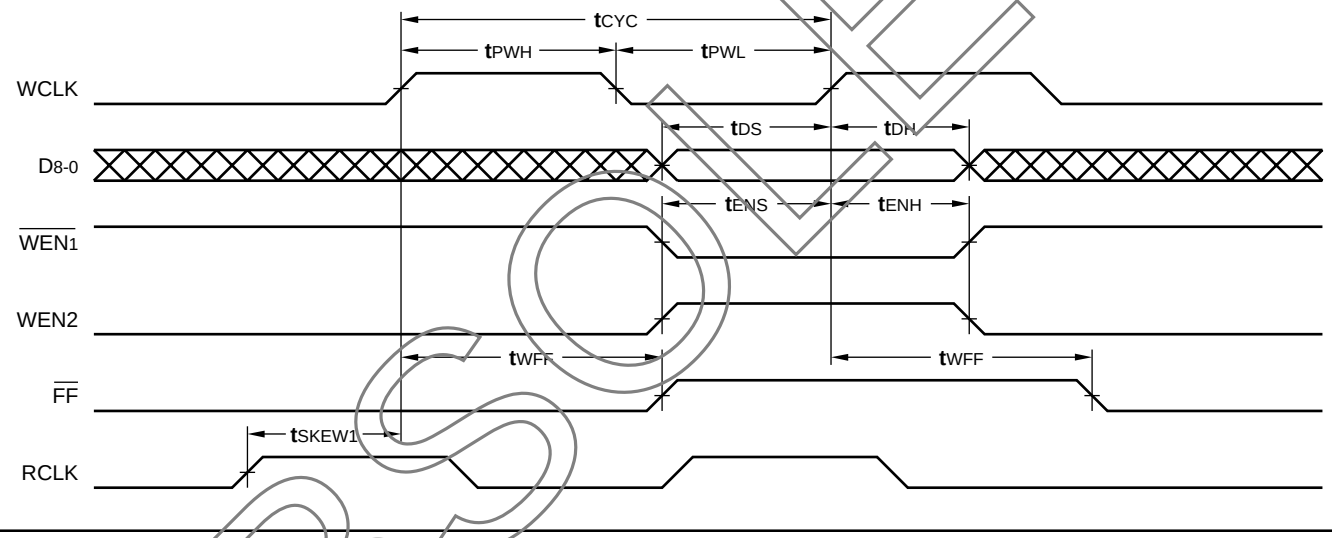
*after reset, Q_{8-0} will be LOW if $\overline{OE}$ = 0 and in HIGH IMPEDANCE if $\overline{OE}$ = 1.

SWITCHING CHARACTERISTICS *Over Operating Range*

WRITE CYCLE TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{WFF}	Write Clock to Full Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags (Note 6)	15		10		8		6	

WRITE CYCLE TIMING

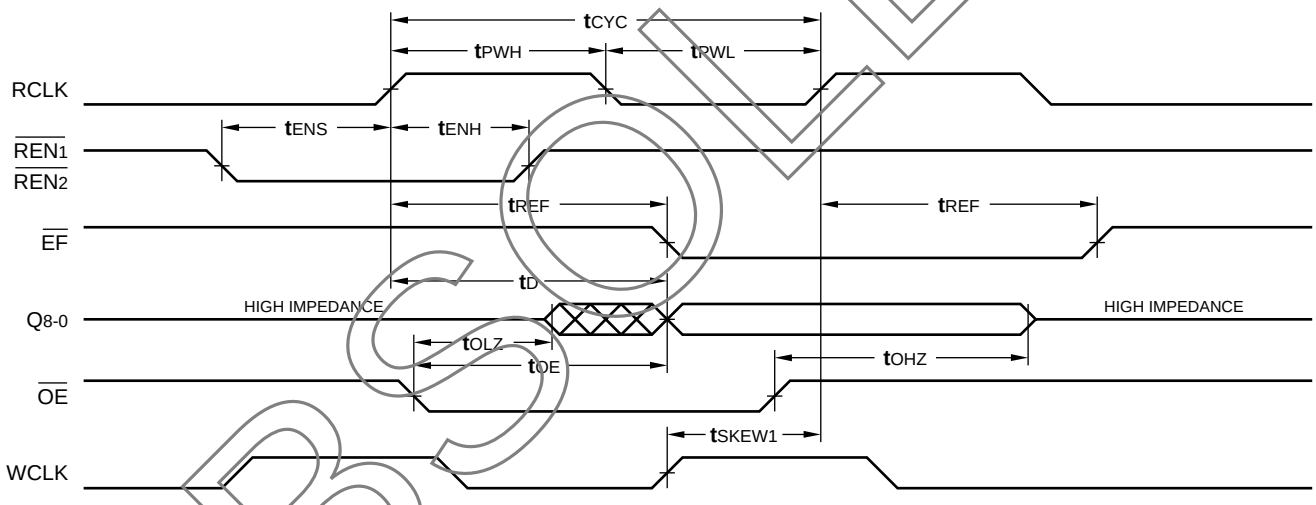


SWITCHING CHARACTERISTICS *Over Operating Range*

READ CYCLE TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{D}	Output Delay	3	25	3	15	2	12	2	10
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	
t_{OHZ}	Output Enable to Output in High Impedance (Notes 7, 8)	3	25	3	13	3	10	3	8
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags (Note 9)	15		10		8		6	

READ CYCLE TIMING

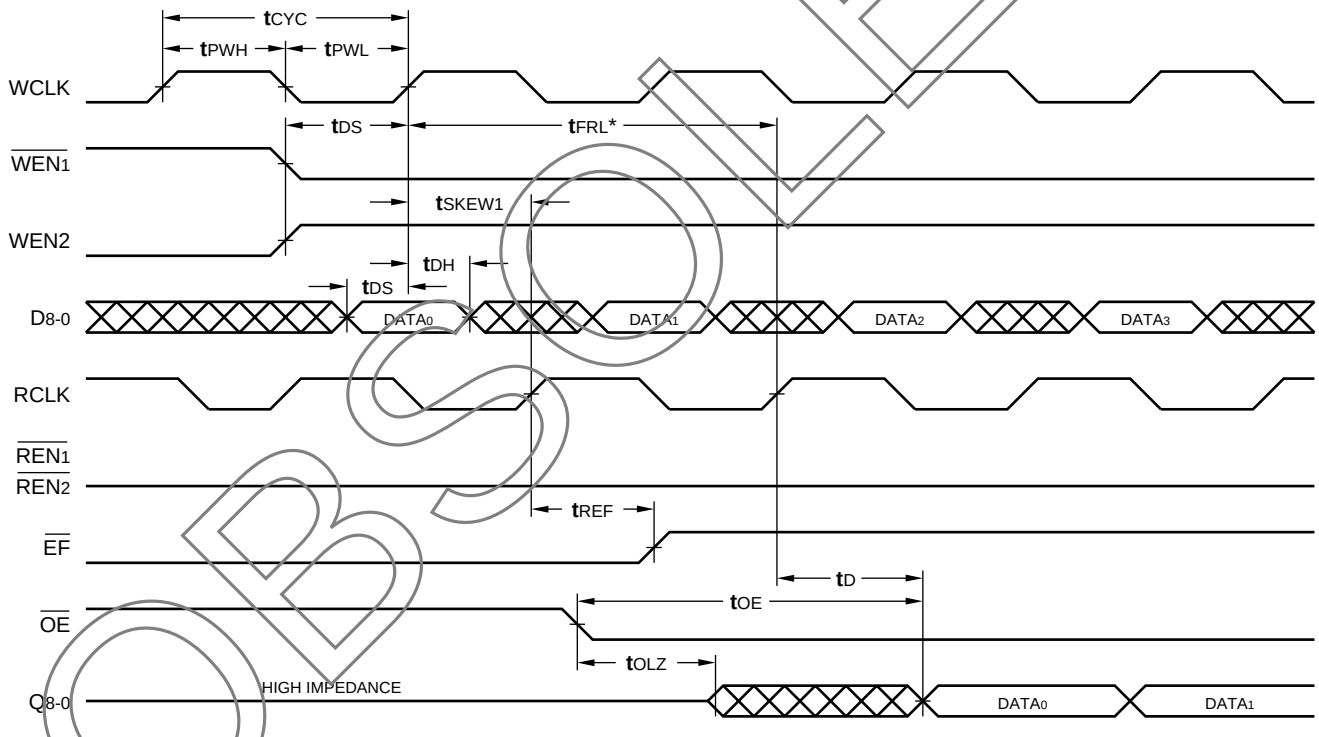


SWITCHING CHARACTERISTICS *Over Operating Range*

FIRST DATA WORD TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{D}	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

FIRST DATA WORD TIMING



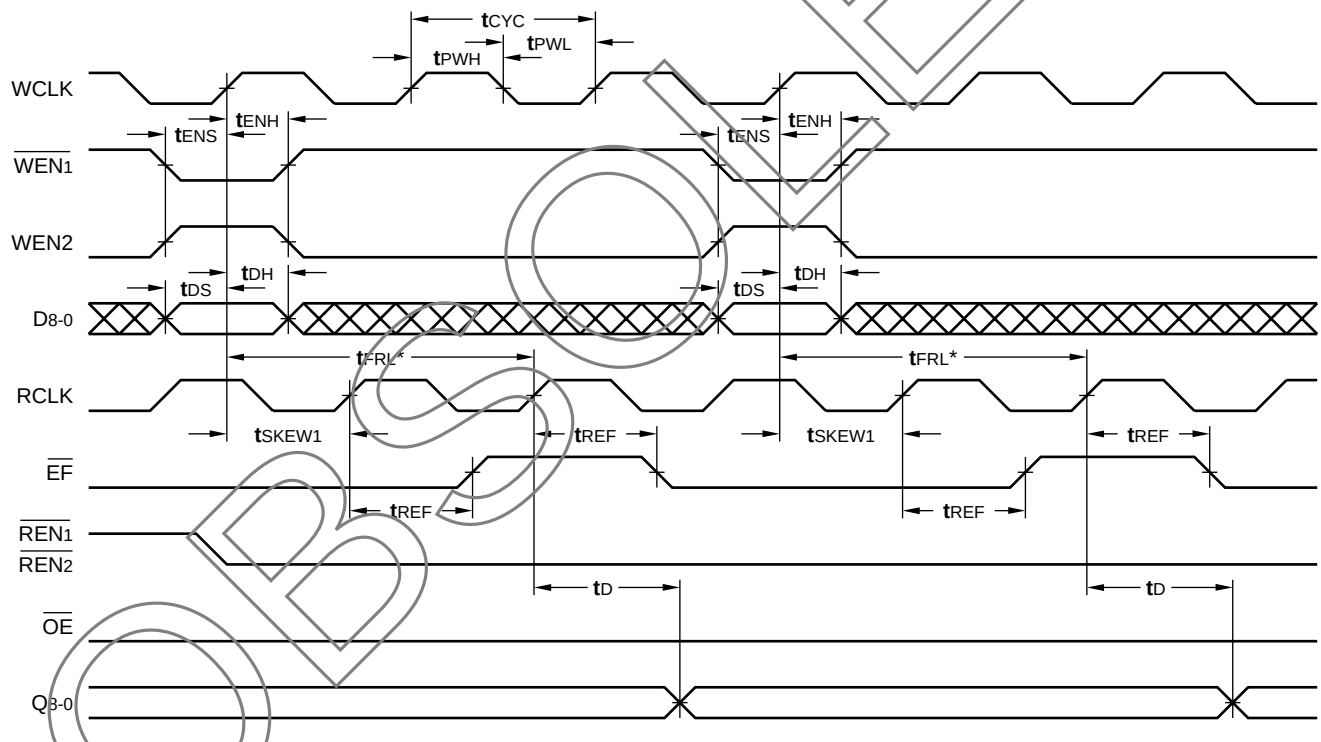
*latency timing is only relevant when the Empty Flag is LOW.
when t_{SKEW1} is less than minimum specification, $t_{FRL} = t_{CYC} + t_{SKEW1}$.
when t_{SKEW1} is greater than minimum specification, $t_{FRL} = 2(t_{CYC}) + t_{SKEW1}$.

SWITCHING CHARACTERISTICS *Over Operating Range*

EMPTY FLAG TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{D}	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{REF}	Read Clock to Empty Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

EMPTY FLAG TIMING



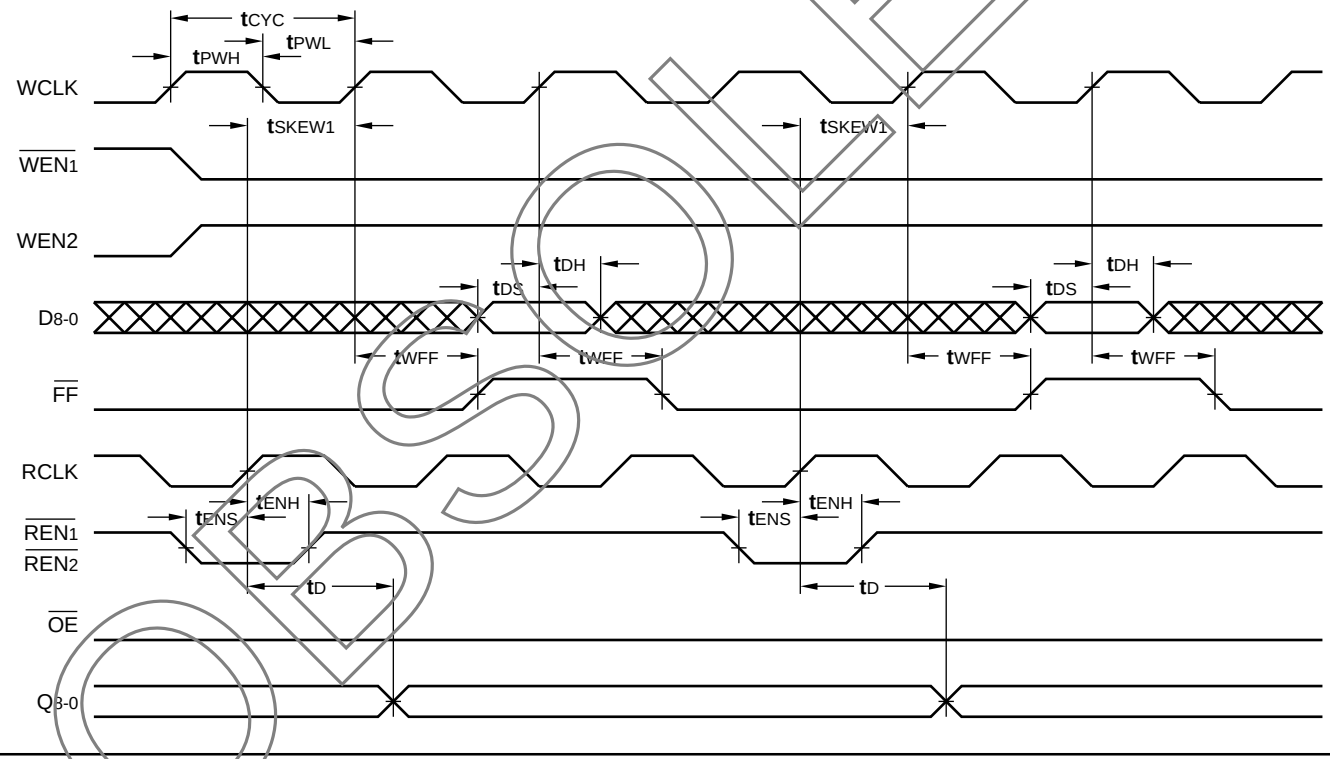
*latency timing is only relevant when the Empty Flag is LOW.
when t_{SKEW1} is less than minimum specification, $t_{FRL} = t_{CYC} + t_{SKEW1}$.
when t_{SKEW1} is greater than minimum specification, $t_{FRL} = 2(t_{CYC}) + t_{SKEW1}$.

SWITCHING CHARACTERISTICS *Over Operating Range*

FULL FLAG TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{D}	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{WFF}	Write Clock to Full Flag		25		15		12		10
t_{SKEW1}	Skew Time Between Read and Write Clocks for Empty and Full Flags	15		10		8		6	

FULL FLAG TIMING

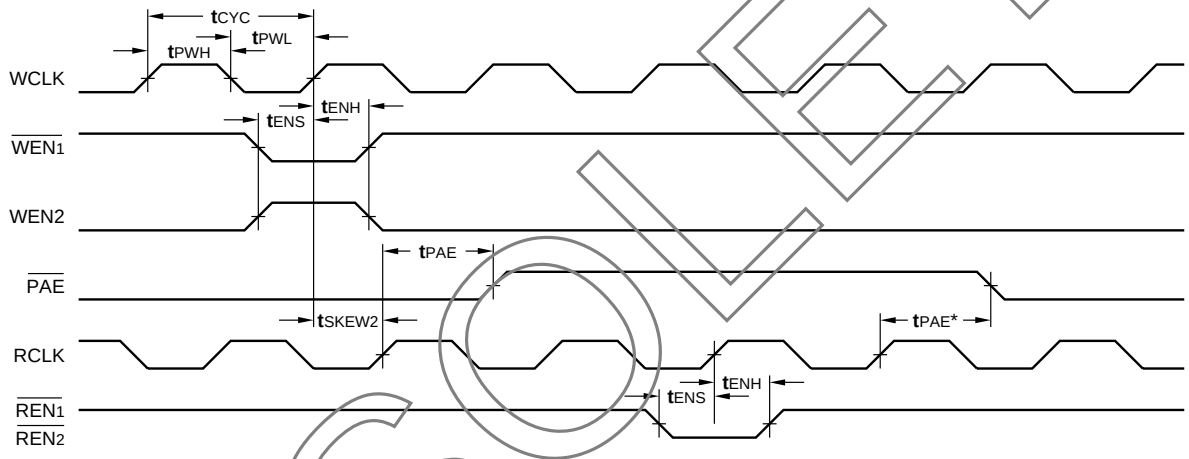


SWITCHING CHARACTERISTICS *Over Operating Range*

PROGRAMMABLE ALMOST-EMPTY/FULL FLAG TIMING *Notes 3, 4 (ns)*

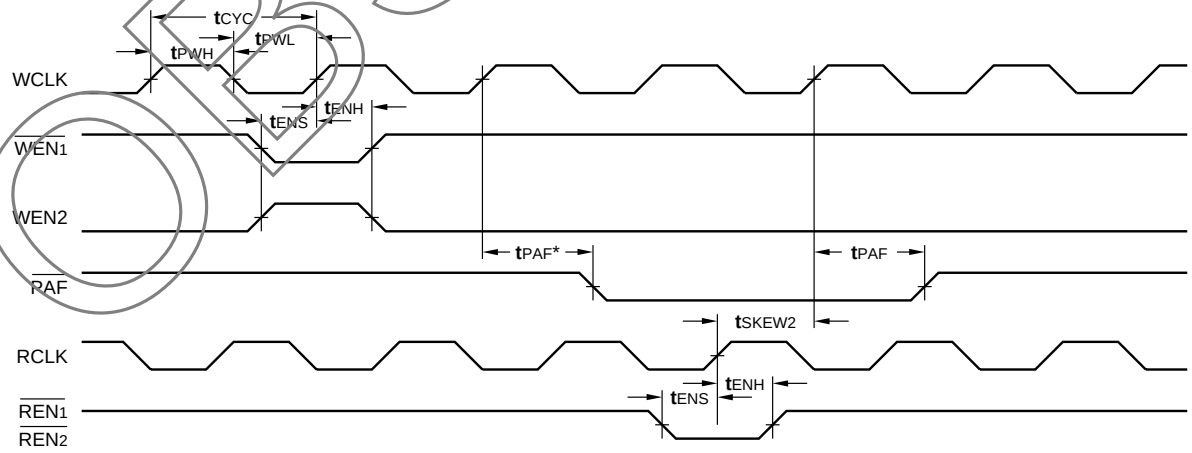
		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{PAF}	Write Clock to Programmable Almost-Full Flag		25		15		12		10
t_{PAE}	Read Clock to Programmable Almost-Empty Flag		25		15		12		10
t_{SKEW2}	Skew Time Between Read/Write Clocks for Almost-Empty/Full Flags	30		20		18		15	

PROGRAMMABLE ALMOST-EMPTY FLAG *Note 10*



*$\overline{PAE}$ is synchronized to the rising edge of RCLK, but in this case the $\overline{PAE}$ transition takes place in the next clock cycle.

PROGRAMMABLE ALMOST-FULL FLAG *Note 11*



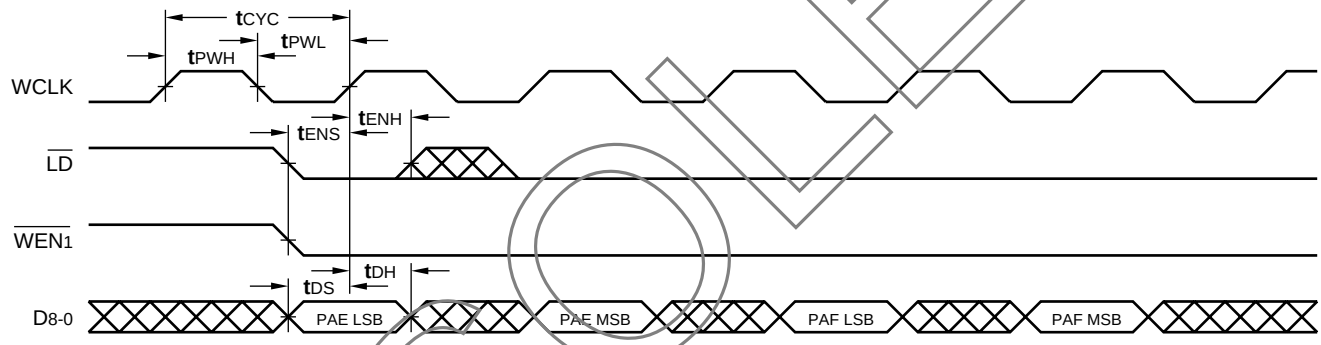
*$\overline{PAF}$ is synchronized to the rising edge of WCLK, but in this case the $\overline{PAF}$ transition takes place in the next clock cycle.

SWITCHING CHARACTERISTICS *Over Operating Range*

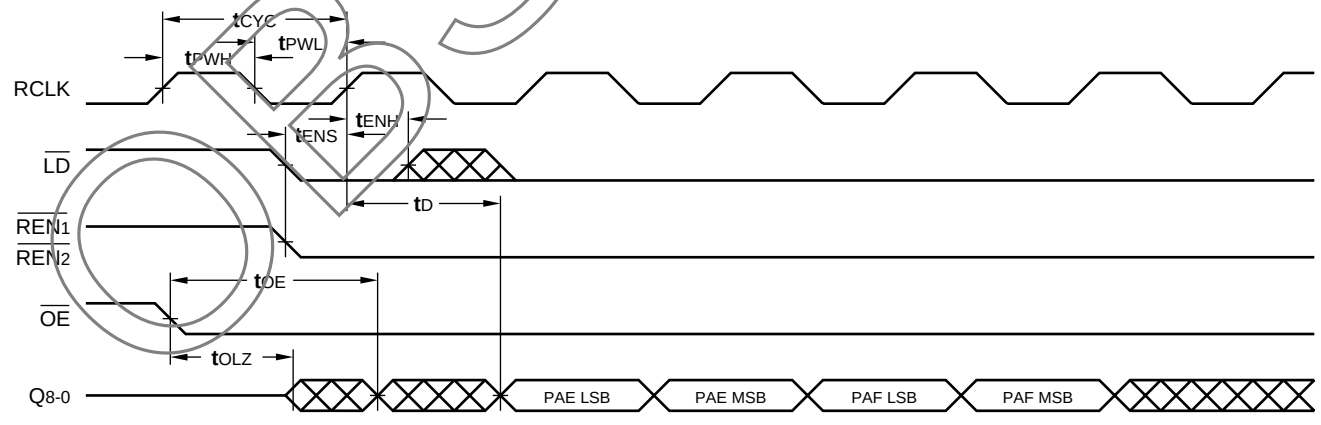
WRITE/READ OFFSET REGISTER TIMING *Notes 3, 4 (ns)*

		L8C211/221/231/241–							
		50		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		25		20		15	
t_{PWH}	Clock Pulse Width HIGH	20		10		8		6	
t_{PWL}	Clock Pulse Width LOW	20		10		8		6	
t_{D}	Output Delay	3	25	3	15	2	12	2	10
t_{DS}	Data Setup Time	10		6		5		4	
t_{DH}	Data Hold Time	1		1		1		1	
t_{ENS}	Enable Setup Time	10		6		5		4	
t_{ENH}	Enable Hold Time	1		1		1		1	
t_{OE}	Output Enable to Output Valid	3	25	3	13	3	10	3	8
t_{OLZ}	Output Enable to Output in Low Impedance (Notes 7, 8)	0		0		0		0	

WRITE OFFSET REGISTER



READ OFFSET REGISTER



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V (Fig. 2).

4. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{DS} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

5. The Read and Write Clocks can be free-running during reset.

6. t_{SKEW1} is the minimum time between the rising edge of RCLK and the rising edge of WCLK for a Full Flag transition to occur in that clock cycle. If t_{SKEW1} is not satisfied, a Full Flag transition may not occur until the next rising WCLK edge.

7. These parameters are guaranteed but not 100% tested.

8. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

9. t_{SKEW1} is the minimum time between the rising edge of WCLK and the rising edge of RCLK for an Empty Flag transition to occur in that clock cycle. If t_{SKEW1} is not satisfied, an Empty Flag transition may not occur until the next rising RCLK edge.

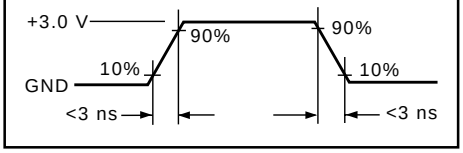
10. t_{SKEW2} is the minimum time between the rising edge of WCLK and the rising edge of RCLK to guarantee that the Programmable Almost-Empty Flag will make a transition to HIGH during that clock cycle. If t_{SKEW2} is not satisfied, the Programmable Almost-Empty Flag may not make the transition to HIGH until the next rising edge of RCLK.

11. t_{SKEW2} is the minimum time between the rising edge of RCLK and the rising edge of WCLK to guarantee that the Programmable Almost-Full Flag will make a transition to HIGH during that clock cycle. If t_{SKEW2} is not satisfied, the Programmable Almost-Full Flag may not make the transition to HIGH until the next rising edge of WCLK.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

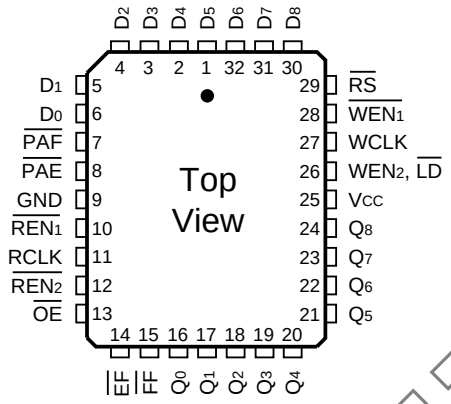
13. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 2.



L8C211 — ORDERING INFORMATION

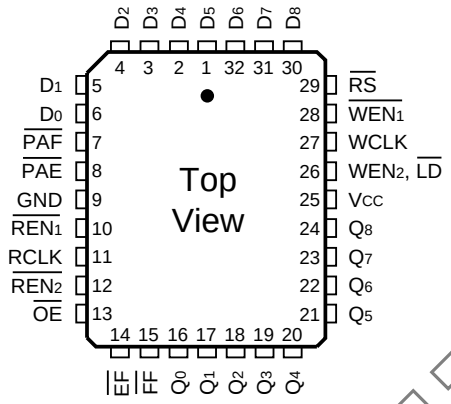
32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C211JC50
25 ns	L8C211JC25
20 ns	L8C211JC20
15 ns	L8C211JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C211JI50
25 ns	L8C211JI25
20 ns	L8C211JI20
15 ns	L8C211JI15

L8C221 — ORDERING INFORMATION

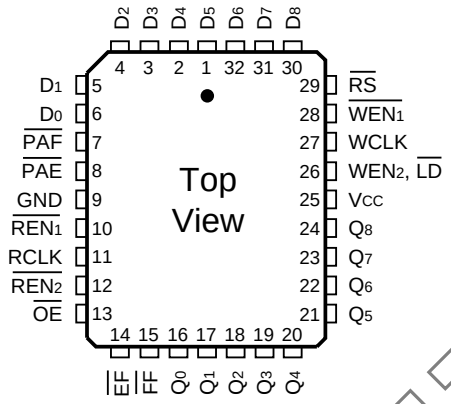
32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C221JC50
25 ns	L8C221JC25
20 ns	L8C221JC20
15 ns	L8C221JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C221JI50
25 ns	L8C221JI25
20 ns	L8C221JI20
15 ns	L8C221JI15

L8C231 — ORDERING INFORMATION

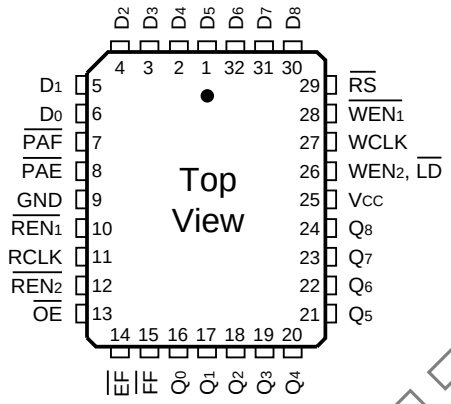
32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C231JC50
25 ns	L8C231JC25
20 ns	L8C231JC20
15 ns	L8C231JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C231JI50
25 ns	L8C231JI25
20 ns	L8C231JI20
15 ns	L8C231JI15

L8C241 — ORDERING INFORMATION

32-pin



Speed	Plastic J-Lead Chip Carrier (J6)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	L8C241JC50
25 ns	L8C241JC25
20 ns	L8C241JC20
15 ns	L8C241JC15
	–40°C to +85°C — COMMERCIAL SCREENING
50 ns	L8C241JI50
25 ns	L8C241JI25
20 ns	L8C241JI20
15 ns	L8C241JI15