Preliminary

N-Channel Enhancement-Mode DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-236AB*	Die
500V	1.0KΩ	3.0mA	LNE150K1	LNE150ND

*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

Product marking for TO-236AB:

NEE✳

where ✳ = 2-week alpha date code

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain

Applications

- ☐ Logic level interface - ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	-0.7V to +10V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

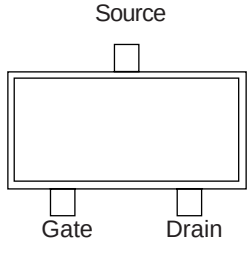
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

This low threshold Enhancement-mode (normally-off) transistor utilizes an advanced DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



TO-236AB

(SOT-23)

top view

Note: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_A = 25°C	θ_{jc} °C/W	θ_a °C/W	I_{DR}	I_{DRM}
TO-236AB	3mA	20mA	0.36W	200	350	3mA	20mA

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500			V	V_{GS} = 0V, I_D = 100µA
BV_{GSS}	Gate-to-Source Diode Breakdown Voltage	10			V	I_{GS} = 100µA
V_{SG}	Source-to-Gate diode Forward Voltage Drop			0.7	V	I_{SG} = 100µA
I_{SG}	Source-to-Gate Continuous Diode Current			3	mA	V_{DS} = 0V
$V_{GS(TH)}$	Gate Threshold Voltage	0.6		2.5	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(TH)}$	Change in $V_{GS(TH)}$ with Temperature			-4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage Current			50	nA	V_{GS} = +5.0V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	V_{GS} =0V, V_{DS} = 500V
$I_{D(ON)}$	ON-State Drain Current	3			mA	V_{GS} = 5.0V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.0	KΩ	V_{GS} = 5.0V, I_D = 500µA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/°C	V_{GS} = 0V, I_D = 500µA
C_{ISS}	Input Capacitance		12		pF	V_{GS} = 0V, V_{DS} = 25V, f=1.0MHz
C_{OSS}	Common Source Output Capacitance		2			
C_{RSS}	Reverse Transfer Capacitance		0.8			
t_{ON}	Turn-ON Time			10	ns	V_{GS} = 0V to 5V, R_{GEN} = 100Ω, V_{DD} = 1.0V, R_{load} = 200Ω
t_{OFF}	Turn-OFF Time			10		
V_{SD}	Diode forward Voltage Drop			1.8	V	V_{GS} = 0V, I_{SD} = 3.0mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit