# SHARP

## LH28F160SPN 16M (2M × 8/1M × 16) Page Mode Flash Memory

#### **FEATURES**

- High speed page mode read performance
  - Normal access time 100 ns
  - Page mode access time 50 ns
- Page depth 16 bytes/8 words
- High speed write performance
  - 32 bytes × 2 plane page buffer
- · High-density symmetrically blocked architecture
  - Thirty-two 64KB erasable blocks
- Enhanced data protection features
  - Flexible block locking
  - Erase/Write lockout during power transitions
- Low power management
  - Deep power-down mode 15 μA (MAX.)
- User configurable x8 or x16 operation
- Extended cycling capability
  - 100,000 block erase cycles
  - 3.2 million block erase cycles/chip
- Enhanced automated syspend options
  - Write suspend to read
  - Block erase suspend to write
  - Block erase suspend to read
- Power supply 3.3 V  $\pm 0.3$  V
- 44-pin SOP Package
- Not designed or rated as radiation hardened

#### **DESCRIPTION**

The LH28F160SPN is a high-performance 16M page mode flash memory organized as  $2M \times 8/1M \times 16$ . The 2MB of data is arranged in thirty-two 64KB blocks which are individually erasable, lockable, and unlockable in-system.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically **APPLICATIONS:**•
Barcode Scanner

executes the algorithms and timings necessary for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

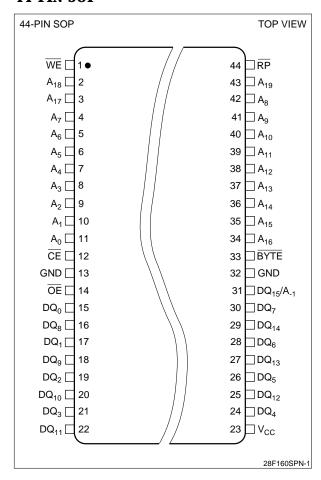
Each block can be independently erased 100,000 times (3.2 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

(Multi) word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of 32 block lockbits gate and  $\overline{RP}$  to lock and unlock bits. Block lock-bits block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (set block lock-bits and clear block lock-bits commands) set and cleared block lock bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

### 44-PIN SOP



This Product Information is from Specification No. FM983017; Issue Date: March 13, 1998.